

1. Description

1.1. Project

Project Name	Disco_F746_FATFS_uSD_RTOS_v	
	1	
Board Name	STM32F746G-DISCO	
Generated with:	STM32CubeMX 6.7.0	
Date	05/13/2023	

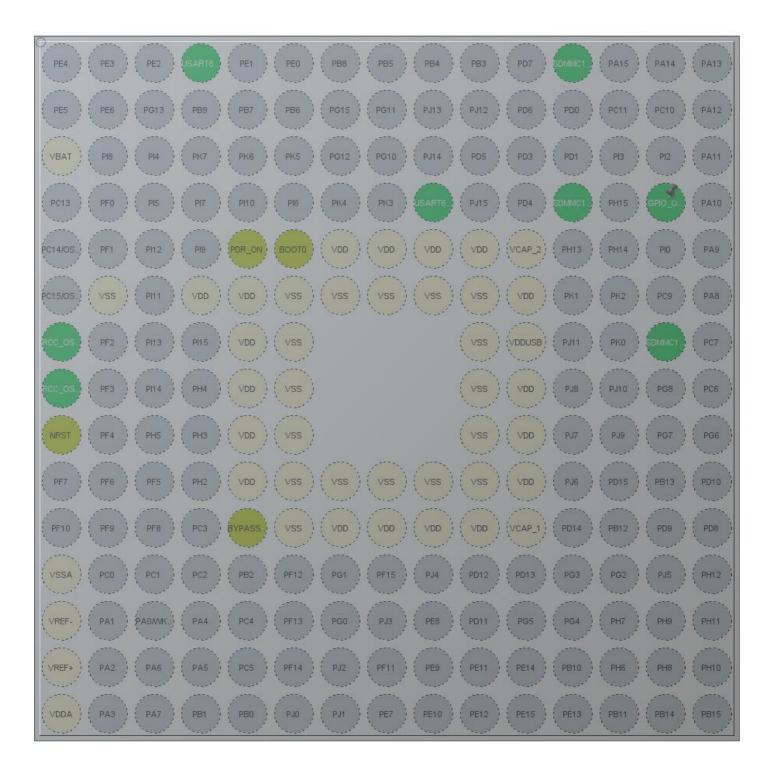
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



TFBGA216 (Top view)

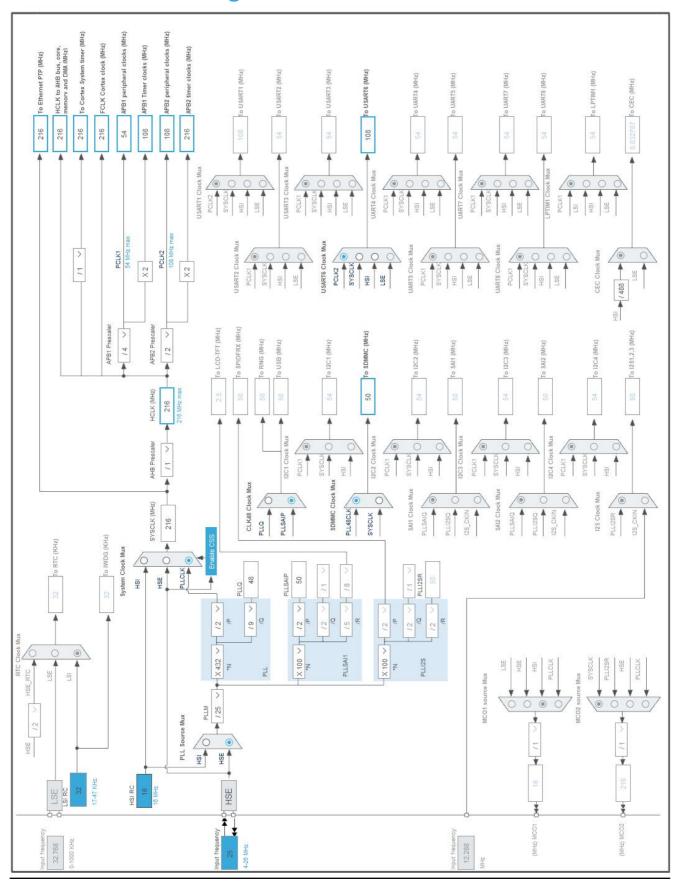
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA216	(function after		Function(s)	
	reset)			
A4	PG14	I/O	USART6_TX	
A12	PC12	I/O	SDMMC1_CK	
C1	VBAT	Power		
D9	PG9	I/O	USART6_RX	
D12	PD2	I/O	SDMMC1_CMD	
D14	PI1 *	I/O	GPIO_Output	
E5	PDR_ON	Reset		
E6	ВООТ0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G14	PC8	I/O	SDMMC1_D0	
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power		
J1	NRST	Reset		
J5	VDD	Power		
J6	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J10	VSS	Power		
J11	VDD	Power		
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
M1	VSSA	Power		
N1	VREF-	Power		
P1	VREF+	Power		
R1	VDDA	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	Disco_F746_FATFS_uSD_RTOS_v1
Project Folder	C:\Users\toussaij\Documents\STM32dev\Disco_F746_FATFS_uSD_RTOS_v1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_SDMMC1_SD_Init	SDMMC1
5	MX_USART6_UART_Init	USART6

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
мси	STM32F746NGHx
Datasheet	DS10916_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

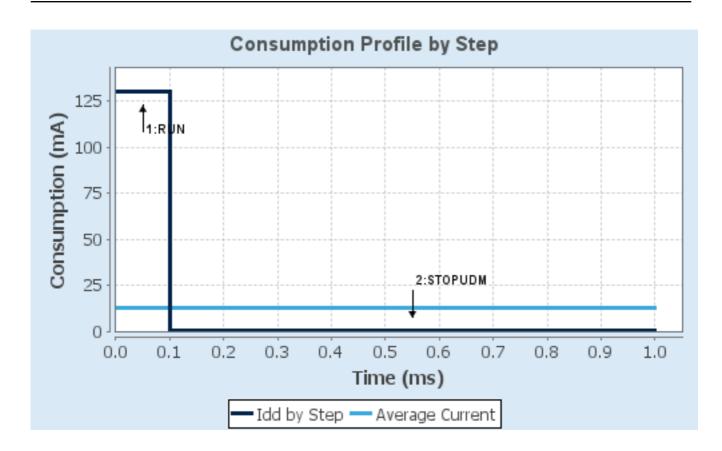
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	92.56	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005
			DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Over Drive Enabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.2. SDMMC1 Mode: SD 1 bit

7.2.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made Rising transition

SDMMC Clock divider bypass Disable

SDMMC Clock output enable when the bus is idle

Disable the power save for the clock

SDMMC hardware flow control

The hardware control flow is disabled

SDMMCCLK clock divide factor 32 *

7.3. SYS

Timebase Source: SysTick

7.4. USART6

Mode: Asynchronous 7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

7.5. FREERTOS

Interface: CMSIS_V1

7.5.1. Config parameters:

API:

FreeRTOS API CMSIS v1

Versions:

FreeRTOS version 10.2.1 CMSIS-RTOS version 1.02

MPU/FPU:

ENABLE_MPU Disabled ENABLE_FPU Disabled

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000
MAX_PRIORITIES 7
MINIMAL_STACK_SIZE 128
MAX_TASK_NAME_LEN 16

USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD E	Enabled
USE_MUTEXES E	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE 8	3
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY E	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION E	Enabled
USE_TICKLESS_IDLE D	Disabled
USE_TASK_NOTIFICATIONS E	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 15360

Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Disabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t
USE_POSIX_ERRNO Disabled

7.5.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled Enabled uxTaskPriorityGet Enabled vTaskDelete Disabled vTaskCleanUpResources vTaskSuspend Enabled Disabled vTaskDelayUntil Enabled vTaskDelay Enabled xTaskGetSchedulerState Enabled xTaskResumeFromISR xQueueGetMutexHolder Disabled Disabled xSemaphoreGetMutexHolder Disabled pcTaskGetTaskName Disabled uxTaskGetStackHighWaterMark Disabled xTaskGetCurrentTaskHandle eTaskGetState Disabled Disabled $x \\ Event Group Set Bit From ISR$ xTimerPendFunctionCall Disabled xTaskAbortDelay Disabled xTaskGetHandle Disabled Disabled uxTaskGetStackHighWaterMark2

7.5.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Enabled *

Project settings (see parameter description first):

Use FW pack heap file Enabled

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0/OSC_I N	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC12	SDMMC1_CK	Alternate Function Push Pull	Pull-up *	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	Pull-up *	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	Pull-up *	Very High	
USART6	PG14	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG9	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PI1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SDMMC1_RX	DMA2_Stream3	Peripheral To Memory	High *
SDMMC1_TX	DMA2_Stream6	Memory To Peripheral	High *

SDMMC1_RX: DMA2_Stream3 DMA request Settings:

Mode: Peripheral Flow Control *

Use fifo: Enable *

FIFO Threshold: Full
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word *
Memory Data Width: Word

Peripheral Burst Size: 4 Increment *

Memory Burst Size: 4 Increment

SDMMC1_TX: DMA2_Stream6 DMA request Settings:

Mode: Peripheral Flow Control *

Use fifo: Enable *

FIFO Threshold: Full
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word *

Peripheral Burst Size: 4 Increment *
Memory Burst Size: 4 Increment

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	15	0	
System tick timer	true	15	0	
DMA2 stream3 global interrupt	true	5	0	
DMA2 stream6 global interrupt	true	5	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt		unused		
SDMMC1 global interrupt	unused			
USART6 global interrupt	unused			
FPU global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	true	true
DMA2 stream3 global interrupt	false	false	true
DMA2 stream6 global interrupt	false	false	true

* User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f7 svd.zip

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