1. Description

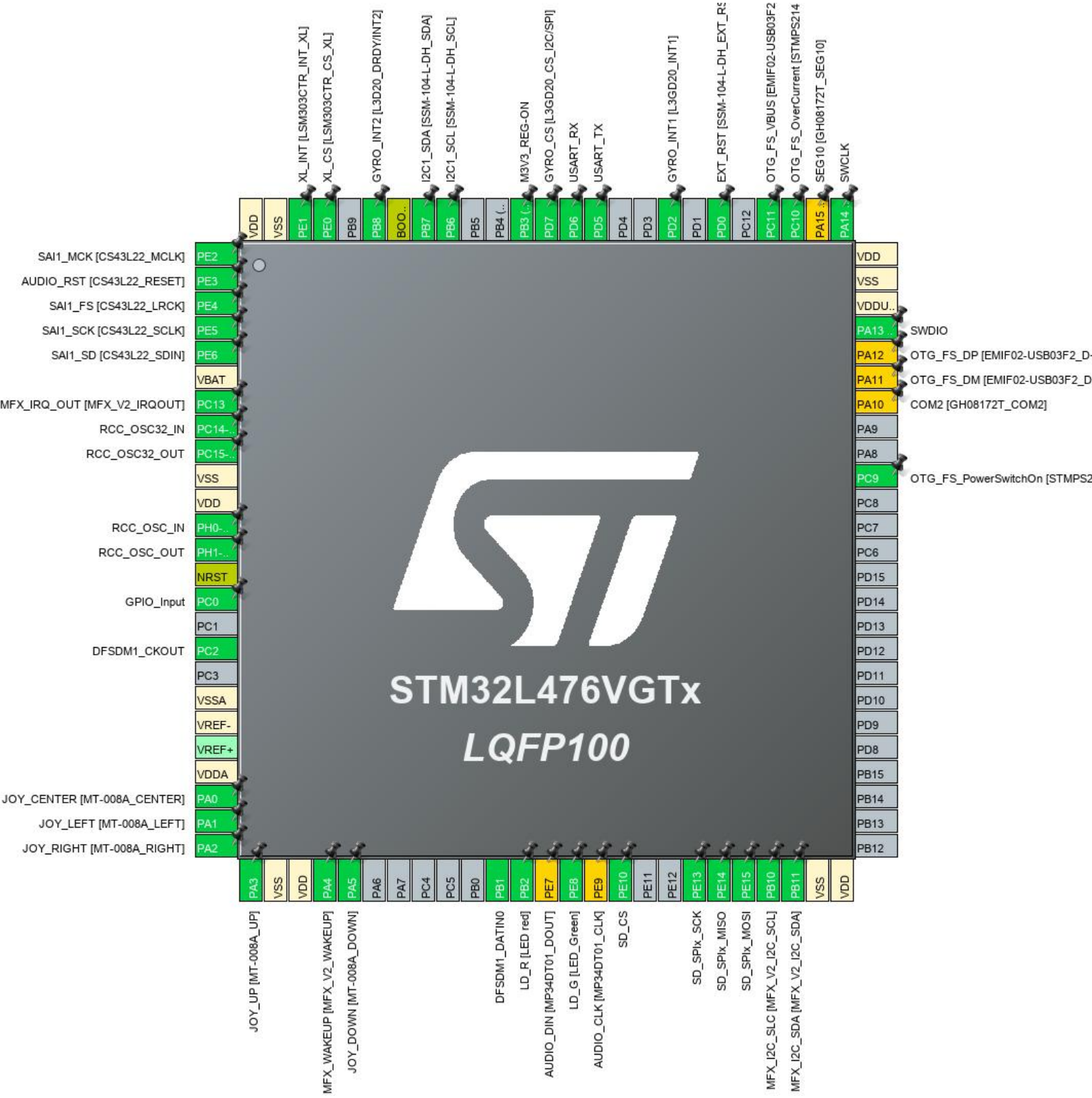
1.1. Project

Project Name	Disco_L476_DSP_SDCARD_v3
Board Name	STM32L476G-DISCO
Generated with:	STM32CubeMX 5.5.0
Date	03/05/2020

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SAI1_MCLK_A	SAI1_MCK [CS43L22_MCLK]
2	PE3 *	I/O	GPIO_Output	AUDIO_RST [CS43L22_RESET]
3	PE4	I/O	SAI1_FS_A	SAI1_FS [CS43L22_LRCK]
4	PE5	I/O	SAI1_SCK_A	SAI1_SCK [CS43L22_SCLK]
5	PE6	I/O	SAI1_SD_A	SAI1_SD [CS43L22_SDIN]
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	MFX_IRQ_OUT [MFX_V2_IRQOUT]
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Input	
17	PC2	I/O	DFSDM1_CKOUT	
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0 *	I/O	GPIO_Input	JOY_CENTER [MT-008A_CENTER]
24	PA1 *	I/O	GPIO_Input	JOY_LEFT [MT-008A_LEFT]
25	PA2 *	I/O	GPIO_Input	JOY_RIGHT [MT-008A_RIGHT]
26	PA3 *	I/O	GPIO_Input	JOY_UP [MT-008A_UP]
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	GPIO_EXTI4	MFX_WAKEUP [MFX_V2_WAKEUP]
30	PA5 *	I/O	GPIO_Input	JOY_DOWN [MT-008A_DOWN]
36	PB1	I/O	DFSDM1_DATIN0	

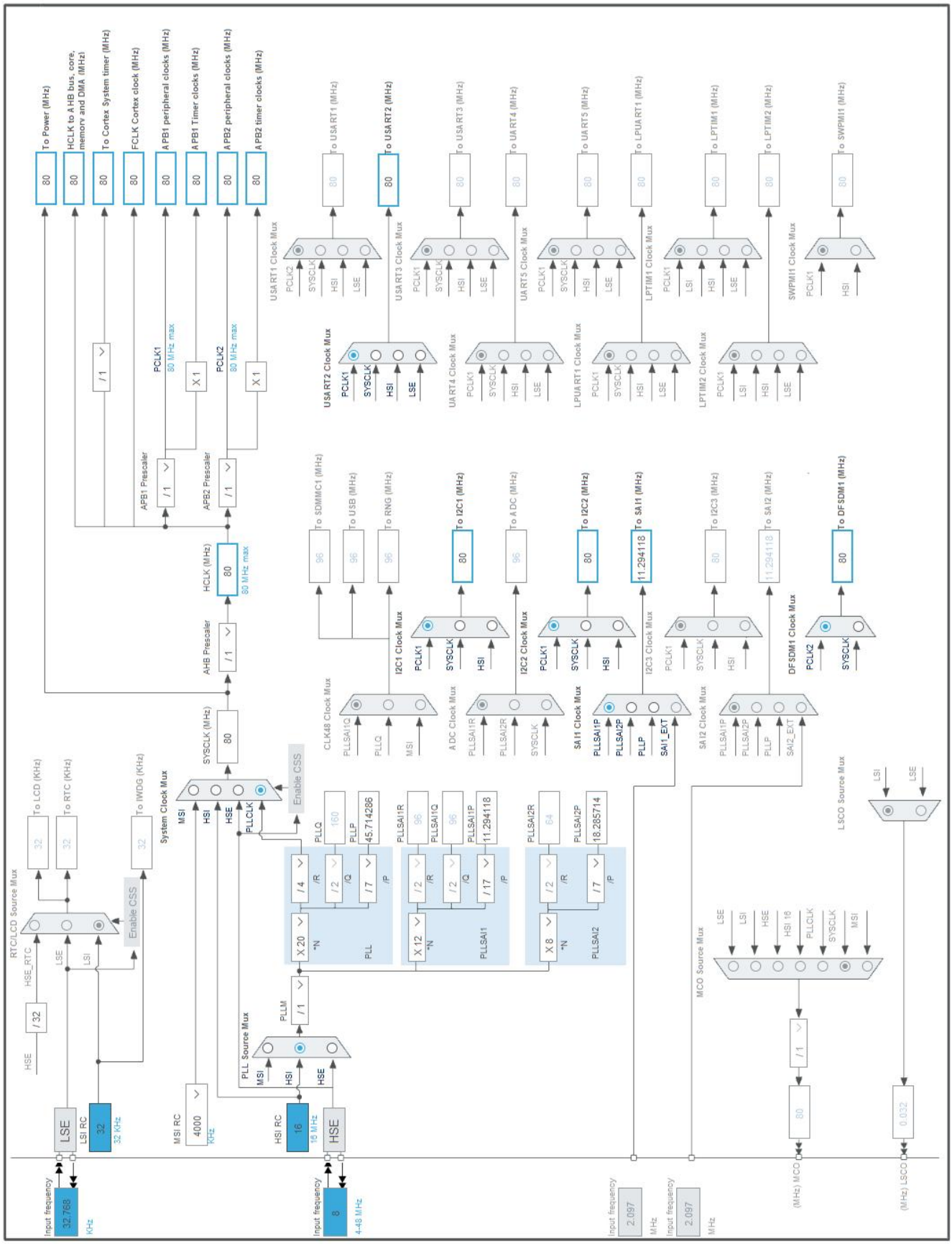
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PB2 *	I/O	GPIO_Output	LD_R [LED red]
38	PE7 **	I/O	SAI1_SD_B	AUDIO_DIN [MP34DT01_DOUT]
39	PE8 *	I/O	GPIO_Output	LD_G [LED_Green]
40	PE9 **	I/O	SAI1_FS_B	AUDIO_CLK [MP34DT01_CLK]
41	PE10 *	I/O	GPIO_Output	SD_CS
44	PE13	I/O	SPI1_SCK	SD_SPIx_SCK
45	PE14	I/O	SPI1_MISO	SD_SPIx_MISO
46	PE15	I/O	SPI1_MOSI	SD_SPIx_MOSI
47	PB10	I/O	I2C2_SCL	MFX_I2C_SLC [MFX_V2_I2C_SCL]
48	PB11	I/O	I2C2_SDA	MFX_I2C_SDA [MFX_V2_I2C_SDA]
49	VSS	Power		
50	VDD	Power		
66	PC9 *	I/O	GPIO_Output	OTG_FS_PowerSwitchOn [STMPS2141STR_EN]
69	PA10 **	I/O	LCD_COM2	COM2 [GH08172T_COM2]
70	PA11 **	I/O	USB_OTG_FS_DM	OTG_FS_DM [EMIF02-USB03F2_D-out]
71	PA12 **	I/O	USB_OTG_FS_DP	OTG_FS_DP [EMIF02-USB03F2_D+out]
72	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	SWDIO
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	SWCLK
77	PA15 (JTDI) **	I/O	LCD_SEG17	SEG10 [GH08172T_SEG10]
78	PC10	I/O	GPIO_EXTI10	OTG_FS_OverCurrent [STMPS2141STR_FAULT]
79	PC11 *	I/O	GPIO_Output	OTG_FS_VBUS [EMIF02-USB03F2_Vbus]
81	PD0	I/O	GPIO_EXTI0	EXT_RST [SSM-104-L-DH_EXT_RST]
83	PD2	I/O	GPIO_EXTI2	GYRO_INT1 [L3GD20_INT1]
86	PD5	I/O	USART2_TX	USART_TX
87	PD6	I/O	USART2_RX	USART_RX
88	PD7 *	I/O	GPIO_Output	GYRO_CS [L3GD20_CS_I2C/SPI]
89	PB3 (JTDO-TRACESWO) *	I/O	GPIO_Output	M3V3_REG-ON

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
92	PB6	I/O	I2C1_SCL	I2C1_SCL [SSM-104-L-DH_SCL]
93	PB7	I/O	I2C1_SDA	I2C1_SDA [SSM-104-L-DH_SDA]
94	BOOT0	Boot		
95	PB8	I/O	GPIO_EXTI8	GYRO_INT2 [L3D20_DRDY/INT2]
97	PE0 *	I/O	GPIO_Output	XL_CS [LSM303CTR_CS_XL]
98	PE1	I/O	GPIO_EXTI1	XL_INT [LSM303CTR_INT_XL]
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Disco_L476_DSP_SDCARD_v3
Project Folder	C:\Users\toussaij\Documents\STM32dev\Disco_L476_DSP_SDCARD_v3
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476VGTx
Datasheet	025976_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. DFSDM1

mode: PDM/SPI input from ch0 and internal clock

7.1.1. Filter 0:

regular channel selection:

regular channel selection	**Channel 0 ***
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	Disable
Dma Mode	Disable

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

Filter parameters:

Sinc Order	FastSinc filter type
Fosr	1
Iosr	1

7.1.2. Filter 1:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.1.3. Filter 2:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.1.4. Filter 3:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.1.5. Output Clock:

Output Clock parameters:

Selection	Source for ouput clock is system clock
Divider	2

7.1.6. Channel 0:

Channel 0 parameters:

Type	SPI with rising edge

Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	**0x00 ***

Analog watchdog parameters:

Filter Order	FastSinc filter type
Oversampling	1

7.2. GPIO

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.6. SAI1

Mode: Master with Master Clock Out

7.6.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous

Basic Parameters

Protocol	Free
Audio Mode	Master Transmit
Frame Length	**32 bits ***
Data Size	**16 Bits ***
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	**16 ***
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	**Before First Bit ***
Slot Parameters	
First Bit Offset	0
Number of Slots	**2 ***
Slot Active Final Value	**0x0000FFFF ***
Slot Active	**All ***
Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	**44.1 KHz ***
Real Audio Frequency	**44.117 KHz ***
Error between Selected	**0.26 % ***
Clock Strobing	Falling Edge
Advanced Parameters	
Fifo Threshold	**One Quarter Full ***
Output Drive	**Enabled ***

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**20.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.9. USART2

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DFSDM1	PC2	DFSDM1_CKOUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	DFSDM1_DATIN0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	I2C1_SCL [SSM-104-L-DH_SCL]
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	I2C1_SDA [SSM-104-L-DH_SDA]
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	MFX_I2C_SLC [MFX_V2_I2C_SCL]
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	MFX_I2C_SDA [MFX_V2_I2C_SDA]
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SAI1	PE2	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_MCK [CS43L22_MCLK]
	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_FS [CS43L22_LRCK]
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_SCK [CS43L22_SCLK]
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_SD [CS43L22_SDIN]
SPI1	PE13	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_SPIx_SCK
	PE14	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_SPIx_MISO

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE15	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_SPIx_MOSI
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
USART2	PD5	USART2_TX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	USART_TX
	PD6	USART2_RX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	USART_RX
Single Mapped Signals	PE7	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AUDIO_DIN [MP34DT01_DOUT]
	PE9	SAI1_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	AUDIO_CLK [MP34DT01_CLK]
	PA10	LCD_COM2	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM2 [GH08172T_COM2]
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OTG_FS_DM [EMIF02-USB03F2_D-out]
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OTG_FS_DP [EMIF02-USB03F2_D+out]
	PA15 (JTDI)	LCD_SEG17	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG10 [GH08172T_SEG10]
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	AUDIO_RST [CS43L22_RESET]
	PC13	GPIO_EXTI13	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	**n/a**	MFX_IRQ_OUT [MFX_V2_IRQOUT]
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	
	PA0	GPIO_Input	Input mode	**Pull-down ***	**n/a**	JOY_CENTER [MT-008A_CENTER]
	PA1	GPIO_Input	Input mode	**Pull-down ***	**n/a**	JOY_LEFT [MT-008A_LEFT]
	PA2	GPIO_Input	Input mode	**Pull-down ***	**n/a**	JOY_RIGHT [MT-008A_RIGHT]
	PA3	GPIO_Input	Input mode	**Pull-down ***	**n/a**	JOY_UP [MT-008A_UP]
	PA4	GPIO_EXTI4	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	**n/a**	MFX_WAKEUP [MFX_V2_WAKEUP]
	PA5	GPIO_Input	Input mode	**Pull-down ***	**n/a**	JOY_DOWN [MT-008A_DOWN]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB2	GPIO_Output	Output Push Pull	**Pull-up ***	**Very High ***	LD_R [LED red]
	PE8	GPIO_Output	Output Push Pull	**Pull-up ***	**Very High ***	LD_G [LED_Green]
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CS
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_PowerSwitchOn [STMPS2141STR_EN]
	PC10	GPIO_EXTI10	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	OTG_FS_OverCurrent [STMPS2141STR_FAULT]
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_VBUS [EMIF02-USB03F2_Vbus]
	PD0	GPIO_EXTI0	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	EXT_RST [SSM-104-L-DH_EXT_RST]
	PD2	GPIO_EXTI2	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	GYRO_INT1 [L3GD20_INT1]
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	GYRO_CS [L3GD20_CS_I2C/SPI]
	PB3 (JTDO-TRACESWO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	M3V3_REG-ON
	PB8	GPIO_EXTI8	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	GYRO_INT2 [L3D20_DRDY/INT2]
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	XL_CS [LSM303CTR_CS_XL]
	PE1	GPIO_EXTI1	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	XL_INT [LSM303CTR_INT_XL]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SAI1_A	DMA2_Channel1	Memory To Peripheral	**Very High ***

SAI1_A: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 channel1 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
DFSDM1 filter0 global interrupt	unused		
SAI1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report