



1. Description

1.1. Project

Project Name	Nucleo_WB_IC_PWM_v1
Board Name	P-NUCLEO-WB55-Nucleo
Generated with:	STM32CubeMX 6.3.0
Date	01/30/2022

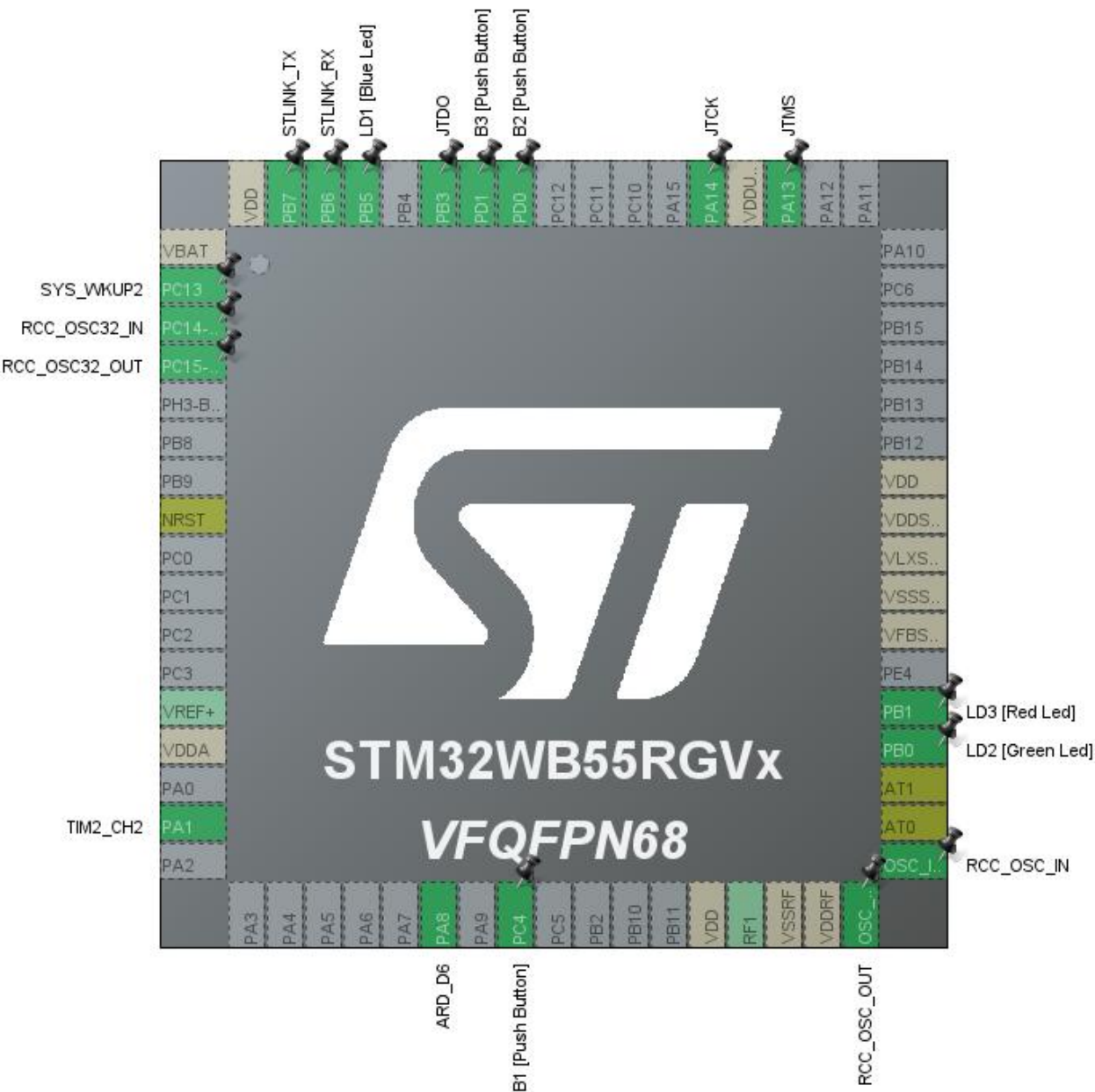
1.2. MCU

MCU Series	STM32WB
MCU Line	STM32WBx5
MCU name	STM32WB55RGVx
MCU Package	VFQFPN68
MCU Pin number	68

1.3. Core(s) information

Core(s)	ARM Cortex-M4
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2. Pinout Configuration

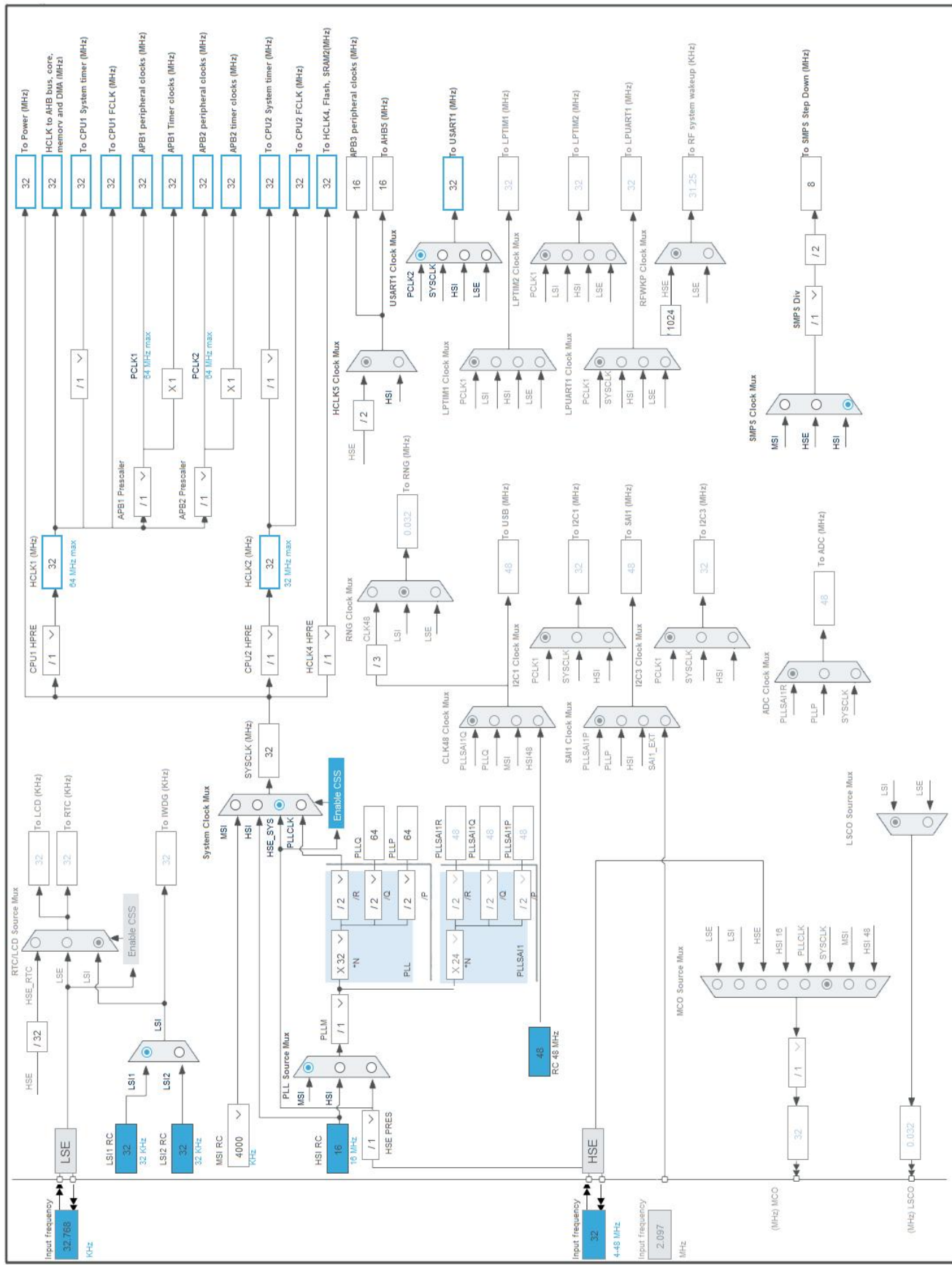


3. Pins Configuration

Pin Number VFQFPN68	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	SYS_WKUP2	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
8	NRST	Reset		
14	VDDA	Power		
16	PA1	I/O	TIM2_CH2	
23	PA8	I/O	TIM1_CH1	ARD_D6
25	PC4 *	I/O	GPIO_Input	B1 [Push Button]
30	VDD	Power		
32	VSSRF	Power		
33	VDDRF	Power		
34	OSC_OUT	MonolO	RCC_OSC_OUT	
35	OSC_IN	MonolO	RCC_OSC_IN	
36	AT0	NC		
37	AT1	NC		
38	PB0 *	I/O	GPIO_Output	LD2 [Green Led]
39	PB1 *	I/O	GPIO_Output	LD3 [Red Led]
41	VFBSMPS	Power		
42	VSSSMPS	Power		
43	VLXSMPS	Power		
44	VDDSMPS	Power		
45	VDD	Power		
54	PA13	I/O	SYS_JTMS-SWDIO	JTMS
55	VDDUSB	Power		
56	PA14	I/O	SYS_JTCK-SWCLK	JTCK
61	PD0 *	I/O	GPIO_Input	B2 [Push Button]
62	PD1 *	I/O	GPIO_Input	B3 [Push Button]
63	PB3	I/O	SYS_JTDO-SWO	JTDO
65	PB5 *	I/O	GPIO_Output	LD1 [Blue Led]
66	PB6	I/O	USART1_TX	STLINK_RX
67	PB7	I/O	USART1_RX	STLINK_TX
68	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Nucleo_WB_IC_PWM_v1
Project Folder	C:\Users\toussaij\Documents\STM32dev\Nucleo_WB_IC_PWM_v1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_WB V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM2_Init	TIM2
4	MX_USART1_UART_Init	USART1
5	MX_TIM1_Init	TIM1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32WB
Line	STM32WBx5
MCU	STM32WB55RGVx
Datasheet	DS11929_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

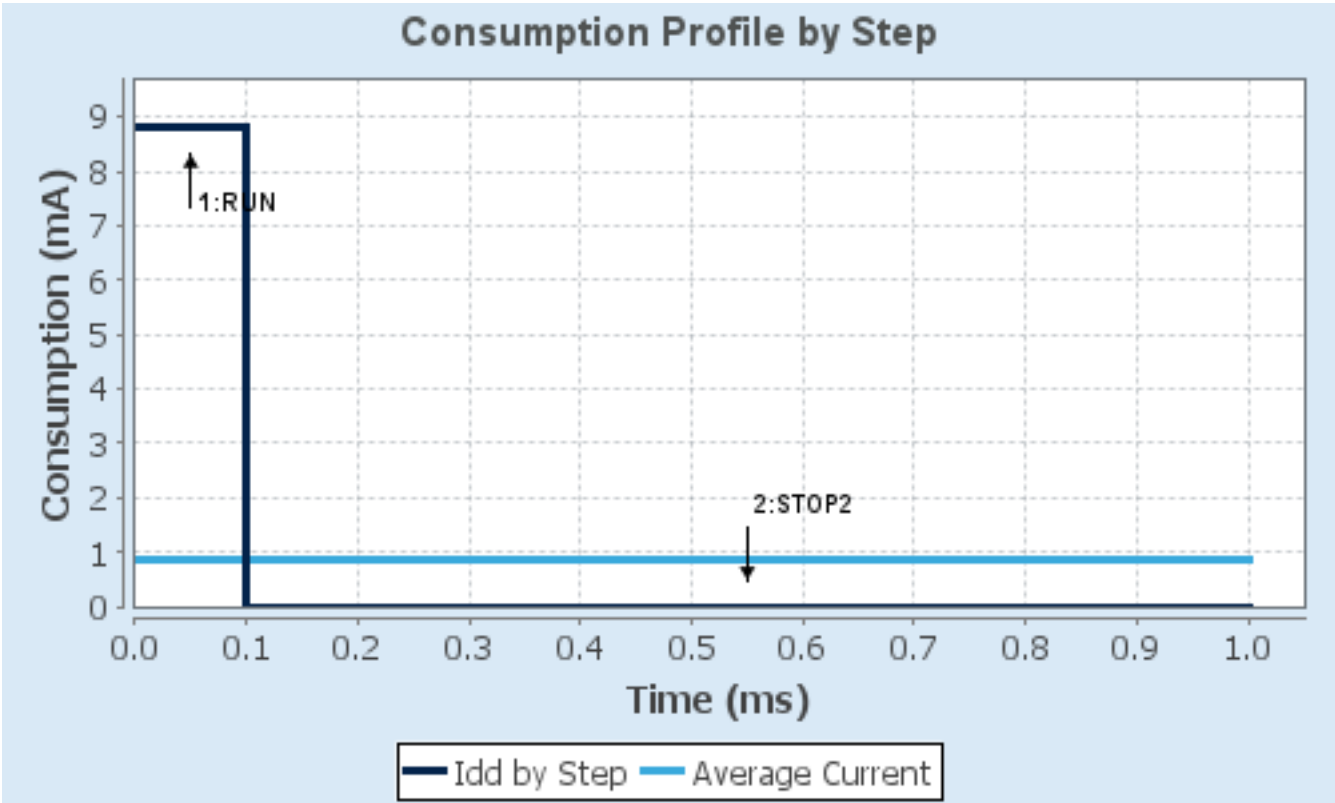
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM1/Flash-PowerDown	FLASH/ART/CACHE
CPU Frequency	64 MHz	0 Hz
Clock Configuration	HSI PLL Regulator_ON	ALL CLOCKS OFF Regulator_ON
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.8 mA	1.85 μ A
Duration	0.1 ms	0.9 ms
DMIPS	80.0	0.0
Ta Max	103.76	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	881.66 μ A
Battery Life	5 months, 7 days, 21 hours	Average DMIPS	8.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
MSI State	Enabled
HSI State	Enabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE
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7.2. SYS

Debug: Trace Asynchronous Sw

mode: System Wake-Up 2

Timebase Source: SysTick

7.3. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1249 *
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Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1279 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	639 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.4. TIM2

Clock Source : Internal Clock

Channel2: Input Capture direct mode

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0xffffffff
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SYS	PC13	SYS_WKUP2	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	JTMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	JTCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	JTDO
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D6
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull-up *	Low	STLINK_RX
	PB7	USART1_RX	Alternate Function Push Pull	Pull-up *	Low	STLINK_TX
GPIO	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Push Button]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red Led]
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B2 [Push Button]
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B3 [Push Button]
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Blue Led]

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM2 global interrupt	true	0	0
PVD/PVM0/PVM2 interrupts through EXTI lines 16/31/33	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CPU2 SEV interrupt through EXTI line 40 and PWR CPU2 HOLD wake-up interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
USART1 global interrupt	unused		
PWR switching on the fly, end of BLE activity, end of 802.15.4 activity, end of critical radio phase interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM2 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware							
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Utilities
DMA		TIM1 ✓	USART1 ✓				
GPIO ✓		TIM2 ✓					
NVIC ✓							
RCC ✓							
SYS ✓							

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00344191.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00318631.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00716581.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00383256.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00311483.pdf

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Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00403796.pdf

Application note http://www.st.com/resource/en/application_note/DM00429003.pdf

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Application note http://www.st.com/resource/en/application_note/DM00492814.pdf

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