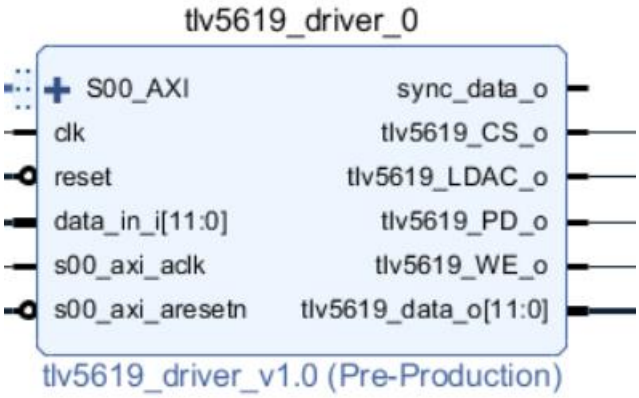
TLV5619_driver



NAME	DIRECTION	DESCRIPTION
S00_AXI BUS	in	Slave AXI 4 lite Interface
S00_AXI_ACLK	in	AXI clk
S00_AXIARESETN	in	AXI reset
CLK	in	CLK
RESET	in	Reset
DATA_IN_I[11:0]	in	Input data
SYNC_DATA_O	out	2 clk cycles previous prefetch for data_in
TLV5619_CS_O	out	Chip select
TLV5619_LDAC_O	out	Load DAC
TLV5619_PD_O	out	Low Consuption mode
TLV5619_WE_O	out	Write enable
TLV5619_DATA_O [11:0]	out	DAC data

The TLV5619_driver creates an interface between AXI 4 Lite and a Tlv5619 Texas Intruments DAC.

It has two modes of function

- **BRAM**: An internal 12bits x 64 Kbit memory can store up to 65536 data points inside and then load them into the DAC at a rate of 10 MHz
- **External**: The data loaded into the DAC is given by data_in_i, an auxiliary ignal sync_data generates a prefetch signal to provide the data.

The configuation of the IP is made via 4 registers:

POSITION	SIZE (BITS)	NAME	DESCRIPTION
0	2	dac_mode_reg_i	Mode 0: Disabled Mode 1: BRAM Mode 2: External
1	16	dac_period_reg_i	Period of repetition when working in BRAM mode
2	12	dac_data_in_reg_i	Data to be stored in the BRAM
3	2	dac_write_ena_reg_i	Enable Writing to the BRAM
4	16	dac_addr_reg_i	BRAM Address