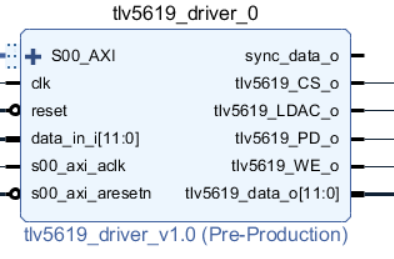
**TLV5619\_driver**



|  |  |  |
| --- | --- | --- |
| Name | Direction | Description |
| S00\_AXI BUS | in | Slave AXI 4 lite Interface |
| s00\_axi\_aclk | in | AXI clk |
| s00\_axiaresetn | in | AXI reset |
| clk | in | CLK |
| reset | in | Reset |
| data\_in\_i[11:0] | in | Input data |
| sync\_data\_o | out | 2 clk cycles previous prefetch for data\_in |
| Tlv5619\_CS\_o | out | Chip select |
| Tlv5619\_LDAC\_o | out | Load DAC |
| Tlv5619\_PD\_o | out | Low Consuption mode |
| Tlv5619\_WE\_o | out | Write enable |
| Tlv5619\_data\_o [11:0] | out | DAC data |

The TLV5619\_driver creates an interface between AXI 4 Lite and a Tlv5619 Texas Intruments DAC.

It has two modes of function

* **BRAM**: An internal 12bits x 64 Kbit memory can store up to 65536 data points inside and then load them into the DAC at a rate of 10 MHz
* **External**: The data loaded into the DAC is given by data\_in\_i, an auxiliary ignal sync\_data generates a prefetch signal to provide the data.

The configuation of the IP is made via 4 registers:

|  |  |  |  |
| --- | --- | --- | --- |
| Position | Size (bits) | Name | Description |
| 0 | 2 | dac\_mode\_reg\_i | Mode 0: Disabled  Mode 1: BRAM  Mode 2: External |
| 1 | 16 | dac\_period\_reg\_i | Period of repetition when working in BRAM mode |
| 2 | 12 | dac\_data\_in\_reg\_i | Data to be stored in the BRAM |
| 3 | 2 | dac\_write\_ena\_reg\_i | Enable Writing to the BRAM |
| 4 | 16 | dac\_addr\_reg\_i | BRAM Address |