DEPARTMENT OF COMPUTER SCIENCE

COLORADO SCHOOL OF MINES
EARTH • ENERGY • ENVIRONMENT

CSCI 341: Computer Organization
WS 12: Data Hazards and Control Hazards

1	Name one difference between forwarding and hazard detection.
2	What are the conditionals for an EX and MEM hazard that the forwarding unit has to implement?
3	What is a control hazard? Why do they arise? Why does the single cycle processor not have control hazards?

4 How many instructions are run before a branch decision is made with the original pipeline architecture? Why is this important?

5 List the three strategies used to reduce the amount of instructions run before a branch decision is made.

6 An assembler may change the following assembly to produce the optimized code shown below.

Original	**Optimized**

`addi t0, zero, zero`
`addi t1, zero, 10`
`forLoop:`
`  … code …`
`  addi t0, t0, 1`
`  lw t2, 0(s1)`
`  bne t0, t1, forLoop`
	`addi t0, zero, zero`
	`addi t1, zero, 10`
	`forLoop:`
	`  … code …`
	`  addi t0, t0, 1`
	`  bne t0, t1, forLoop`
	`lw t2, 0(s1)`

Why does this work for pipelined processors? Will this work for a single cycle processor? What is this an example of?

7	Explain how dynamic branch prediction works. Why does it work?
8	Will increasing the number of bits in a branch predictor eventually result in 100% accuracy?