DEPARTMENT OF
COMPUTER SCIENCE

COLORADO SCHOOL OF MINES
EARTH • ENERGY • ENVIRONMENT

CSCI 341: Computer Organization
WS 13: Pipelined Datapath and Control

1	Why must the clock cycle for a computer be determined by the longest instruction? Why can’t variable length cycles be used? Solution: Every instruction must be able to be completed in the time that it is allotted. Having a machine that varies its clock cycle based on the instruction running would be too complex to feasibly build. Also, as discussed later, this would not work for a pipelined datapath as multiple instructions are running at once.
2	Explain the concept of pipelining. This is an important concept so be through in your explanation. Solution: There are multiple instructions running at once, with a new instruction starting with every clock cycle. This allows for a greater throughput rather than a direct increase in speed of the hardware, even though equivalent programs will run faster on a pipelined datapath than a non-pipelined datapath.
3	How many clock cycles are there per instruction in a RISC-V pipelined processor? Solution: There will be as many clock cycles as there are stages in the pipelined datapath. For RISC-V, this means 5 clock cycles.
4	Is every functional unit used by every instruction? Solution: No.
5	For instructions that need to update a register, how does the register that needs to be updated get passed through the pipeline? Solution: Pipeline registers between each stage of the pipeline.
6	List the three hazards possible on a pipelined datapath as well as why they occur.

Solution:

1. Structural: attempt to use the same resource in two different ways at the same time
2. Control: attempt to make a decision before condition is evaluated
3. Data: attempt to use item before it is ready

7 By introducing pipelining there can no longer just be one set of control signals. How does the RISC-V pipelined processor solve this problem?

Solution:
There are additional registers in each of the pipeline register files that pass through the appropriate control signals for the current instruction at each stage.

8 List the control registers at each stage in the pipeline.

Solution:
ID/EX: WB(2 registers),M(3 registers),EX(2 registers)
EX/MEM: WB(2 registers),M(3 registers)
MEM/WB: WB(2 registers)

9 What problem does data forwarding solve?

Solution:
It solves problems that arise when successive instructions write and then read from the same register. Without forwarding, instructions right after the first instruction that writes to the register will get the wrong value. With forwarding, the value calculated from the ALU can be sent to other stages of the pipeline, removing the need to stall the pipeline.

10 Which instructions will either need forwarding or create a hazard?

```
add t0, t0, t0
add t1, t1, t0
add t0, t1, t2
sw t1, 0(s0)
```

Solution:
t0 in instructions 1 and 2
t1 in instructions 2 and 3
t0 in instructions 1 and 3 assuming that no nops are inserted before instruction 2
t1 in instructions 2 and 4 assuming that no nops are inserted before instruction 3