

CSCI 341: Computer Organization
WS 5: Bitwise Instructions

1	<p>How would you bit mask the bottom half of a word? That is, how would you set the top half of a word to 0 using logical operators only?</p> <p>Solution: without pseudo/enhanced instructions, only 12 bit immediates</p> <pre>addi t0, zero, 0xFF # t0 = 0xFF slli t0, t0, 8 # t0 = 0xFF00 ori t0, t0, 0xFF # t0 = 0xFFFF and s0, s0, t0</pre>															
2	<p>The NOR operation does not exist in RISC-V. How would you do this in RISC-V? Here is its truth table:</p> <table><tr><td>A</td><td>B</td><td>A NOR B</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> <p>Assuming values are in t0 and t1, result in t0:</p> <pre>or t0, t0, t1 xori t0, t0, -1</pre>	A	B	A NOR B	0	0	1	0	1	0	1	0	0	1	1	0
A	B	A NOR B														
0	0	1														
0	1	0														
1	0	0														
1	1	0														
3	<p>Assume that x (using s0) and y (using s1) are both ints. Recall that bits are numbered from right to left in a word starting with bit 0.</p> <p>Write two lines of RISC-V code to set x to the value contained in bits 15 to 10 of y. That is, x has y's bits 15 to 10 as its bits 5 to 0, and 0's in all other bits.</p> <p>Shift and mask solution:</p> <pre>srli s0, s1, 10 # x = y>>10 andi s0,s0,0x3F # x=x&0x3F (= (y>>10) &0x3F)</pre> <p>Two shift solution:</p> <pre>slli s0,s1,16 # x = y <<16 srli s0, s0, 26 # x = x >> 26 (= (y<<16) >>26)</pre>															

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Set s1 to hold the value 0xAACCBDD

End up with the value 0x00AACC00 in s0, using only logical operations to erase bits and move bits around, and print it out as a hexadecimal.

Make it so that it creates a value from s1 that is the upper two bytes of s1 as the middle two bytes of s0 no matter what the starting value is.

```
lui s1, 0xAACCC
addi s1, s1, 0xFFFFBDD
srli s0, s1, 16
slli s0, s0, 8
```

```
addi a7, zero, 34
add a0, zero, s0
ecall
addi a7, zero, 11
addi a0, zero, 10
ecall
```

```
lui s1, 0xAACCC
addi s1, s1, 0xFFFFBDD
lui t0, 0xFFFF0
and s0, s1, t0
srli s0, s0, 8
```

```
addi a7, zero, 34
add a0, zero, s0
ecall
```