DEPARTMENT OF COMPUTER SCIENCE

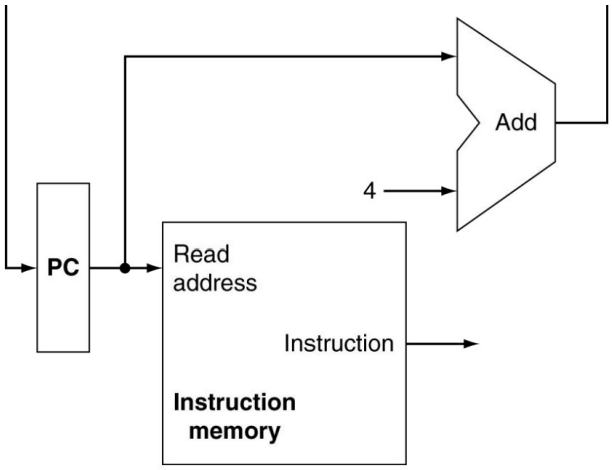
COLORADOSCHOOLOFMINES
EARTH • ENERGY • ENVIRONMENT

CSCI 341: Computer Organization
WS 11: Single Cycle Data Path

1	What two types of functional units are present in a data path? What defines when a state can change or not in a data path? Solution: Combinational and state elements. The rising clock edge triggers data write, any other time and writing is not allowed.

2	What assembly instruction is represented by the following lines of register transfer language?
	`1. R[rd]<-R[rs1]+R[rs2]`
	`2. R[rd]<-MEM[R[rs1]+SignExtImm]`
	
	Solution:
	1. add rd, rs1, rs2
	2. lw rd, Imm(rs1)

3	Why does the register file need both a Write Register and Write Data input? Solution: The register needs to know both where to write the data and what data to write.
4	Draw the datapath for the instruction fetch stage. Solution:



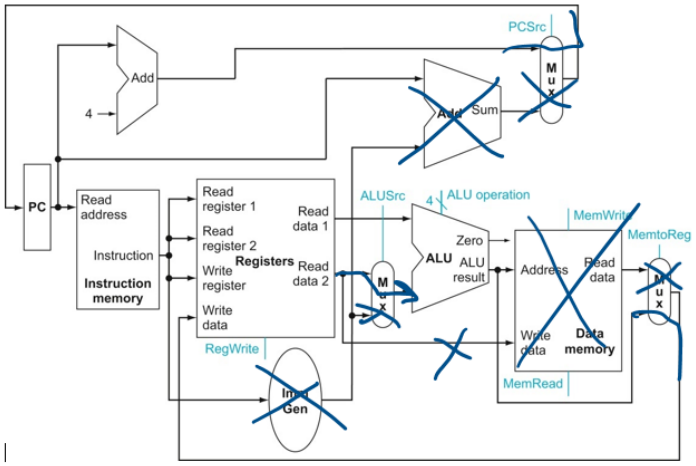
5 What are the five stages in the pipeline, in order?

Solution:

1. Fetch, Update PC
2. Decode
3. Execute
4. Memory
5. Write Back

6 Draw a picture showing the datapath (with all functional units that are used) for `add t2, t1, t0`
Explain what is happening in each functional unit.

Solution:



(a picture without the X'd out elements shows what is used by the add)

	PC is passed to adder (+4) to be updated to next instruction address. PC is also passed to Instruction Memory to locate the add instruction. Registers gets the read and write register inputs, and puts the two read registers (t1 and t0) on the outputs to go to the ALU. It has the write register as t2. The ALU adds the two values, and puts it on its output, which comes around to be the value to write to the write register, which is the final action taken here.