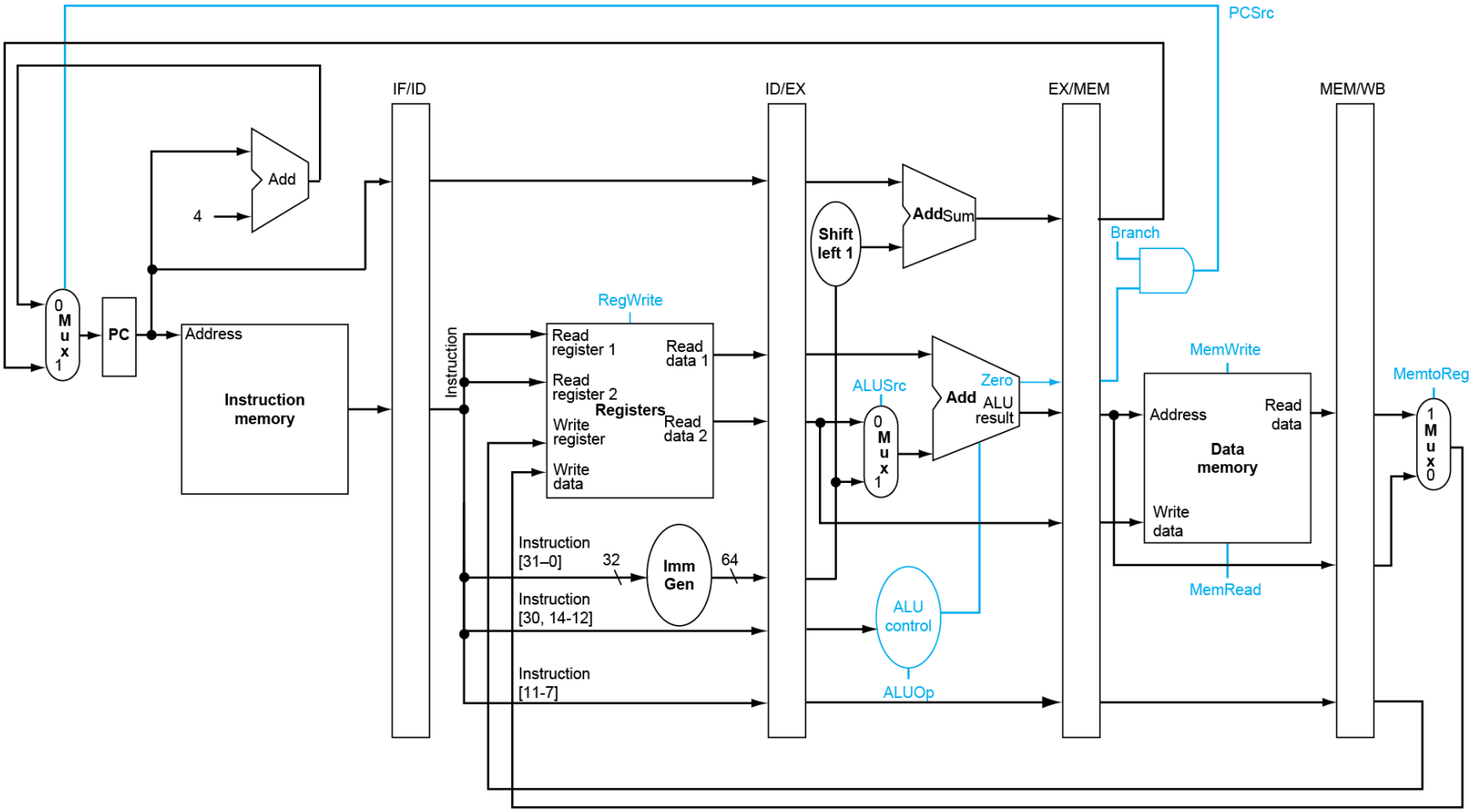
Pipelined Datapath Control



Observations

- **No write control for all pipeline registers and PC**
  - they are updated at every clock cycle.
- **To specify the control for the pipeline**
  - set the control values during each pipeline stage.
- **Control lines can be divided into 5 groups:**
  - IF – NONE
  - ID – NONE
  - EXE – ALUOp, ALUSrc
  - MEM – Branch, MemRead, MemWrite
  - WB – MemtoReg, RegWrite

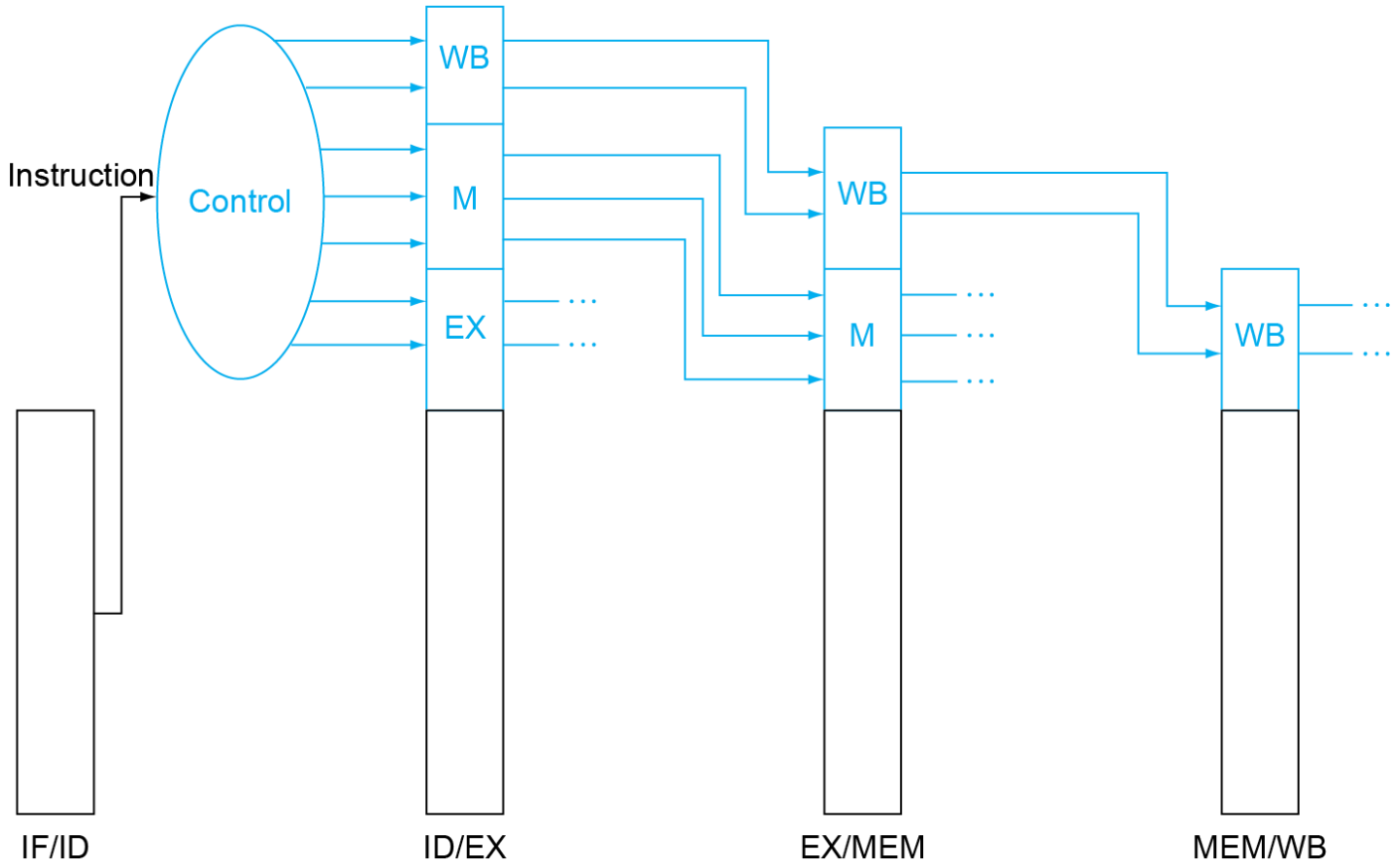
Control for Pipelined Datapath

Instruction	Execution/address calculation stage control lines		Memory access stage control lines			Write-back stage control lines	
	ALUOp	ALUSrc	Branch	Mem-Read	Mem-Write	Reg-Write	Memto-Reg
R-format	10	0	0	0	0	1	0
lw	00	1	0	1	0	1	1
sw	00	1	0	0	1	0	X
beq	01	0	1	0	0	0	X

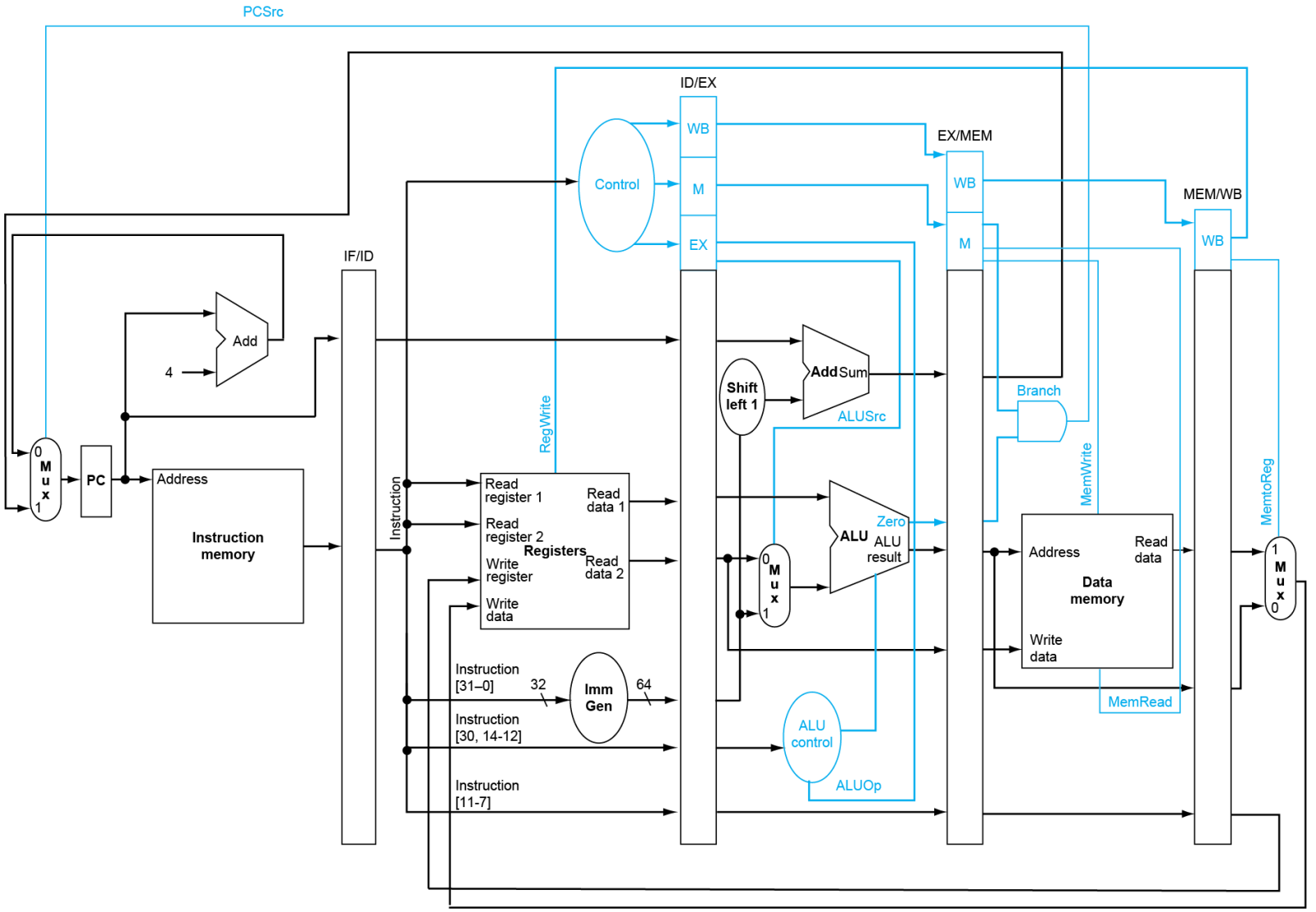
- **Control signals are generated at ID stage, how to pass them to other stages?**

Pass Control Signals

- **Extend the pipeline registers to include control information**



The Complete Pipelined Datapath

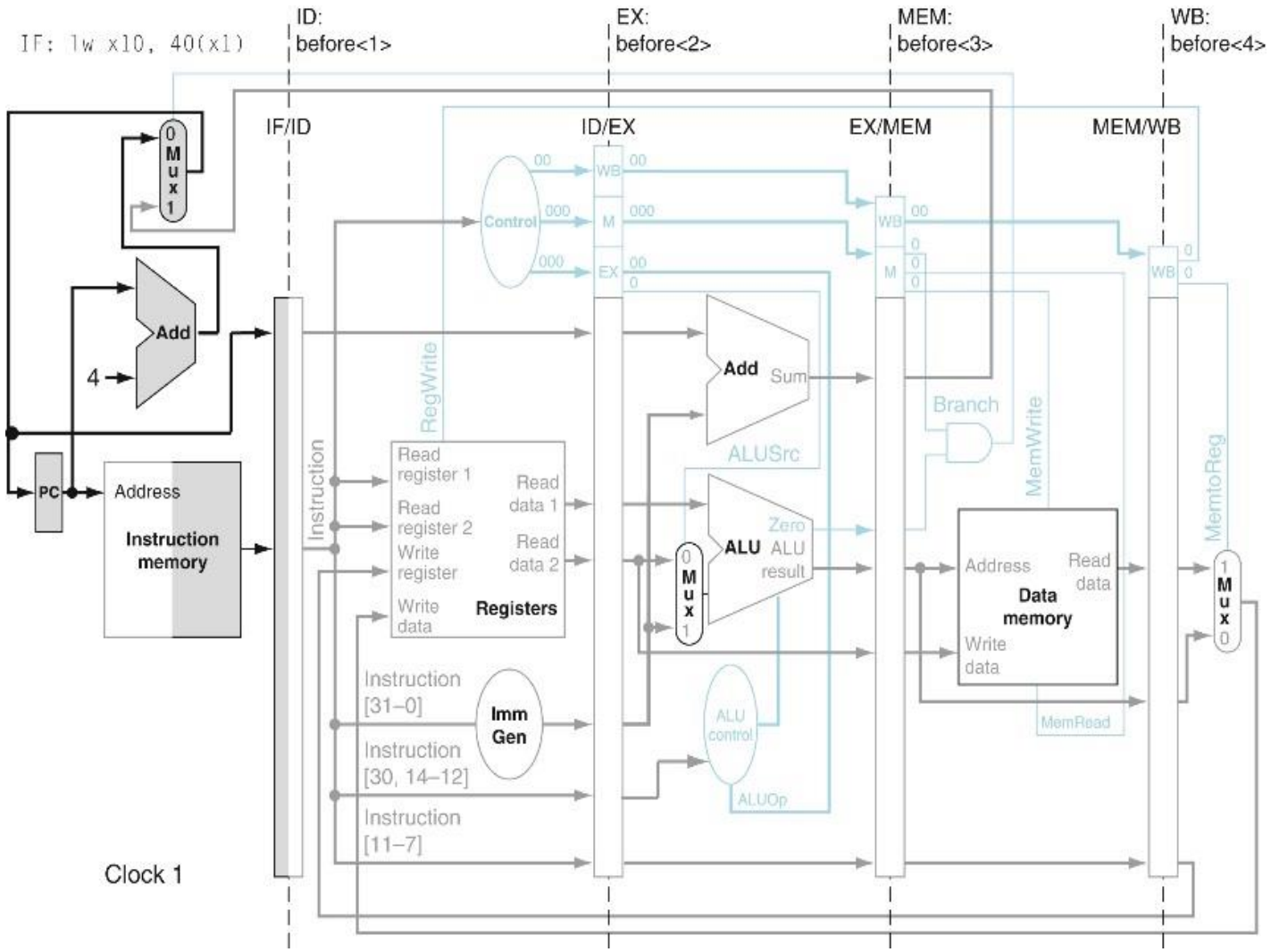


Example Pipeline Execution

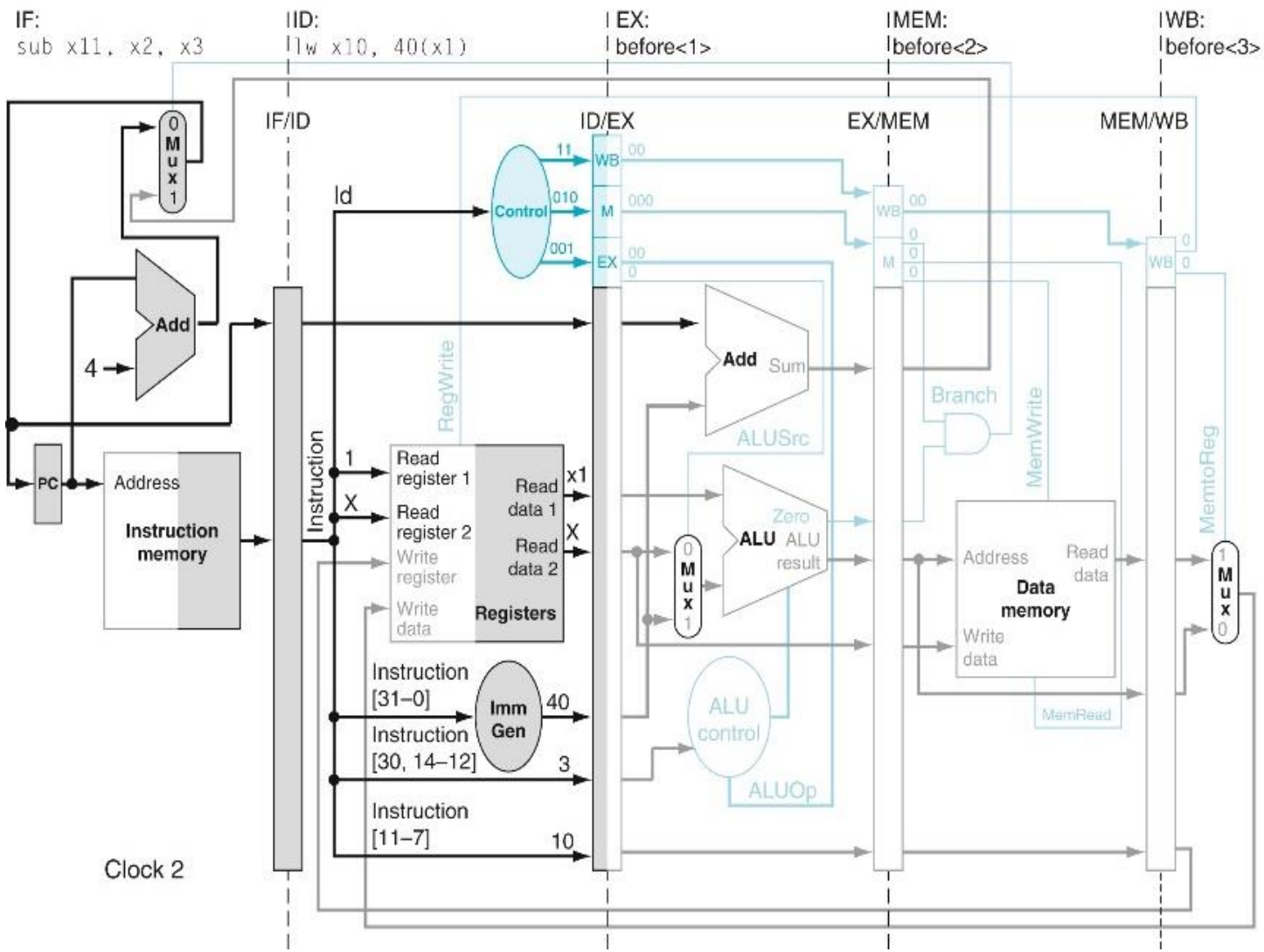
Note our instructions are independent of each other (no data hazards)

```
lw  x10, 40(x1)
sub x11, x2, x3
and x12, x4, x5
or  x13, x6, x7
add x14, x8, x9
```

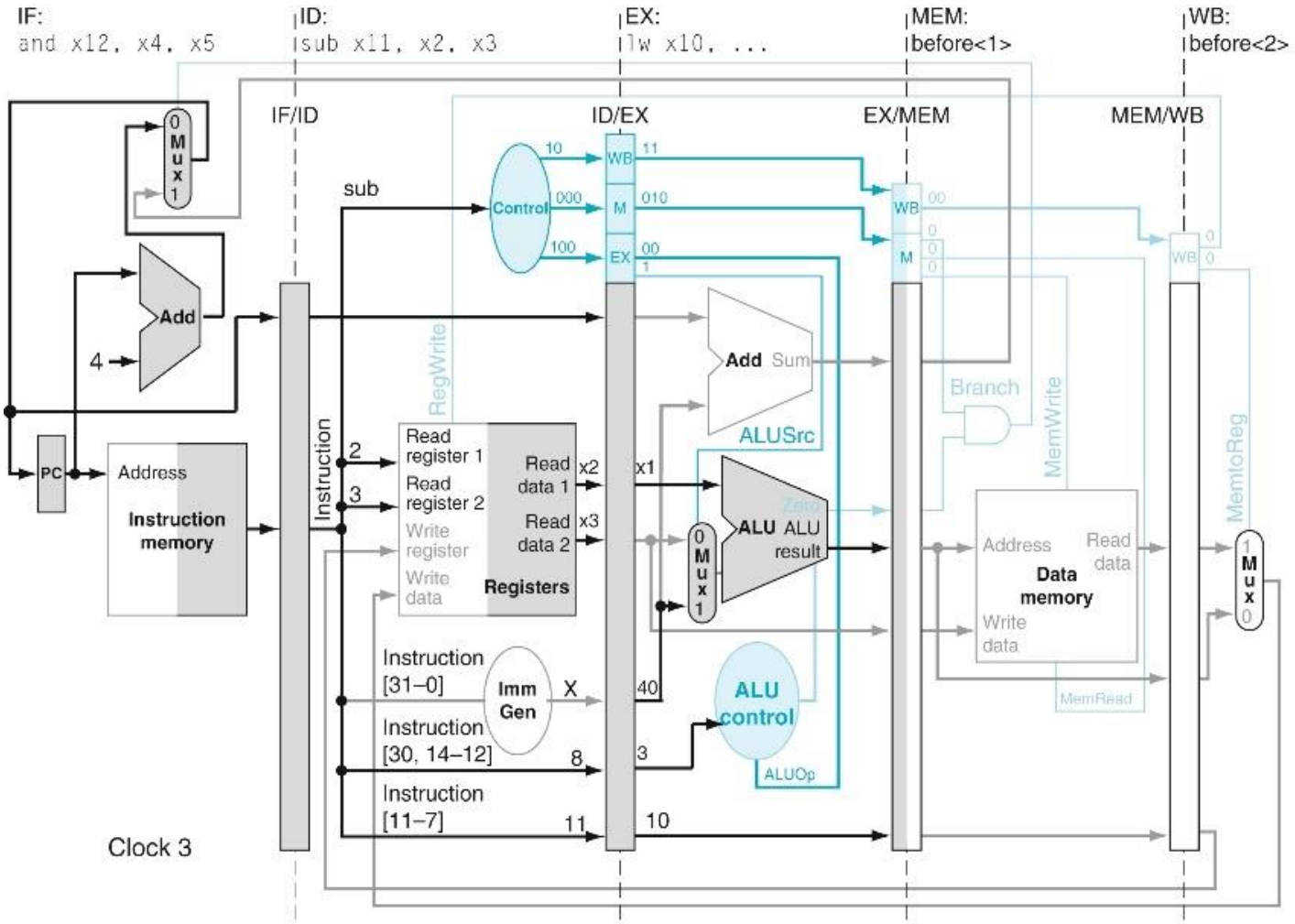
Clock Cycle 1



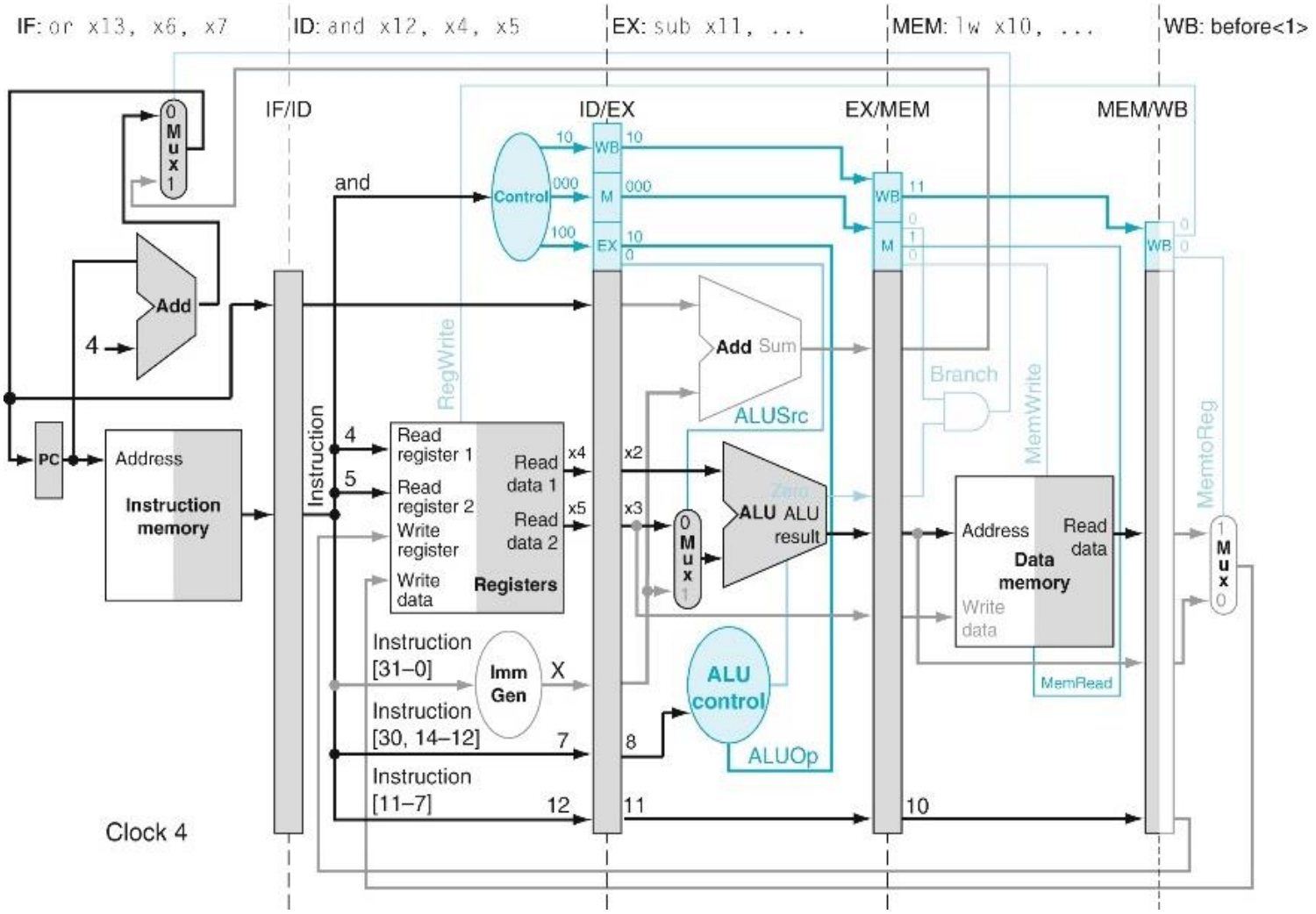
Clock Cycle 2



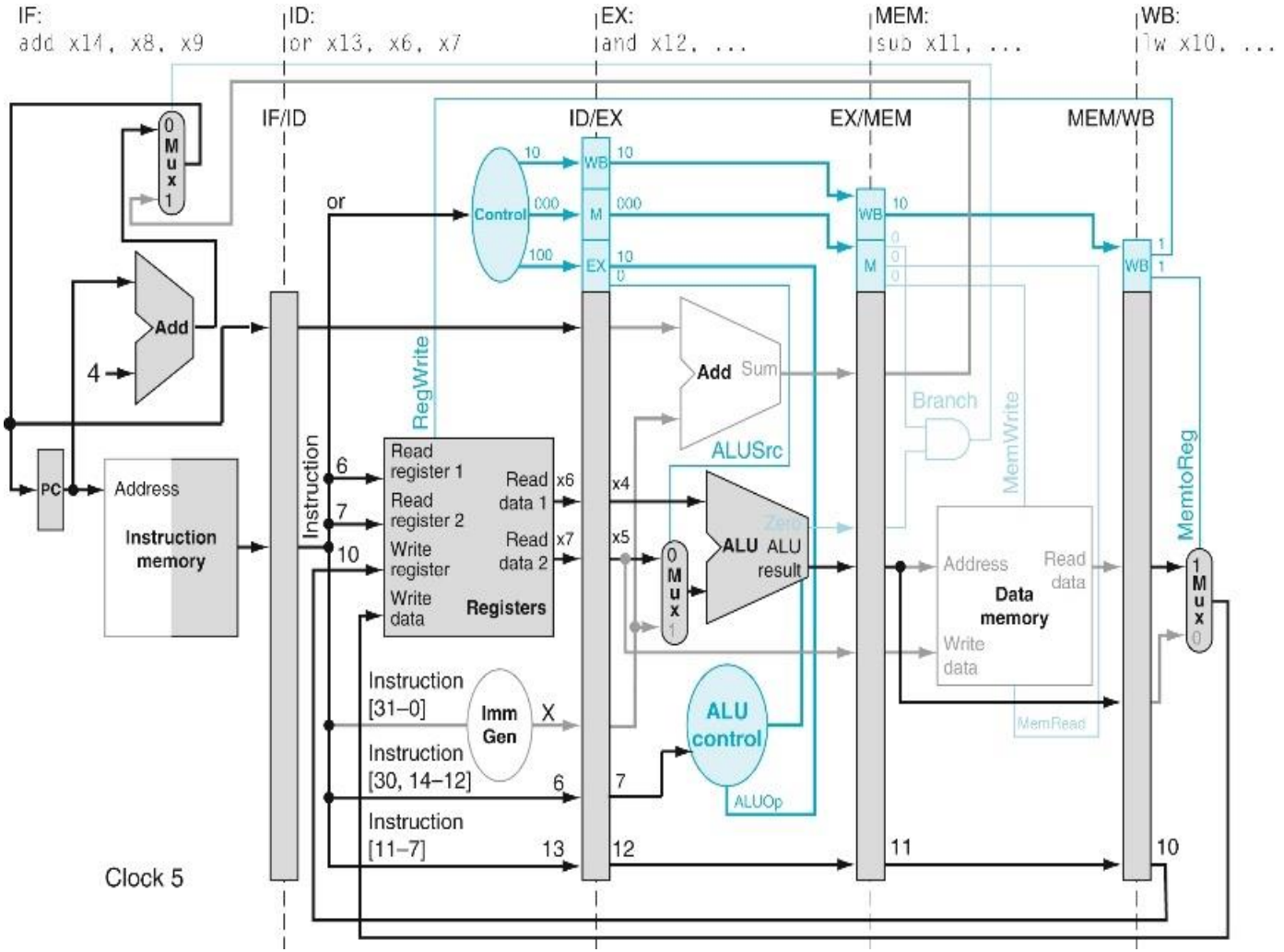
Clock Cycle 3



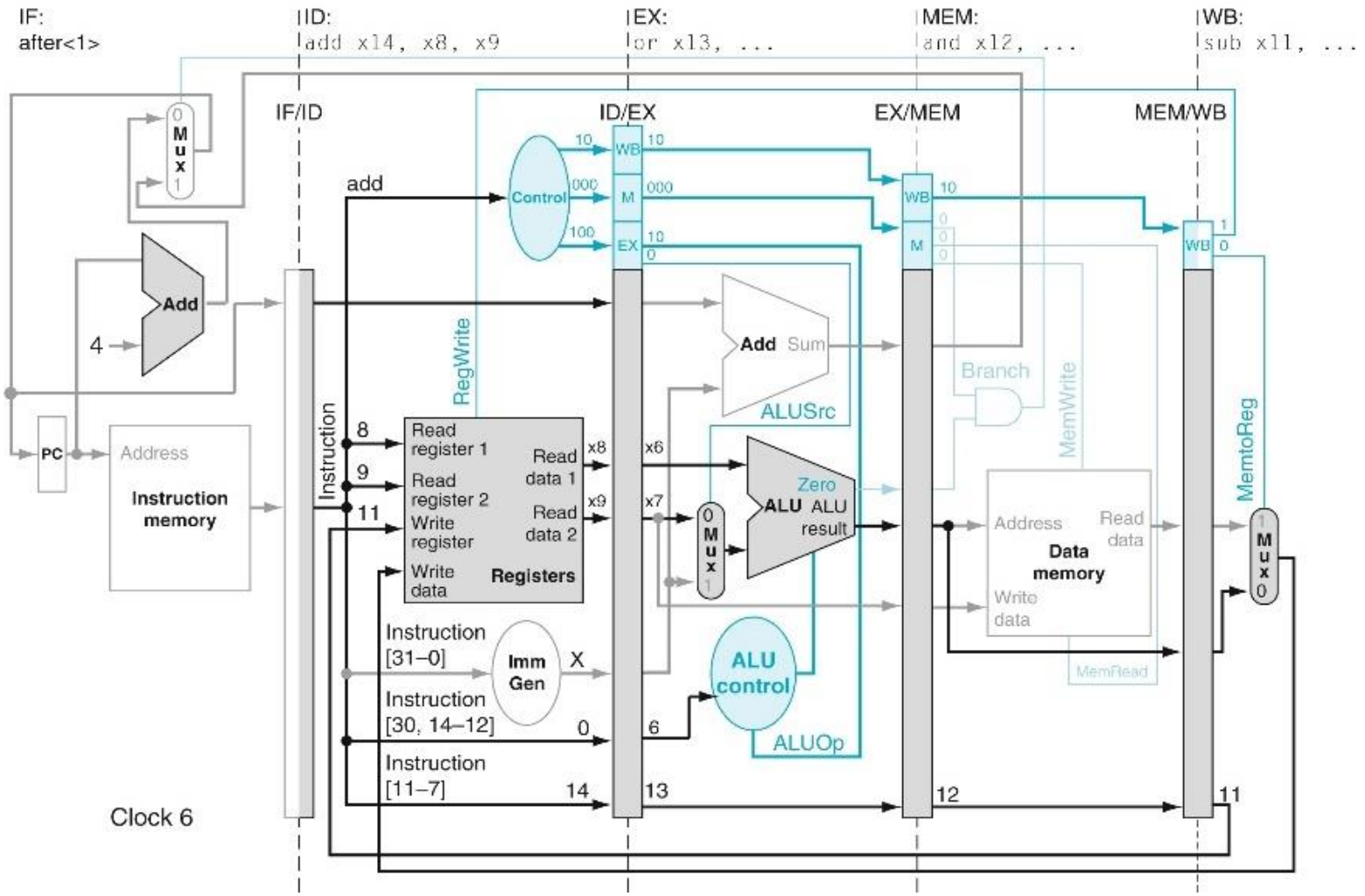
Clock Cycle 4



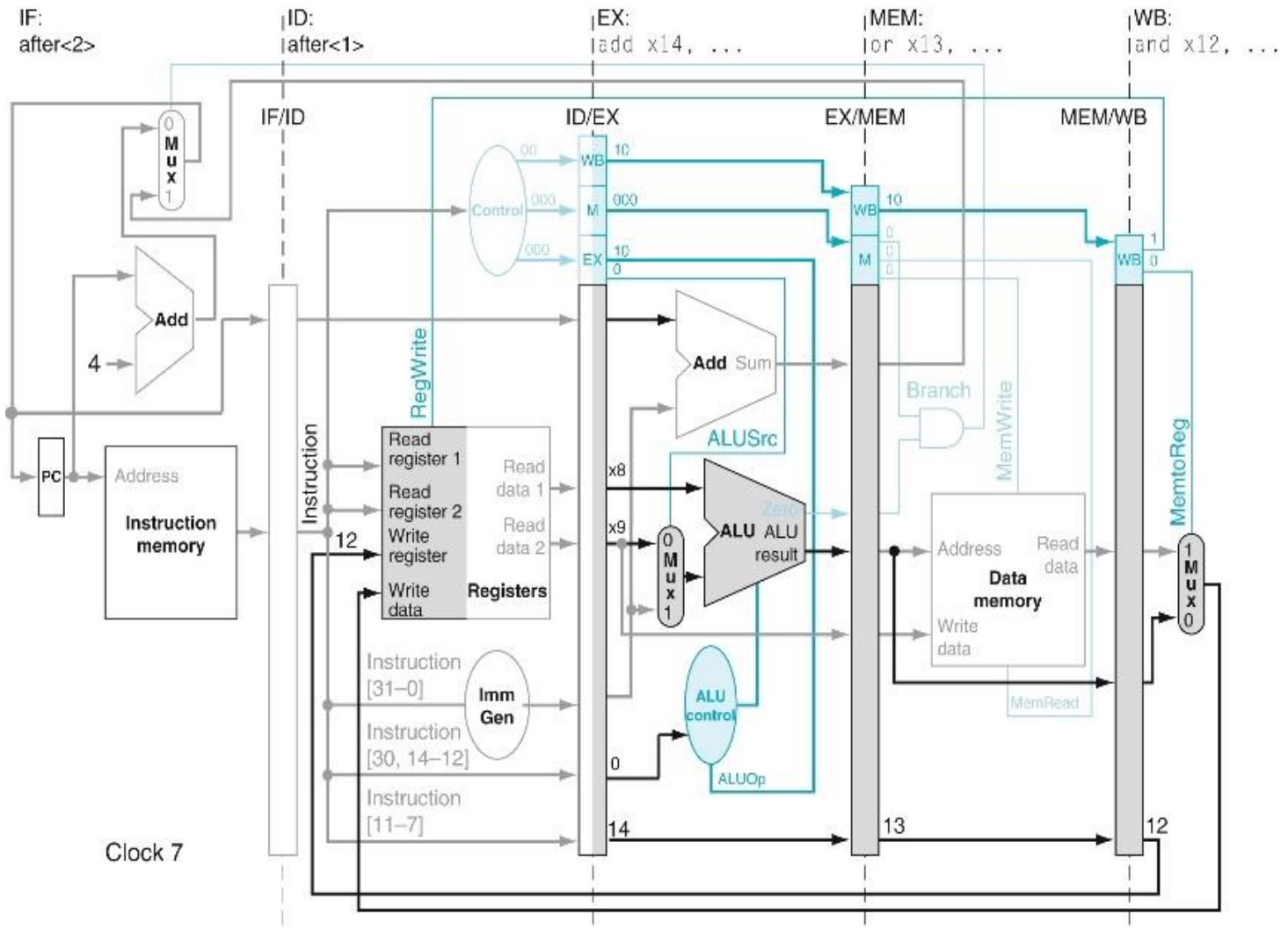
Clock Cycle 5



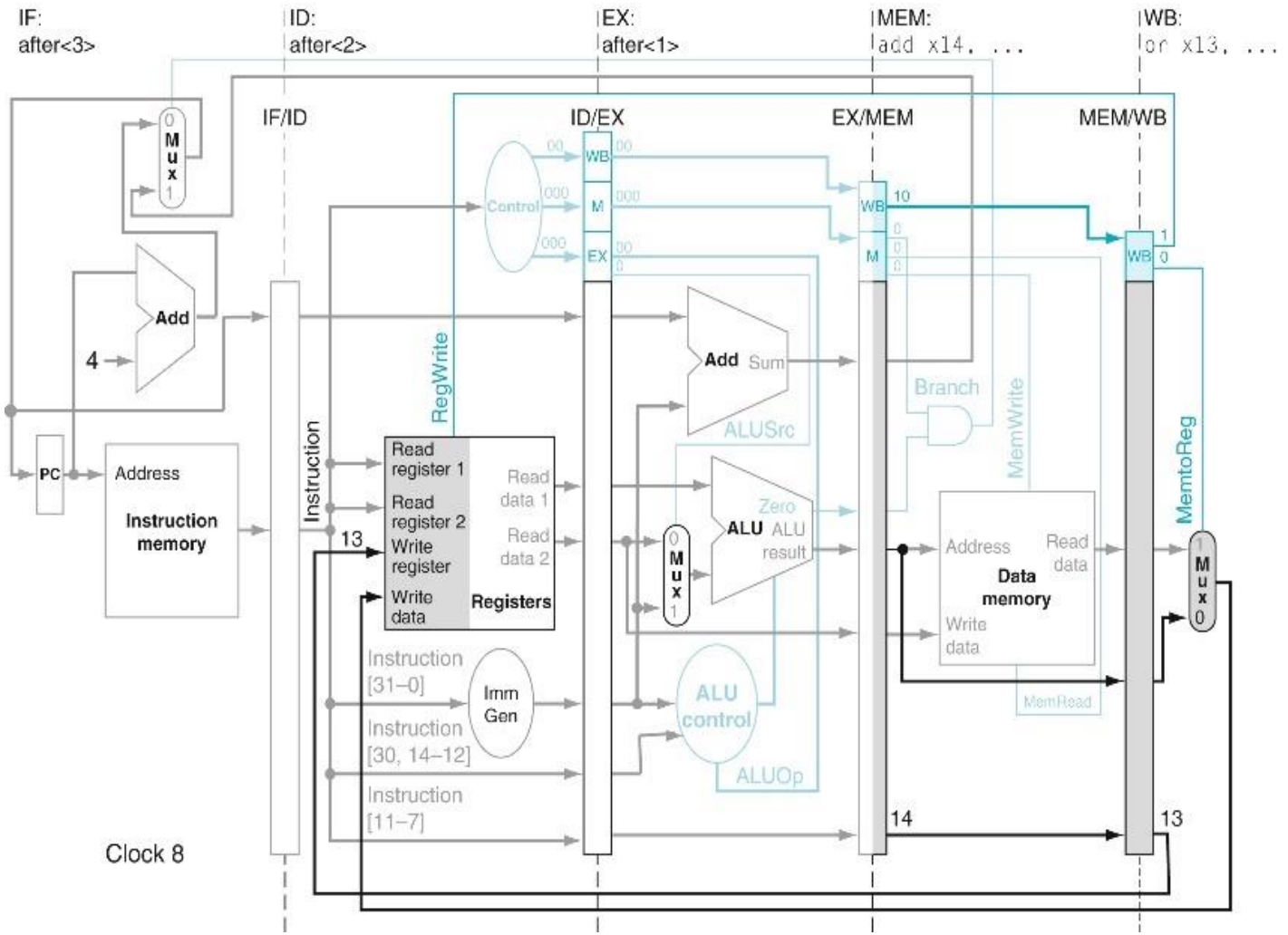
Clock Cycle 6



Clock Cycle 7



Clock Cycle 8



Clock Cycle 9