DEPARTMENT OF COMPUTER SCIENCE

COLORADO SCHOOL OF MINES
EARTH • ENERGY • ENVIRONMENT

CSCI 341: Computer Organization
WS 13: Pipelined Datapath and Control

1	Why must the clock cycle for a computer be determined by the longest instruction? Why can't variable length cycles be used?
2	Explain the concept of pipelining. This is an important concept so be through in your explanation.
3	How many clock cycles are there per instruction in a RISC-V pipelined processor?
4	Is every functional unit used by every instruction?

5	For instructions that need to update a register, how does the register that needs to be updated get passed through the pipeline?
6	List the three hazards possible on a pipelined datapath as well as why they occur.
7	By introducing pipelining there can no longer just be one set of control signals. How does the RISC-V pipelined processor solve this problem?
8	List the control registers at each stage in the pipeline.
9	What problem does data forwarding solve?

10	Which instructions will either need forwarding or create a hazard?
	
	`add t0, t0, t0`
	`add t1, t1, t0`
	`add t0, t1, t2`
	`sw t1, 0(s0)`