FEUP
Universidade do Porto
Faculdade de Engenharia

Departamento de Engenharia Eletrotécnica e de Computadores

Digital Systems Design

4th year – 1st semester
Exam – January 16th, 2013

Maximum duration: 2h30m, closed book.

[4 points]

1 – During the digital design process for microelectronic technologies it is fundamental to perform various verification stages that are applied to the models of the system under design.

a) Explain the differences between the logic simulation processes for functional verification and for post-implementation (or post-route) verification. Refer to characteristics of the circuit models used and the expected results or each of the simulation stages.

b) Based on your experience acquired during the laboratory projects for the FPGA technology, explain under which circumstances can the post-route verification be avoided, and which are the potential risks that may arise from this procedure.

[6 points]

2 – Consider the following Verilog module, where **clk1** and **clk2** are clock signals with frequencies equal to 200 kHz e 800 kHz, respectively. These two clock signals are derived from the same 100 MHz clock source.

```
module exam_psd_1213(reset, clk1, clk2, din, dout);
input reset, clk1, clk2;
input  [15:0] din;
output [15:0] dout;
reg    [15:0] R1,R2,R3,R4;
always @(posedge clk1)
  if (reset)
    {R1,R2,R3} <= 48'd0;
  else
  begin
    R1 <= din; R2 <= R1; R3 <= R1 - R2;
  end
always @(posedge clk2)
  if (reset)
    R4 <= 16'd0;
  else
    R4 <= R4 + R3;
assign dout = {{2{R4[15]}}, R4[15:2]};
endmodule
```

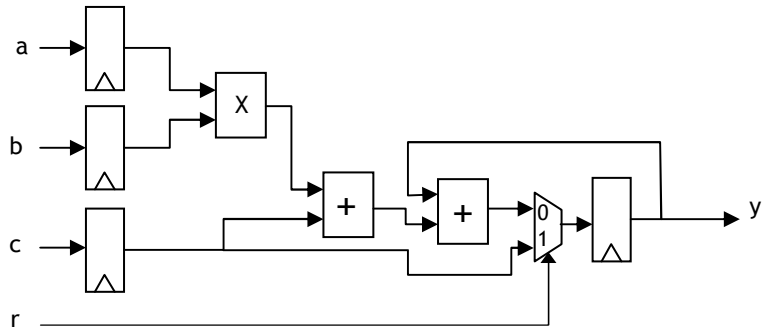
a) Draw a RTL block diagram that represents the logic circuit that is inferred from the Verilog code above by a RTL synthesis tool (this should be represented in terms of arithmetic blocks, registers and other blocks)

b) The input and output data (**din[15:0]** and **dout[15:0]**, respectively) represent signed integers in two's complement. During the functional simulation it has been observed that, in some situations, the numeric results are not numerically correct. Explain why and indicate which corrections should be done in the Verilog code in order to correct that situation.

c) This circuit uses two clock signals, receiving input data at **din[15:0]** at clk1 rate and producing the output results in **dout[15:0]** at clk2 rate. Explain how could you build an alternative design for this system, using a single 100 MHz clock signal for the whole circuit.

[4 points]

3 - The following figure shows the block diagram of a digital system, where the inputs (**a**, **b** and **c**), the output (**y**) and all the internal connections are 32 bit wide (the **r** input is a single bit). The arithmetic blocks that perform the addition and multiplication are fully combinational circuits.



a) Write a synthesizable Verilog module that represents the circuit above.

b) Consider you know the timing characteristics of the registers, adder, multiplier and multiplexer (the maximum and minimum propagation delays). Explain how could you estimate the maximum clock frequency supported by this circuit, before performing the logic synthesis process.

[4 points]

4 - Consider the circuit depicted in the figure above (question 3). This system receives the input data and produces the output results in each clock cycle. From the analysis of the application this will be used into, it is known that the input `b` is zero for 50% of the time, during 40% it is equal to 1 and only 10% of the values are different from zero and 1. Besides, it is also known that it is frequent to receive in this input long sequences of ones or zeros.

a) Explain how could you take advantage of this knowledge to transform the given circuit in order to reduce the power consumption. If convenient, illustrate you answer with a block diagram that shows the suggested modifications.

b) Another solution that has been proposed to further reduce the power consumption consists in transforming the arithmetic blocks into pipelined circuits, that will be able to operate with a faster clock signal. Do you agree with this proposal? Justify your answer.

[2 points]

5 - When developing a (incorrect) model of a combinational circuit, the RTL synthesis process may translate some signals to memory elements of type transparent latch. Explain in which situations this may occur and the consequences that may arise for the operation of the circuit after its physical implementation.

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