Flexible, 3D Fan-Out Wafer Level Packaging for Wearable Devices

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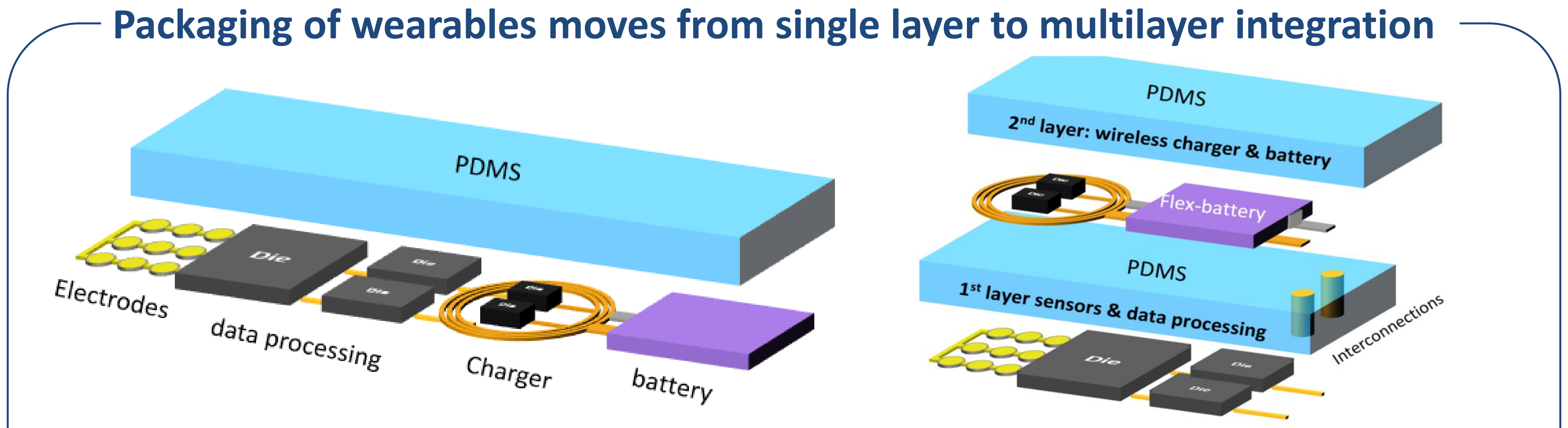
Introduction and motivation

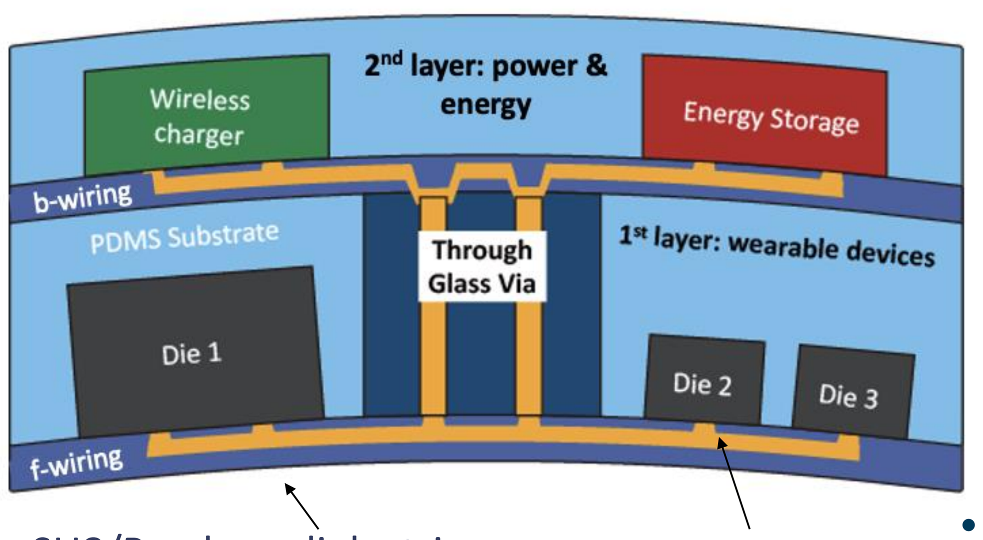
Packaging of wearables moves from single layer to multilayer integration



- Low level of integration & large form factor
- Limited sensing resolution and modality
- Insufficient capability in personalized configuration

- Reduced form factor of wearables
- Enhanced performances in spatial resolution and multifunctional integration
- Addressed safety concern of batteries

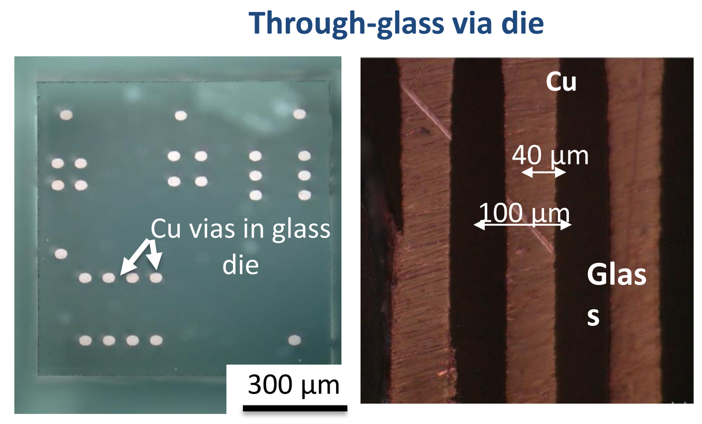
Newly designed flexible 3D FOWLP for wearables



SU8/Parylene dielectric layer

Electroplated Cu

Through-glass via die



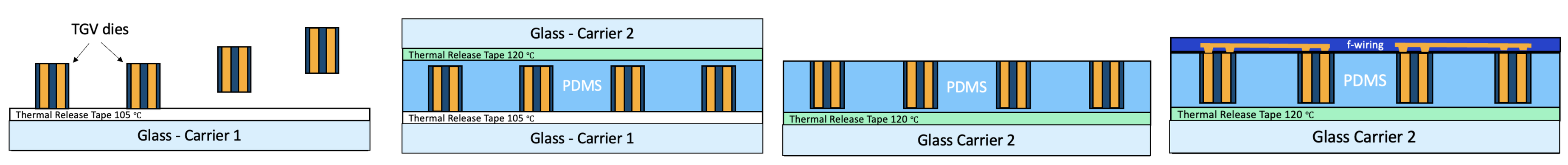
Top view

Cross-section

- Flexible FOWLP (FlexTrate™)
- Backside wiring for multilayer interconnections
- Through-glass via die (TGV) as through PDMS via

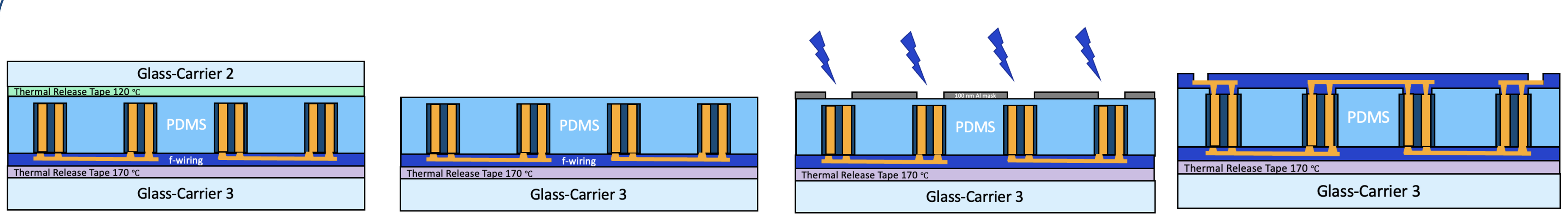
Fabrication process of 3D FOWLP

Conventional flexible FOWLP, (FlexTrate™)



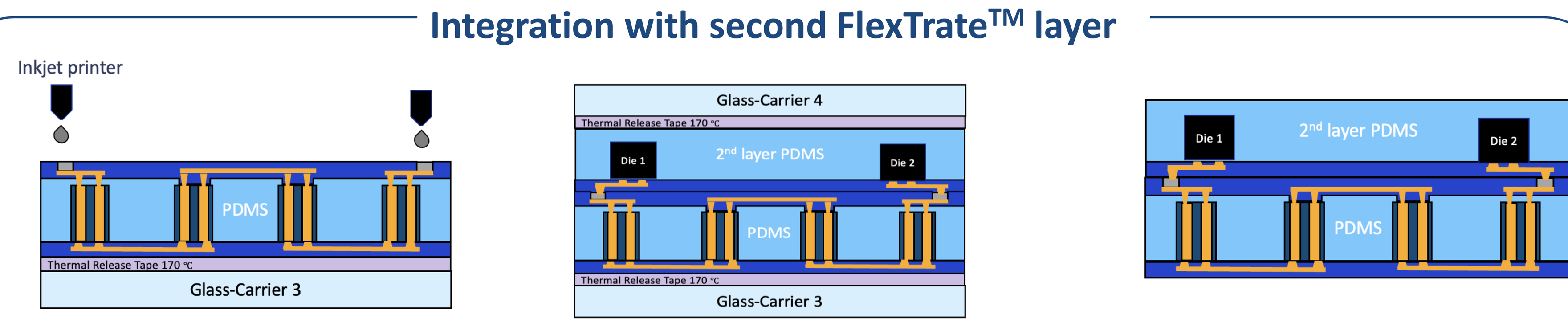
1. Placement of TGVs on thermal release tape
2. Molding and curing of PDMS with the 2nd carrier
3. Release of the 1st carrier
4. Corrugation and metallization of wiring

Opening backside contacts and wiring



5. Lamination of 3rd carrier
6. Release of the 2nd carrier
7. Al hard mask deposition and dry etching contact
8. Fabrication of back-RDL

Integration with second FlexTrate™ layer

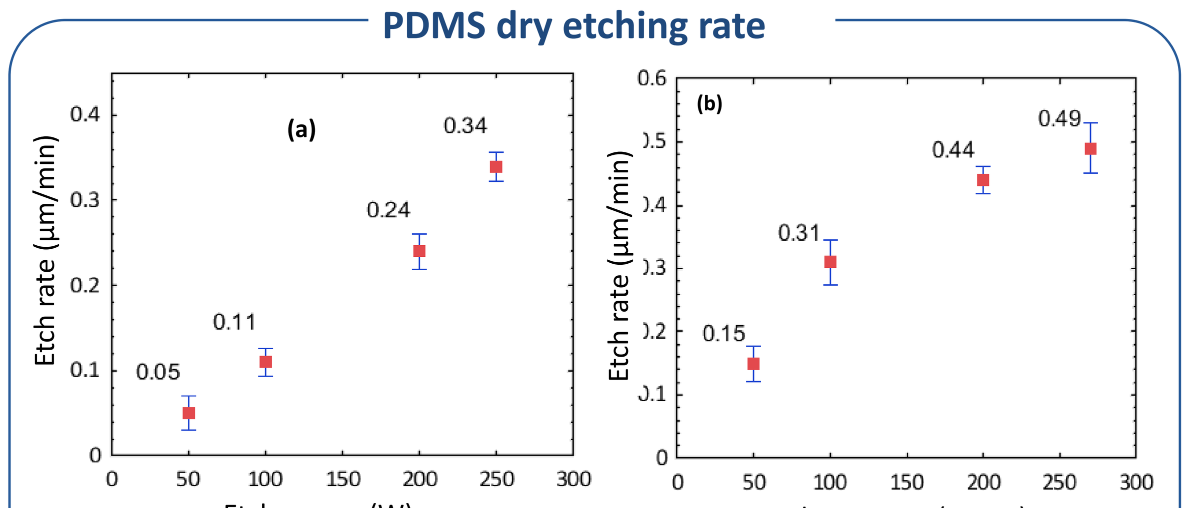


9. Inkjet printing on the opening contact
10. Alignment with another sample and bonding through the silver ink
11. Release of all carriers

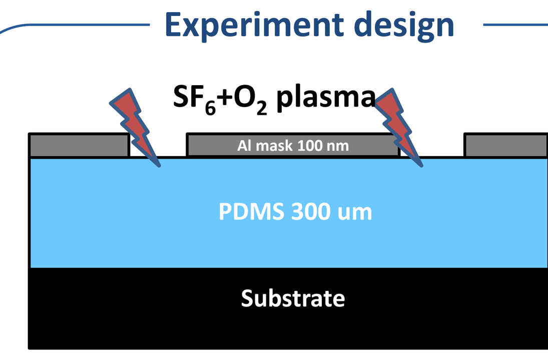
Results and Discussion – Backside opening of FOWLP

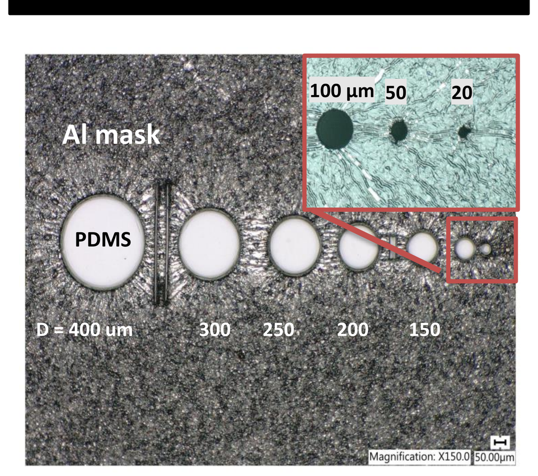
- 100 nm pure Al evaporated on PDMS (Base:cure agent = 10:1) as a hard mask
- Feature size: diameters are from 10 µm to 500 µm
- RIE dry etch samples for 20 mins
- Plasma gas flow $SF_6 : O_2$ = 80 sccm : 20 sccm

PDMS dry etching rate



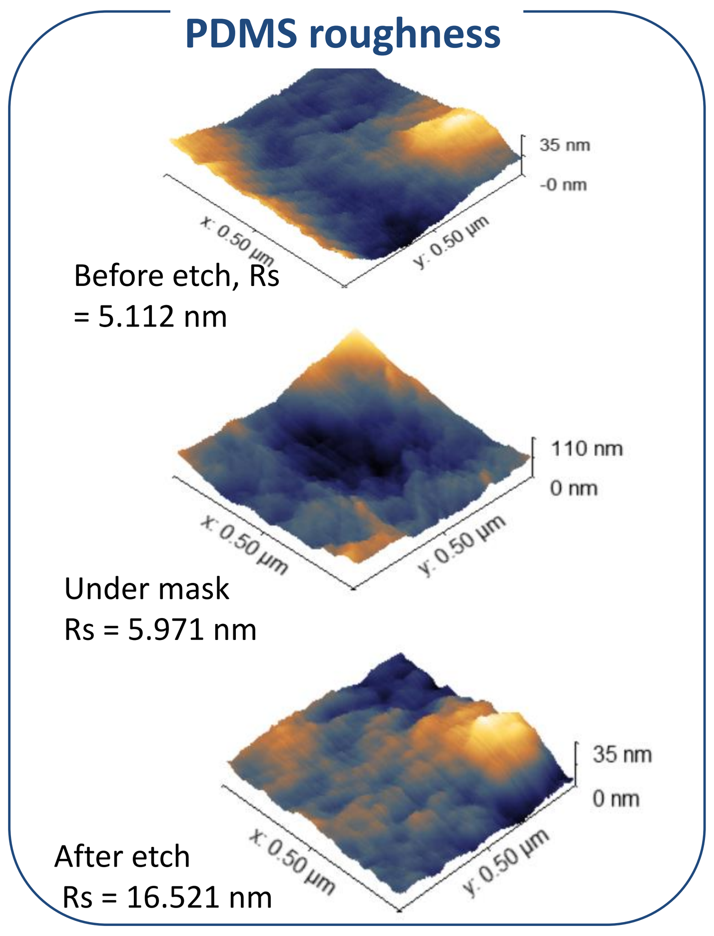
Experiment design



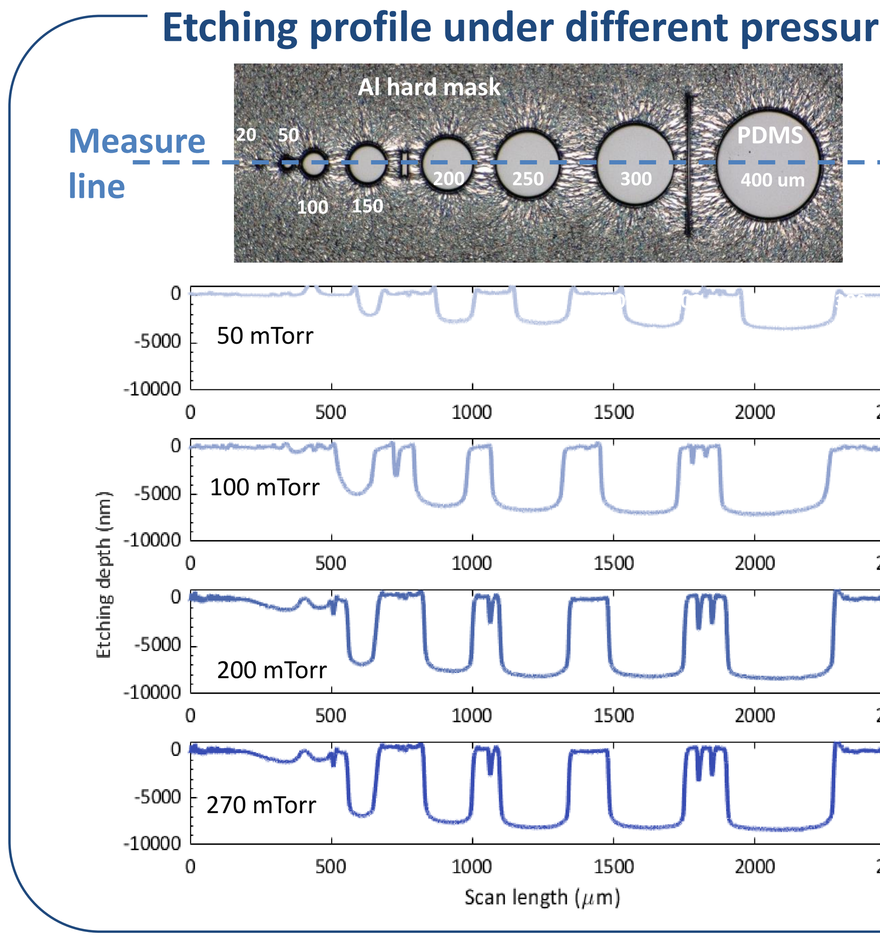


Optical image of PDMS film with patterned mask

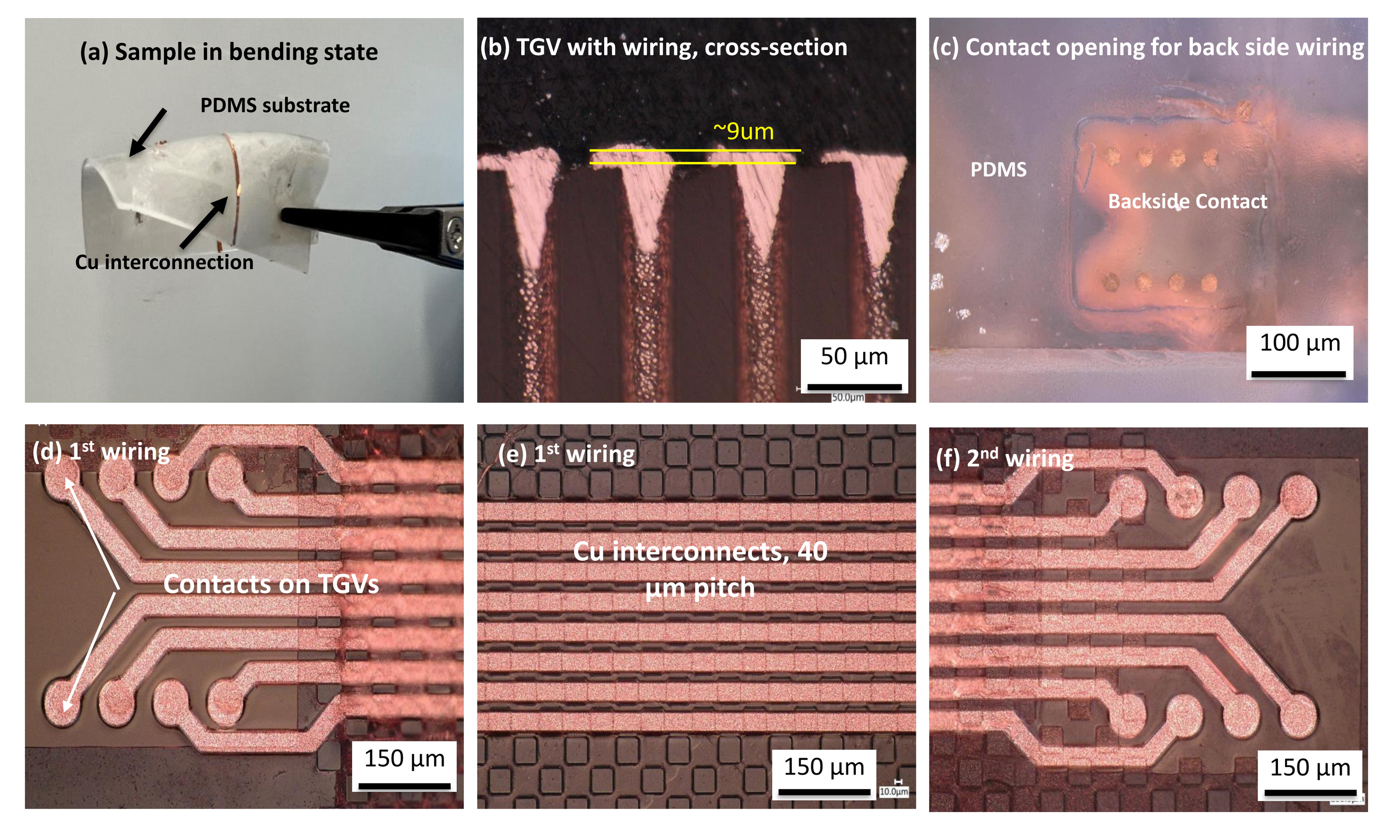
PDMS roughness



Etching profile under different pressure

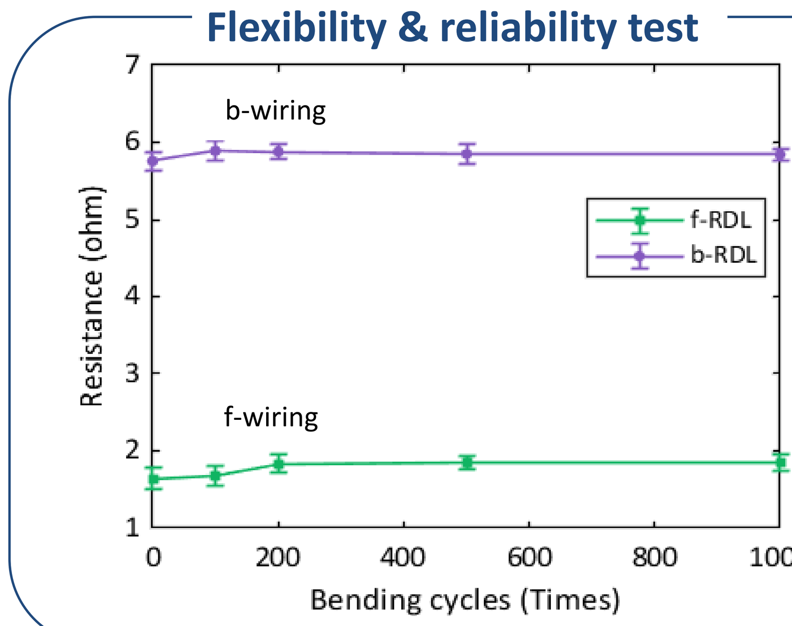


Results and discussion – wiring on backside of FOWLP

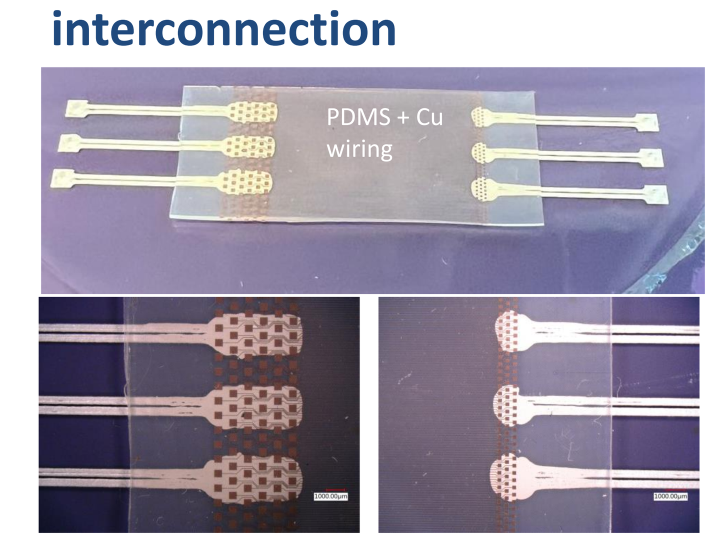


- 40 µm wire pitch front side wiring (f-wiring) and back-side wiring (b-wiring) is developed with ~ 9 µm Cu wire thickness
- 4-point probe measurement after the bending test at 1 mm, 1000 times is conducted for demonstrating the flexibility

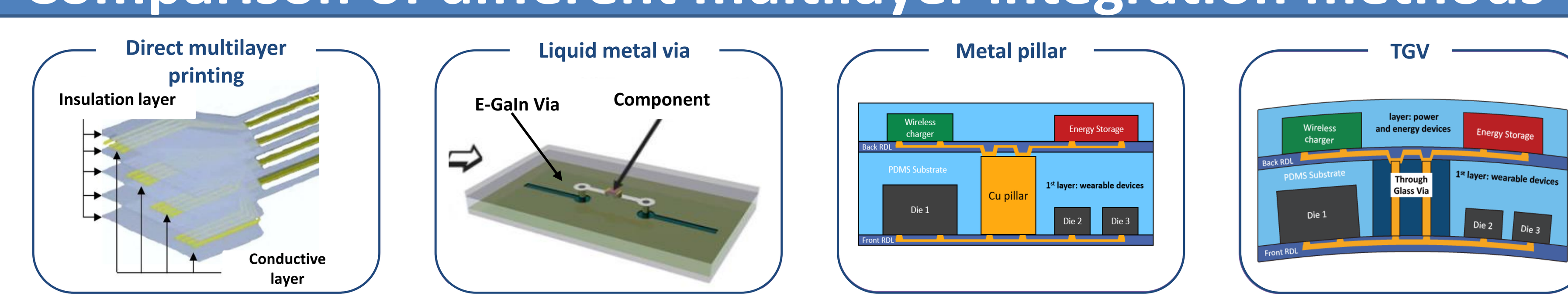
Flexibility & reliability test



Inkjet printing for multilayer interconnection



Comparison of different multilayer integration methods



Methods	Fabrication process	Integration	Via materials	Conductivity (10^6 S/m)	Thermal conductivity (W/m·K)	Via pitch (um)	Flexibility (mm)	Cost	Remark
Multilayer printing [1]	Inkjet printing	Monolithic, homogeneous	Conductive ink (Silver)	1-10	5-200	~ 100	Foldable	Low	Stress accumulation during fabrication
Liquid Metal Via [2]	laser drilling	Heterogeneous	E-GaIn	3.4	20	> 100	< 1 mm	High	Low aspect ratio, safety, reliability
Metal pillar [3]	Pick&place	Heterogeneous	Cu	59	401	> 500	< 1 mm	Low	Alignment accuracy
TGV dielets (This work)	Pick&place	Heterogeneous	Cu	59	401	< 100	< 1 mm	Medium	Excellent RF performance

Conclusion and acknowledgement

- A multilayer integration structure using 3D FOWLP for flexible wearable devices is proposed
- Developed a multilayer fabrication process with
  - TGV dies with **100 µm pitch, 7.5 aspect ratio** are employed for the connection of two layers
  - Dry etching of PDMS with **maximum 0.49 µm/min** etching rate
  - Front and back side RDLs and inkjet printing of silver conductive gel process

- We would like to thank the UCLA CHIPS consortium for supporting this work!

[1] Liu, Xin, et al. Journal of Microelectromechanical Systems (2021).
[2] Jiang, Qin, et al. Advanced Materials Technologies (2021).
[3] Y. Susumago et al, ECTC (2021)

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