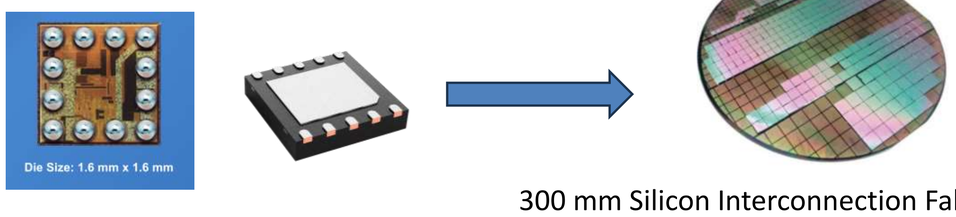
Structure Rebuilding Of Legacy Chips For Flip-Chip Fine Pitch Bonding on Si-IF

Cheng-Ting Yang, Haoxiang Ren, and Subramanian S. Iyer | UCLA CHIPS

Motivation

- Most of the legacy chips on the shelf are packaged
- Packaged chips have large-size I/Os and footprint, which limit their applications in fine-pitch packaging and fan-out wafer level packaging (FOWLP) as figure shown below



300 mm Silicon Interconnection Fabric (Si-IF) [1]

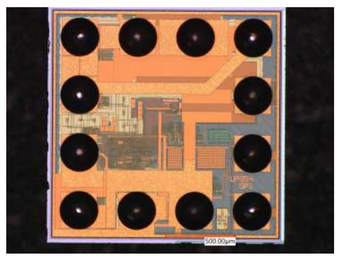
Legacy chips are not compatible with Si-IF and wafer-scale computing

- The package also induces large parasitics which degrade the system's overall performance
- Systematic methods of reconstructing various traditional I/Os are investigated

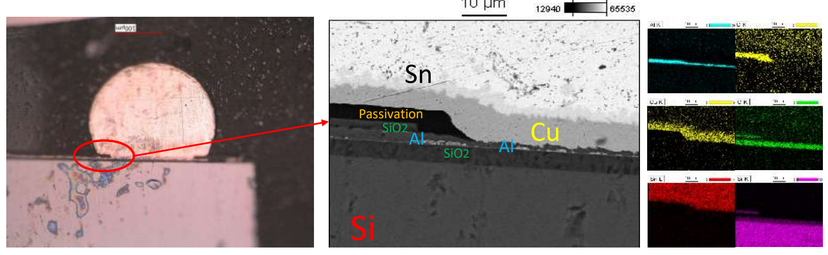
[1] S. Jangam and S. S. Iyer, "Silicon-Interconnect Fabric for Fine-Pitch (≤10 µm) Heterogeneous Integration," IEEE TCPMT, 2021.

Legacy BGA I/O Rebuilding

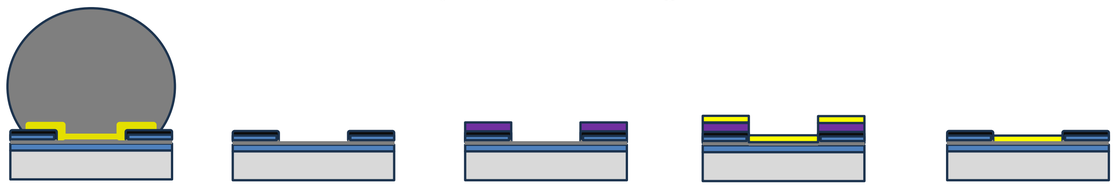
- BGA Chip



- Solder Bump Cross-section

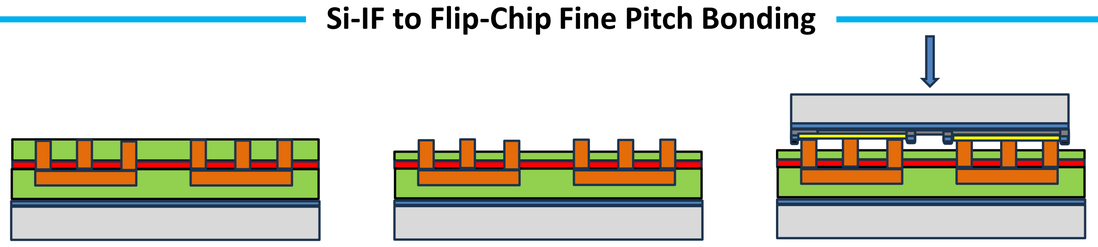


BGA Chips I/O Rebuilding Process



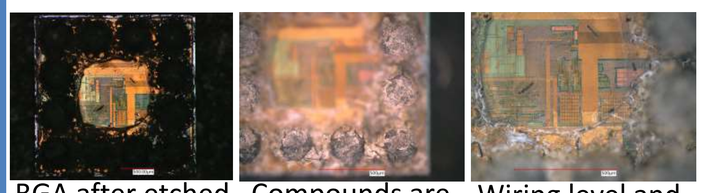
1. BGA solder bumps
2. Etch solder bump and copper
3. Photoresist patterned
4. Gold sputtering
5. Lift off

Si-IF to Flip-Chip Fine Pitch Bonding



1. Cu pillar CMP
2. Recess SiO2 to expose Cu pillar
3. Rebuilding BGA flip-chip fine pitch bonding

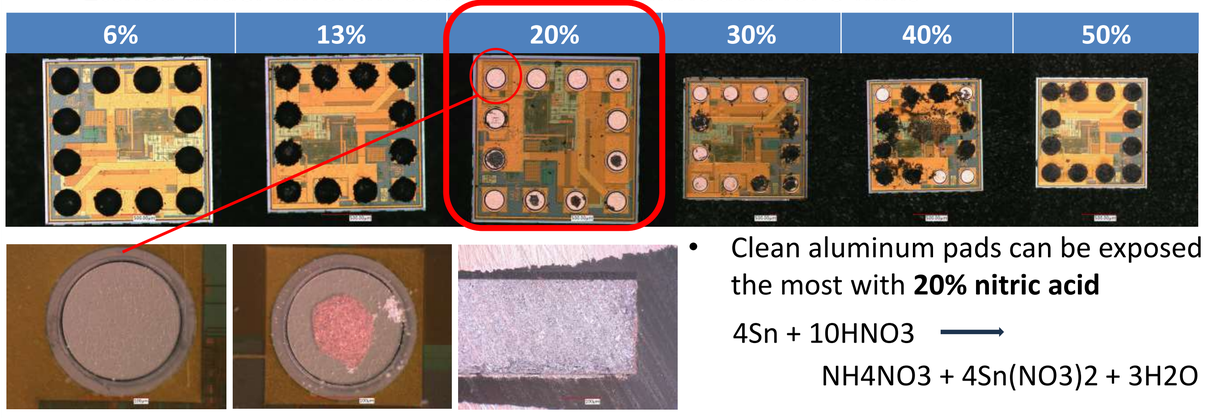
- **Etched under 70% nitric acid for 5 minutes**



BGA after etched by 70% nitric acid | Compounds are insoluble | Wiring level and passivation layer are intact

- The reaction of tin and **concentrated nitric acid** generates compounds insoluble for water or acid
- The compounds prevent the copper under the aluminum from being t the whole structure away

- **Etched under different concentration of nitric acid for 5 mins**



Copper and tin residuals

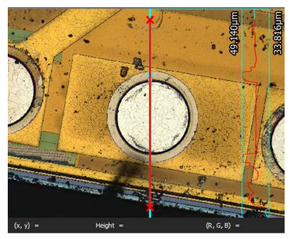
- Clean aluminum pads can be exposed the most with **20% nitric acid**

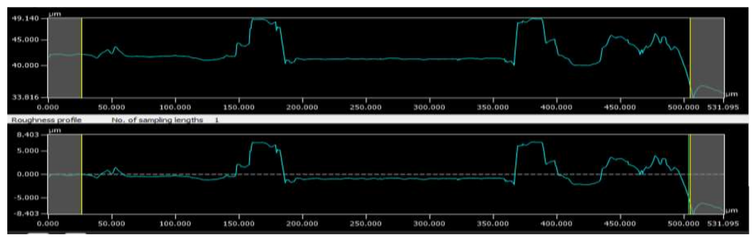
$$4Sn + 10HNO_3 \longrightarrow NH_4NO_3 + 4Sn(NO_3)_2 + 3H_2O$$

- Die and BEOL remains intact

Legacy BGA I/O Rebuilding (cont.)

- Pre-sputtering pad investigation

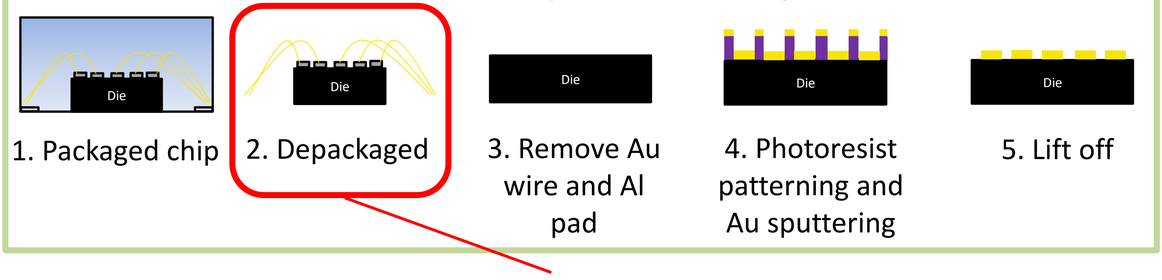




- The height difference between the passivation layer and aluminum conforms to the structure shown in SEM before BGA rebuilding
- Aluminum is successfully exposed

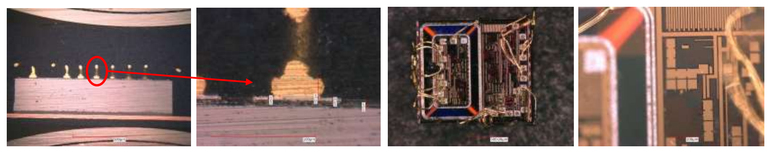
Legacy Wire-Bond Chips Reconstructing

Au-Al Wire-Bond Chips Reconstructing Process



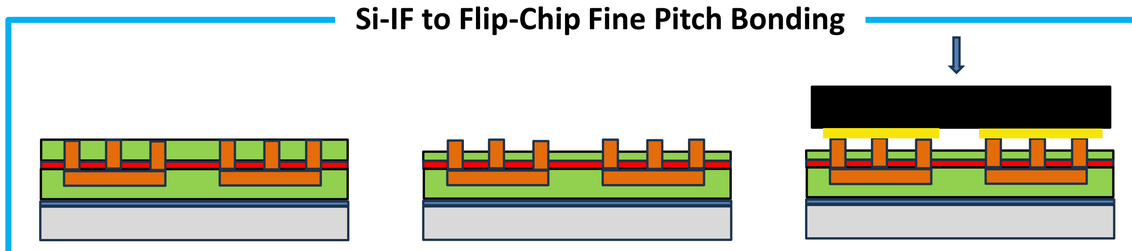
1. Packaged chip
2. Depackaged
3. Remove Au wire and Al pad
4. Photoresist patterning and Au sputtering
5. Lift off

- Wire-bond die cross-section
- After depackaged



- Die can be fully exposed by selectively etching
- BEOL and the die remain intact

Si-IF to Flip-Chip Fine Pitch Bonding

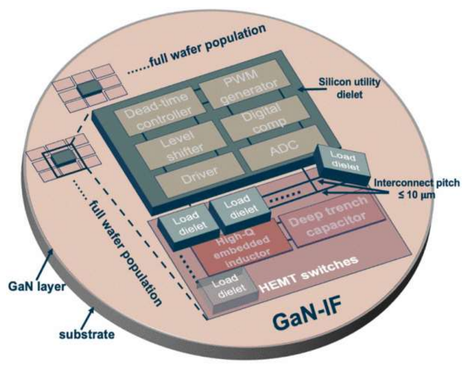


1. Cu pillar CMP
2. Recess SiO2 to expose Cu pillar
3. Rebuilding wire-bond chip flip-chip fine pitch bonding

Summary

- Legacy BGA chip and legacy wire-bond chip are successfully reconstructed by selective etching
- Structures and components should be determined before rebuilding the chips
- Wire-bond material includes Au wires to Al pads and Cu wires to Cu-caped-Al pads, different metal systems require distinct chemicals and concentrations to expose or remove the original I/Os

Potential Applications



3D schematic of the GaN-IF: a wafer-scale heterogeneous die-to-wafer integration [2]

- Depackaging is a powerful technique for failure analysis
- Rebuilt chips are especially beneficial for Si-IF and significantly eliminate the time for waiting for taped-out chips to test wafer-scale system
- GaN driver chip directly bonded and connected with GaN switch on Si-IF reduces the parasitics thus minimizing the gate ringing

[2] H. Ren, K. Sahoo, T. Xiang, G. Ouyang and S. S. Iyer, "Demonstration of a Power-efficient and Cost-effective Power Delivery Architecture for Heterogeneously Integrated Wafer-scale Systems," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 1614-1621, doi: 10.1109/ECTC51909.2023.00274.

Acknowledgement

This work was supported in part by the Semiconductor Research Corporation (SRC) JUMP CHIMES, UCOP MRPI MRP-17-454999, and the UCLA CHIPS consortium.

2023 UCLA CHIPS Workshop
Poster Session

UCLA CHIPS CENTER FOR HETEROGENEOUS INTEGRATION AND PERFORMANCE SCALING