# Study of CTT-based nvSRAM array

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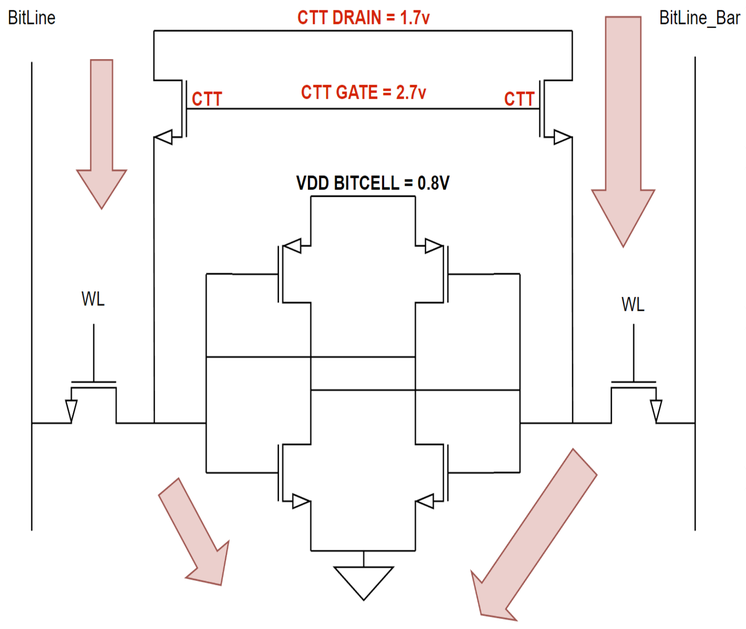
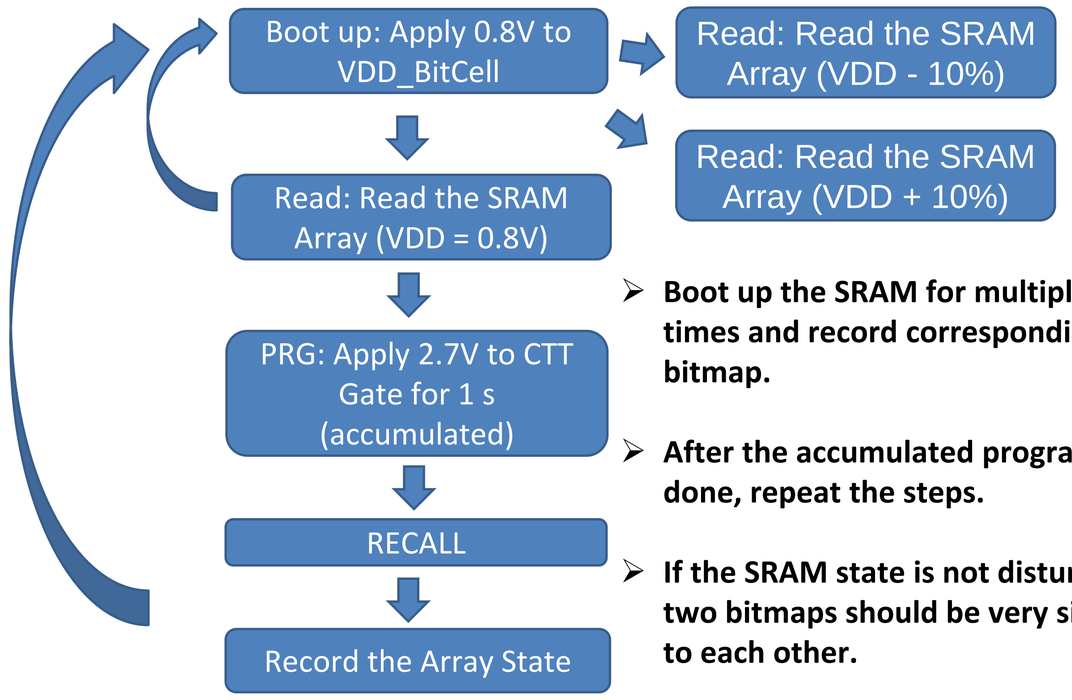
## Introduction



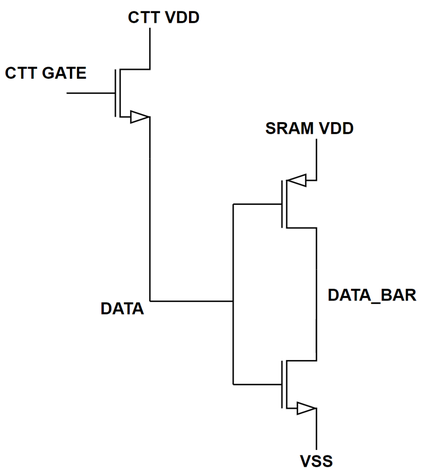

- We have previously proposed an 8-T CTT–based non-volatile SRAM structure.
- However, the programming operation affects normal SRAM devices
- The introduced $V_{TH}$ mismatch is insufficient to ensure 100% recall accuracy
- A novel 10-T structure is proposed to overcome the challenges.

## Experiment Setup

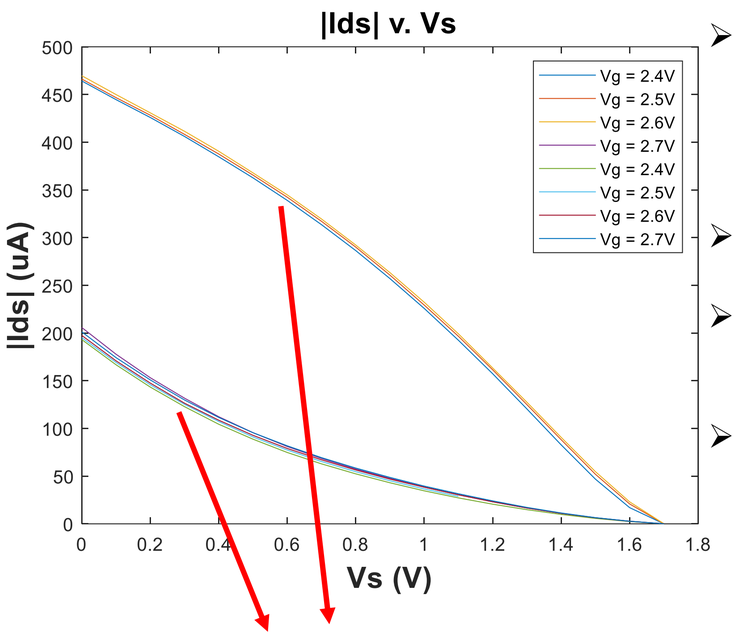



- Boot up the SRAM for multiple times and record corresponding bitmap.
- After the accumulated program is done, repeat the steps.
- If the SRAM state is not disturbed, two bitmaps should be very similar to each other.

## Circuit analysis



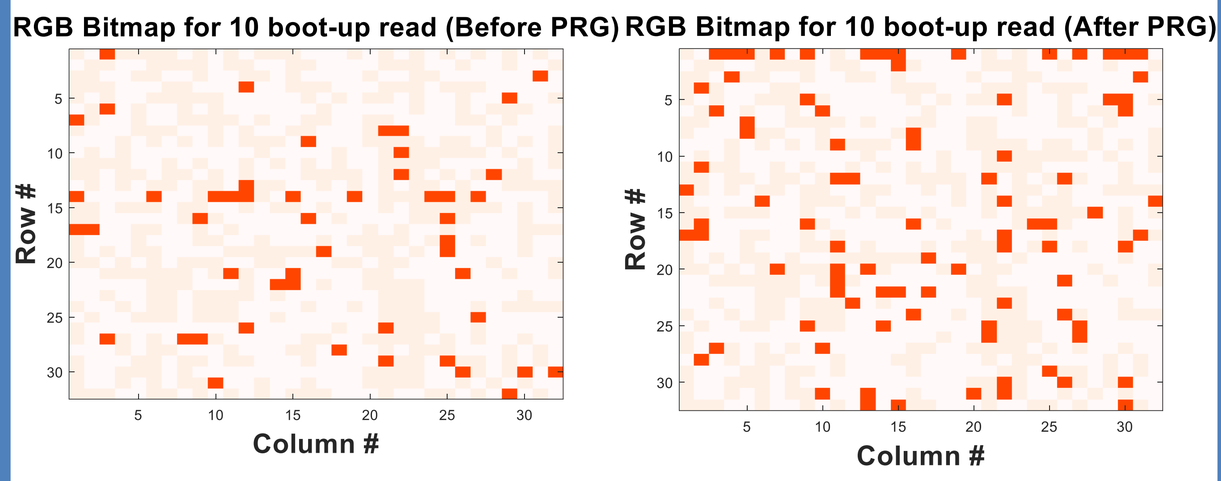

- 22nm FDSOI device model does not support high voltage simulation.
- Half circuit hand analysis is used in complement to the simulation
- During the programming stage, the positive feedback of the SRAM latch is broken
- Due to the rise of data and data_bar node voltage, CTT program is less efficient than expected.




- The measurement is done using probe station under high voltage operating condition (Vg = 2.7V, Vd = 1.7V).
- The data note voltage is estimated to be 1.1V
- The data bar note voltage is estimated to be 0.4V.
- This dual-effect decreases the programming efficiency.
- The high-voltage program produces large threshold voltage difference up to 200mV.

During the PRG mode, the program current not only flows through the CTT cells, but also the SRAM. The low side NMOS is programmed as well, thus irreversibly shifts the NMOS threshold voltage and affects the SRAM state.

## Experiment results




Comparison between the boot-up state bitmap shows SRAM state is being changed during the program stage.

| CTT_VDD = 1.7V CTT_GATE = 2.7V | |
|---|---|
| Accumulated PRG time (msec) | PRG Success-Rate |
| 100 | 83 |
| 200 | 85.7 |
| 300 | 86.7 |
| 400 | 89.1 |
| 500 | 90.3 |
| 600 | 91.2 |
| 700 | 92.4 |
| 800 | 93.1 |
| 900 | 72 |
| 1000 | 70 |

- Since the program efficiency is inadequate, long voltage pulse has similar affect to short voltage pulse.
- The statistical behavior of charge-trapping effect is compensated.
- After PRG time accumulates, both CTT trapping levels are reaching saturation.

## Conclusion

The success rate issue can be more effectively improved with the novel circuit design. The large current to perform program can be absorbed by transistors other than the SRAM cells. This can improve program efficiency and increase success rate.

## Acknowledgement

- This chip was designed by Dr. Nouri and fabricated by Global Foundry in 22FD-SOI technology node.
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