Demonstration of Charge-Trap Transistor for Compute-in-Memory

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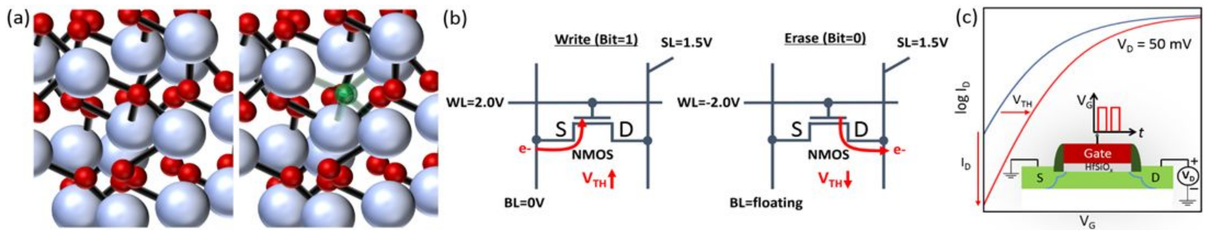
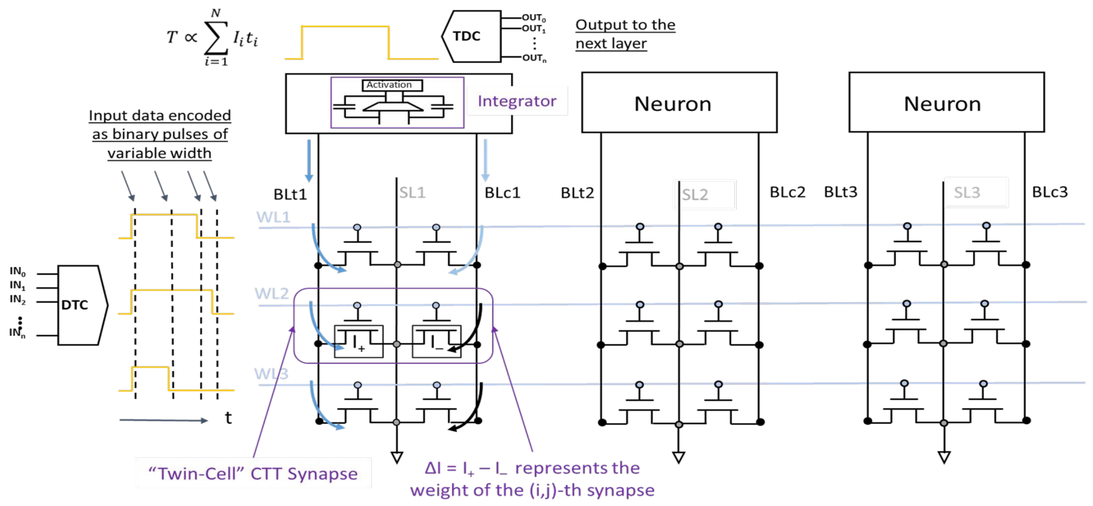
Introduction to Analog CTT for CiM

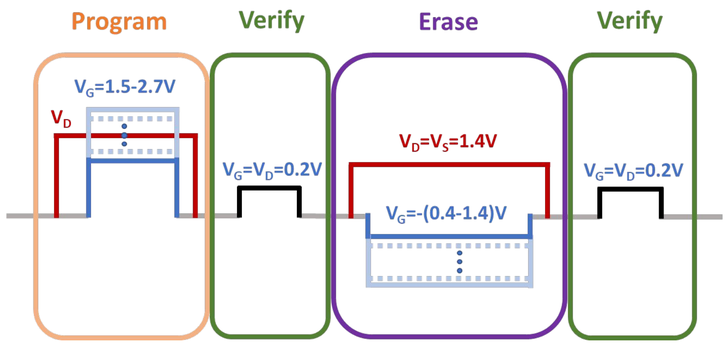


- Oxygen vacancies in HfO_2 can be used to trap charges in a controllable manner
- The mechanism has been successfully used for commercial digital memory
- This mechanism has also been successfully demonstrated for analog memory

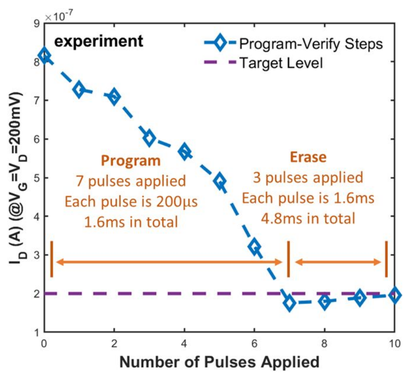


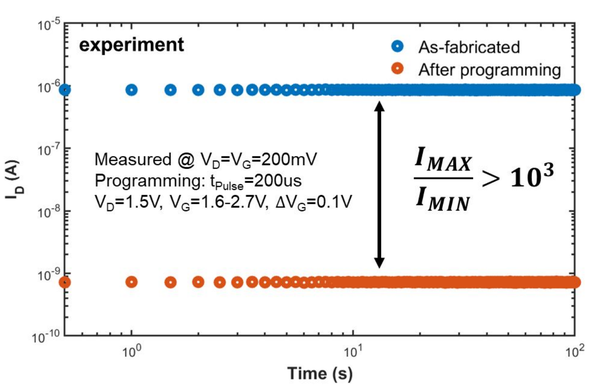
- Twin-cell configuration to encode both positive and negative weight values
- *We demonstrate matrix-vector multiplication (MVM) operation using CTT, fabricated in a standard logic process, as analog non-volatile memory*

Characteristics of CTT as Analog Nonvolatile Memory

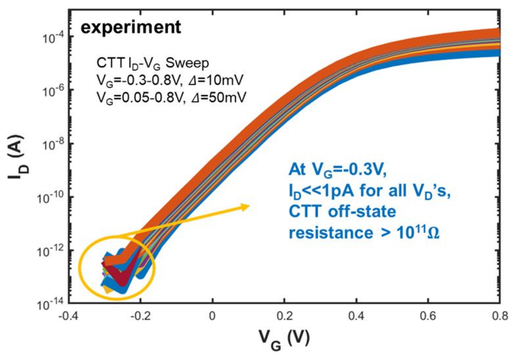


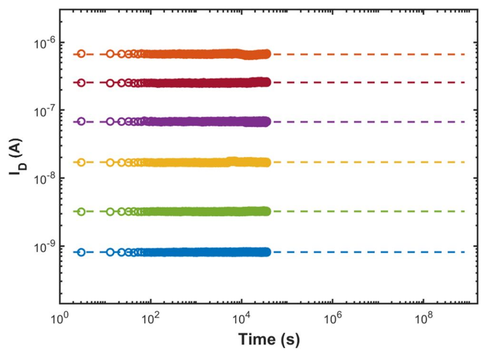
- Closed-loop write-verify calibration process
- Various pulse amplitude with set Pulse width for write
- Constant bias for read/verify
- Calibration ends when boundary conditions are met





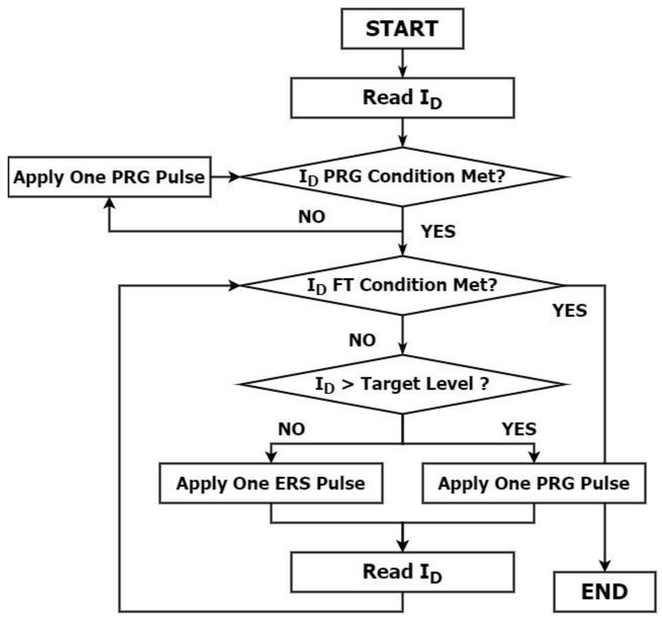
- Write-verify within 3% accuracy with 200 µs prgm and 1.6 ms erase pulses
- As-fabricated CTT current readouts vs. after applying 12 programming pulses
- Programming exhibits ~1000x reduction in channel conductance



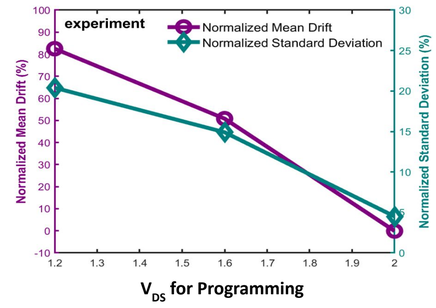


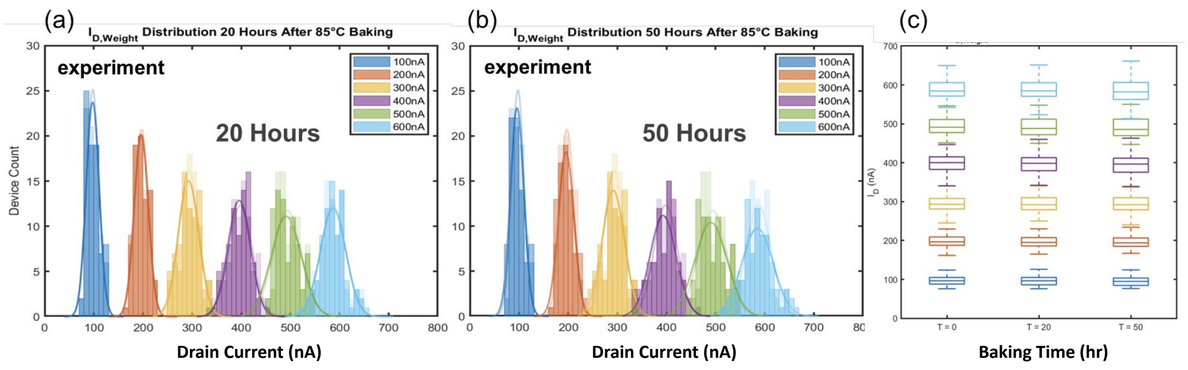
- Less than 1 pA leakage current with -300 mV V_{GS}
- CTT doubles as selector thanks to its three-terminal nature
- Excellent state retention at room temperature

CTT Array Characterization and Study

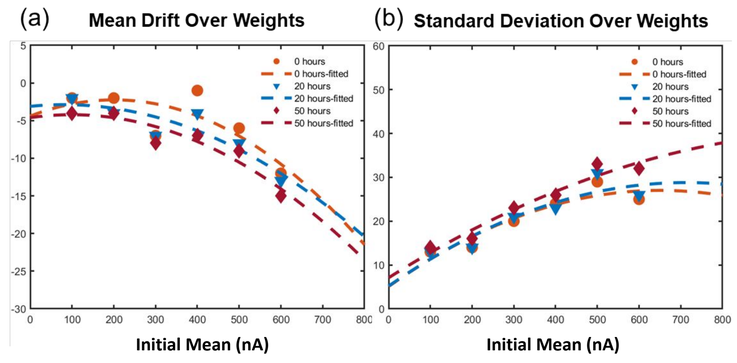


- Closed-loop calibration process
- Calibration terminates when CTT is within 3% error of target
- 20-hr 125 ℃ test shows CTTs with better retention when programmed with larger V_{DS}

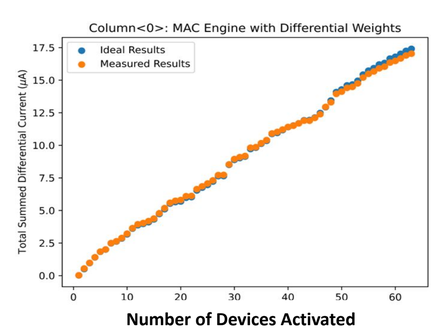




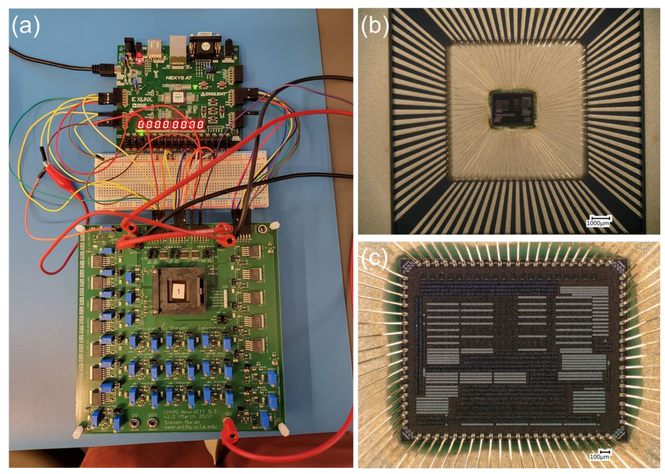
- Programmed array cell distribution after 0, 20, and 50 hours of storage at 125 ℃
- Minimal retention loss after experiments, indicating good temperature resilience



- Measured mean drift and standard deviation after 0, 20, and 50 hours of storage at 125 ℃
- Curves fitted to data points for device modeling



- Measured and Ideal Output vs. number of inputs
- <2% error due to on-chip mux resistance and IR drop



- Setup for testing and experiments

Summary and Acknowledgement

- We demonstrated CTT for analog CIM using commercial technology
- CTT can be embedded with standard logic devices with no additional process
- CTT offers excellent properties as nonvolatile analog memory for edge CiM
  - Negligible retention loss **(up to 125 ℃)**
  - High off-state resistance **(>10^{11} Ω)**
  - Accurate vector-matrix multiplication **(<2% error)**
- We would like to thank the UCLA CHIPS consortium for supporting this work!

2023 UCLA CHIPS Workshop
Poster Session

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