

# Electrical Characterization of Interconnects on FlexTrate

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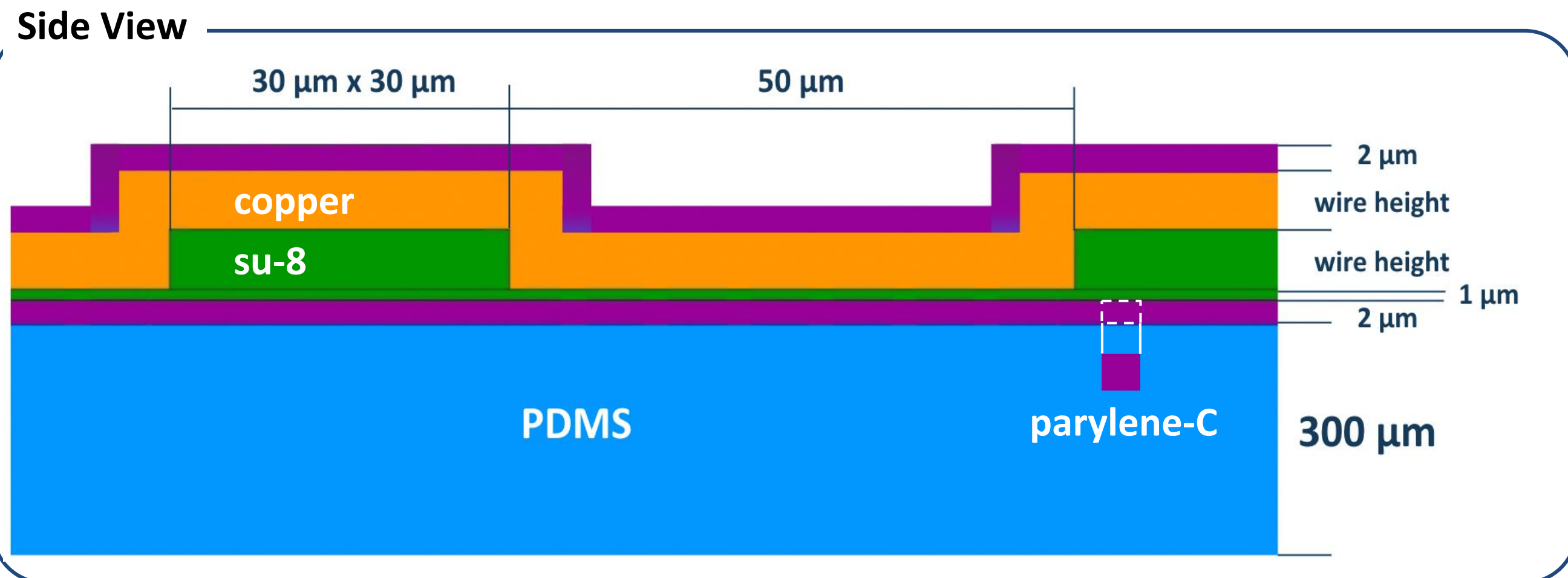
## Introduction

Goal: to characterize the electrical parameters of FlexTrate<sup>TM</sup> over a range of frequencies for different line widths/heights

- Achieved through simulation
- Over 0.1-5 GHz for interconnect behavior at high frequencies
- 5  $\mu\text{m}$ , 10  $\mu\text{m}$ , and 20  $\mu\text{m}$  to cover range of valid fabrication widths

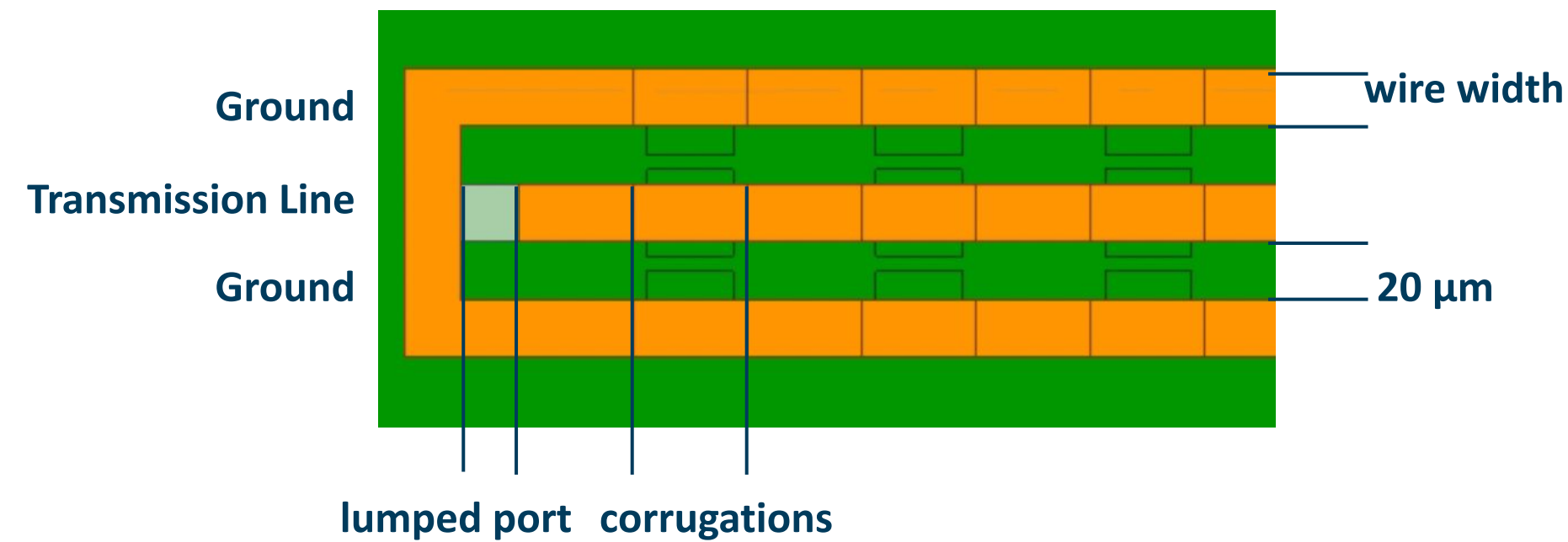
## Simulation Set Up

Full 3D Coplanar Waveguide Model in ANSYS HFSS



\*not to scale

Top View (without conformal top layer of parylene-C)



Wire Width	Wire Height
2.5 $\mu\text{m}$	1 $\mu\text{m}$
5 $\mu\text{m}$	1 $\mu\text{m}$
10 $\mu\text{m}$	2.5 $\mu\text{m}$
20 $\mu\text{m}$	5 $\mu\text{m}$

Dielectric Constants Used (determined through research papers/production):

Material	Parylene-C [1]	Su-8 [2]	PDMS [3]
Dielectric Constant (K)	3.1	2.85	2.75

[1] <https://vsparylene.com/parylene-properties/>

[2] Ayad Ghannam, e.g., EuMC, 2009

[3] N. J. Farcich, e.g., IEEE Transactions on Microwave Theory and Techniques, 2008

Simulation Settings

- Driven terminal solution type with 50  $\Omega$  port impedance for each width/height

## Conversion to RLGC

Conversion:

- Matlab script converts Z-parameter simulation results to RLGC using following equations:

Script Verification:

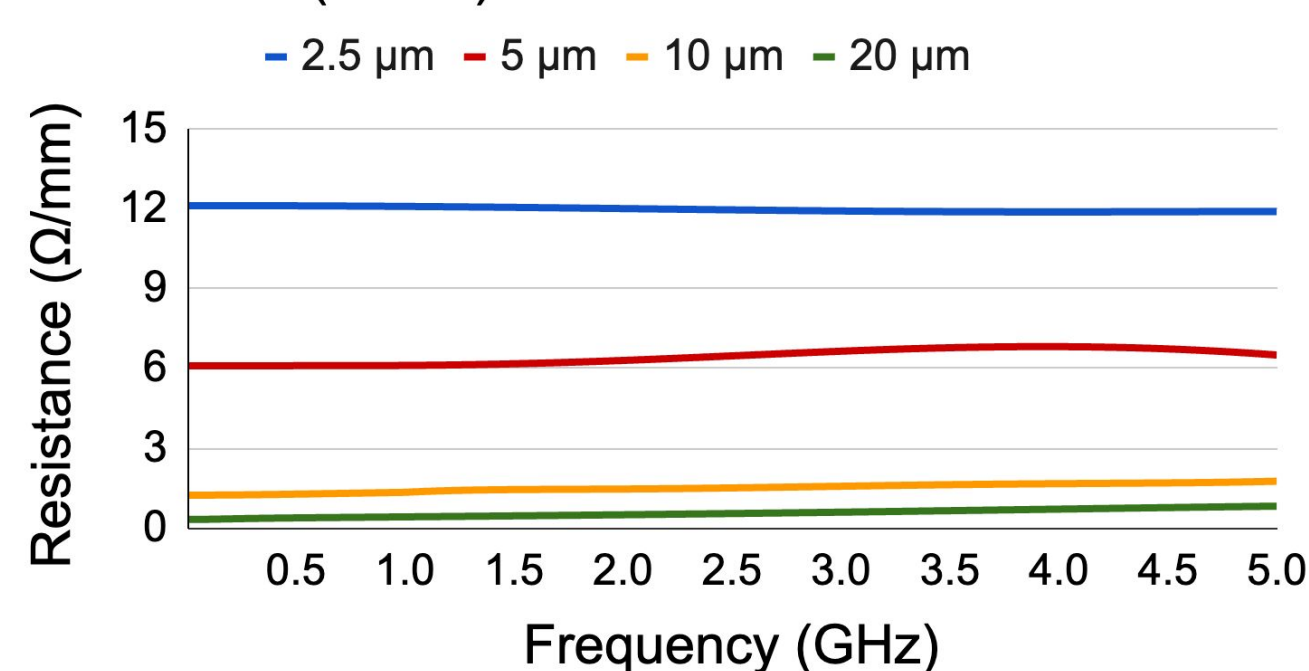
- comparison of hand-calculated RLGC results with converted z parameters of simple microstrip line to verify accuracy of code
- lengths: 1 mm, 10 mm, and 100 mm

$$\begin{aligned} \bar{T} &= \begin{bmatrix} \bar{A} & \bar{B} \\ \bar{C} & \bar{D} \end{bmatrix} = \begin{bmatrix} \bar{Z}_{11}\bar{Z}_{21}^{-1} & \bar{Z}_{11}\bar{Z}_{21}^{-1}\bar{Z}_{22} - \bar{Z}_{12} \\ \bar{Z}_{21}^{-1} & \bar{Z}_{21}^{-1}\bar{Z}_{22} \end{bmatrix} \\ M_1 &= (\bar{Y}\bar{X}^{-1} + \bar{X}\bar{Y}^{-1})(\bar{X}\bar{Y}^{-1} - \bar{Y}\bar{X}^{-1})^{-1} & M_2 &= (\bar{X}\bar{Y}^{-1} - \bar{Y}\bar{X}^{-1})^{-1} \\ X &= T_1 + T_2 & Y &= T_1 - T_2 & \bar{l} &= l_1 - l_2 \\ M_1 &= \begin{bmatrix} A_{M1} & B_{M1} \\ C_{M1} & D_{M1} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma\bar{l}) & 0 \\ 0 & \cosh(\gamma\bar{l}) \end{bmatrix} \\ M_2 &= \begin{bmatrix} A_{M2} & B_{M2} \\ C_{M2} & D_{M2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2}Z_0\sinh(\gamma\bar{l}) \\ \frac{1}{2}\sinh(\gamma\bar{l})Z_0^{-1} & 0 \end{bmatrix} \\ \gamma &= \frac{1}{\bar{l}}\cosh^{-1}(D_{M1}) & Z_0 &= \frac{1}{2}C_{M2}^{-1}\sinh(\gamma\bar{l}) \\ R_m(\omega) &= \text{Re}(Z_0\gamma) & L_m(\omega) &= \frac{1}{\omega}\text{Im}(Z_0\gamma) \\ G_m(\omega) &= \text{Re}(\gamma Z_0^{-1}) & C_m(\omega) &= \frac{1}{\omega}\text{Im}(\gamma Z_0^{-1}) \end{aligned} \quad [4]$$

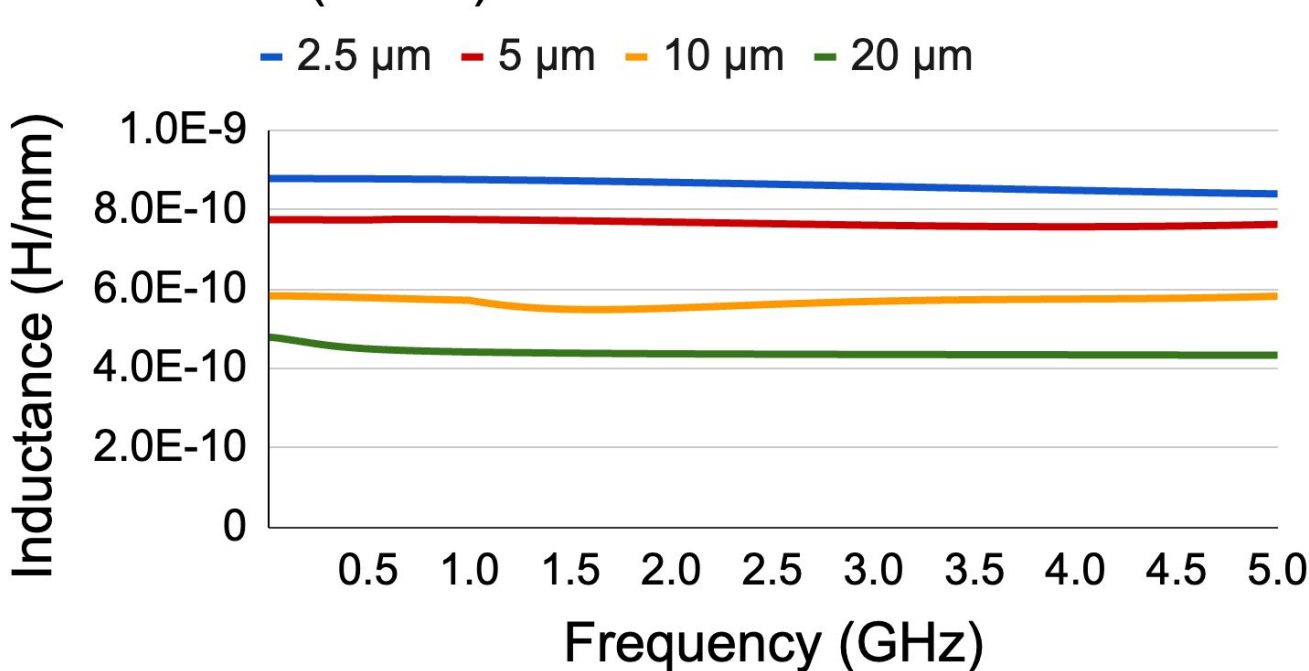
[4] M. K. Sampath IEEE-EPEP 2008

## RLGC Graphs for Each Line Width

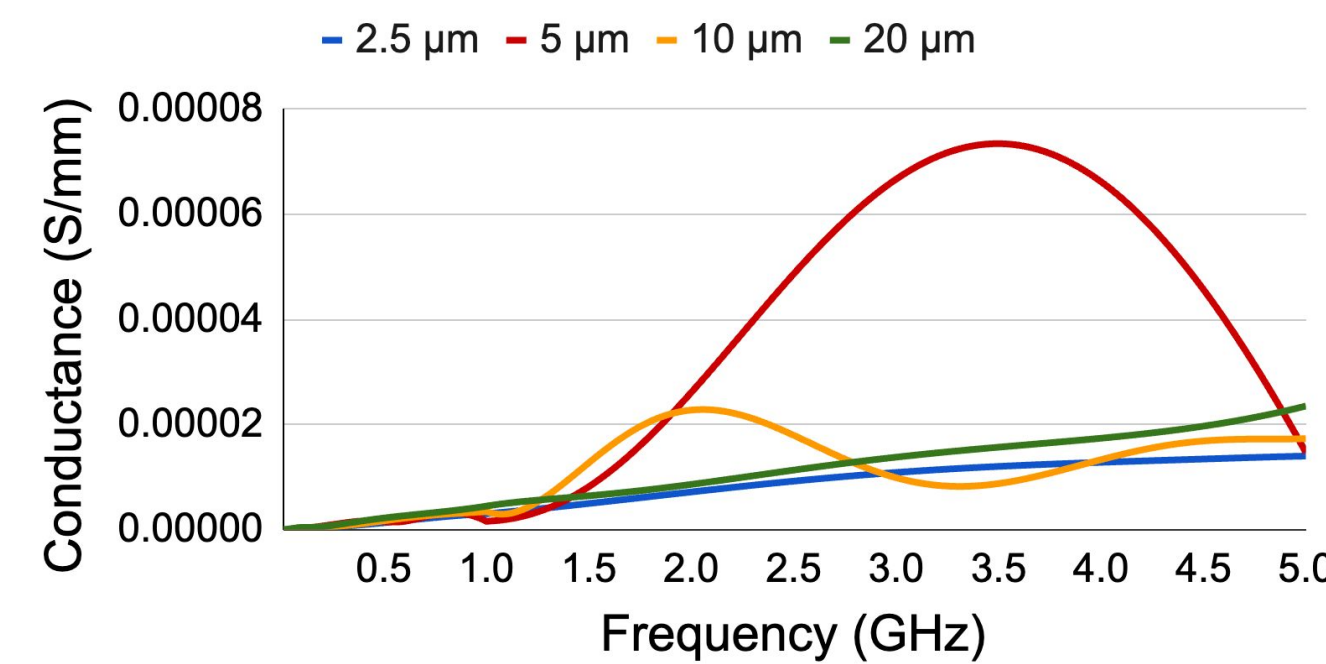
Resistance ( $\Omega/\text{mm}$ ) at Different Line Widths



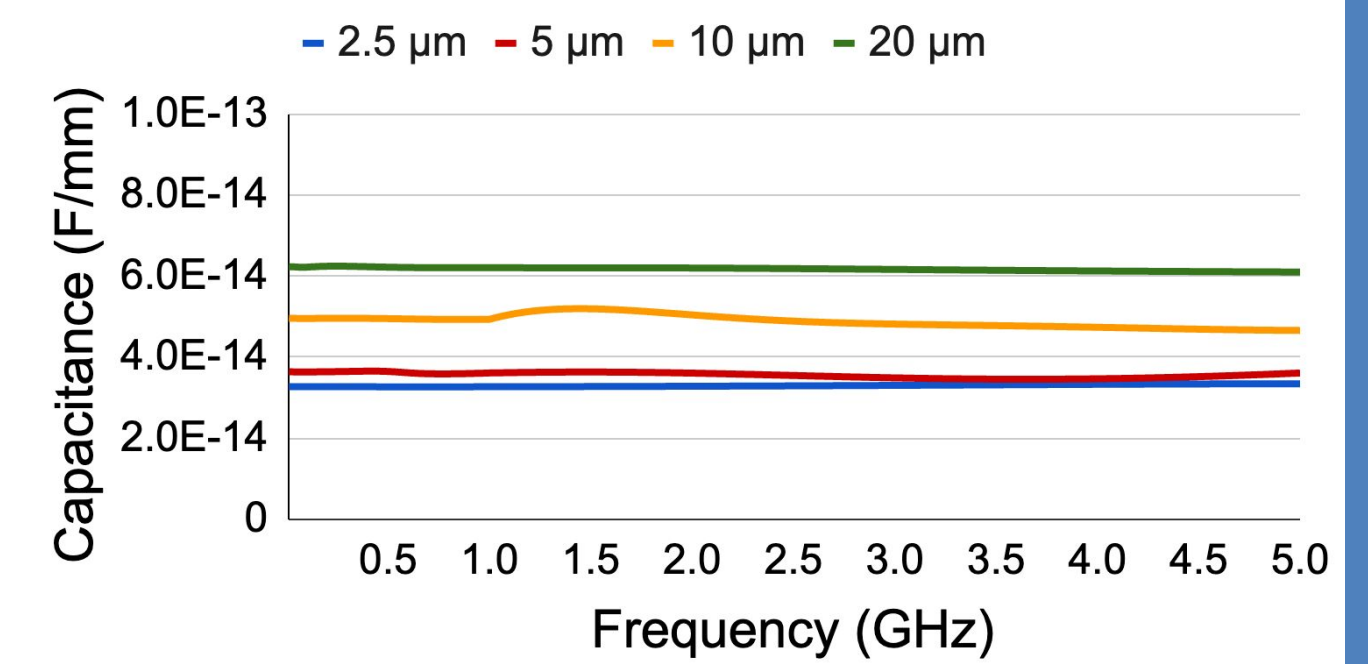
Inductance (H/mm) at Different Line Widths



Conductance (S/mm) at Different Line Widths



Capacitance (F/mm) at Different Line Widths

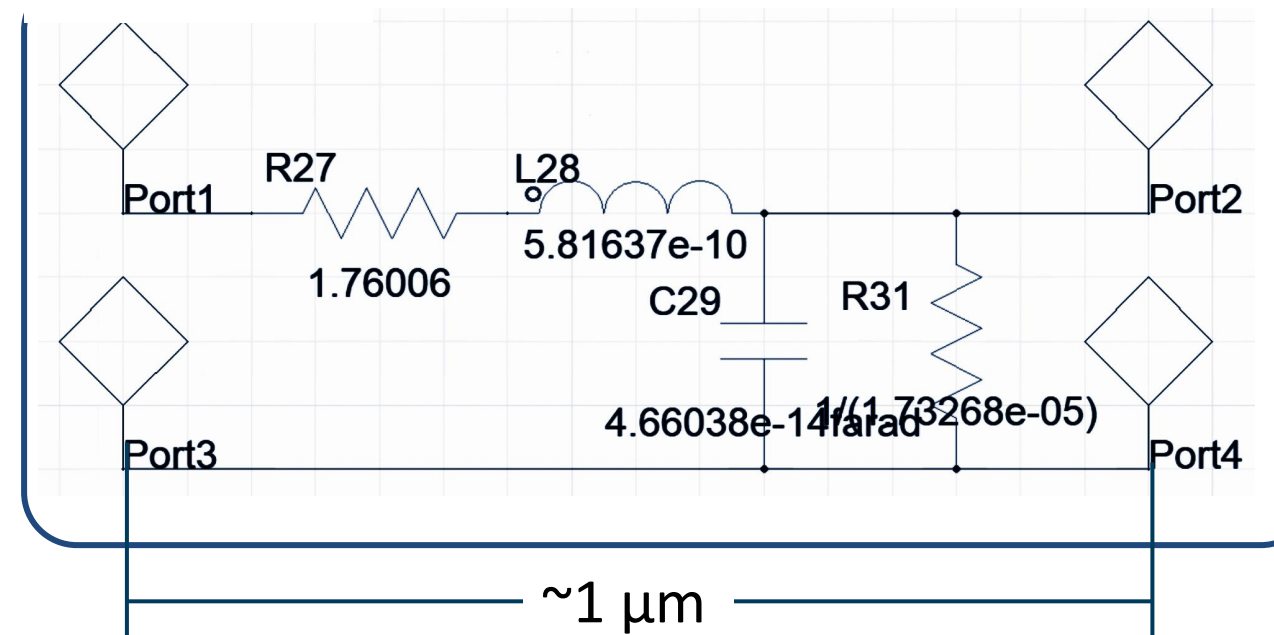


## RLGC Verification

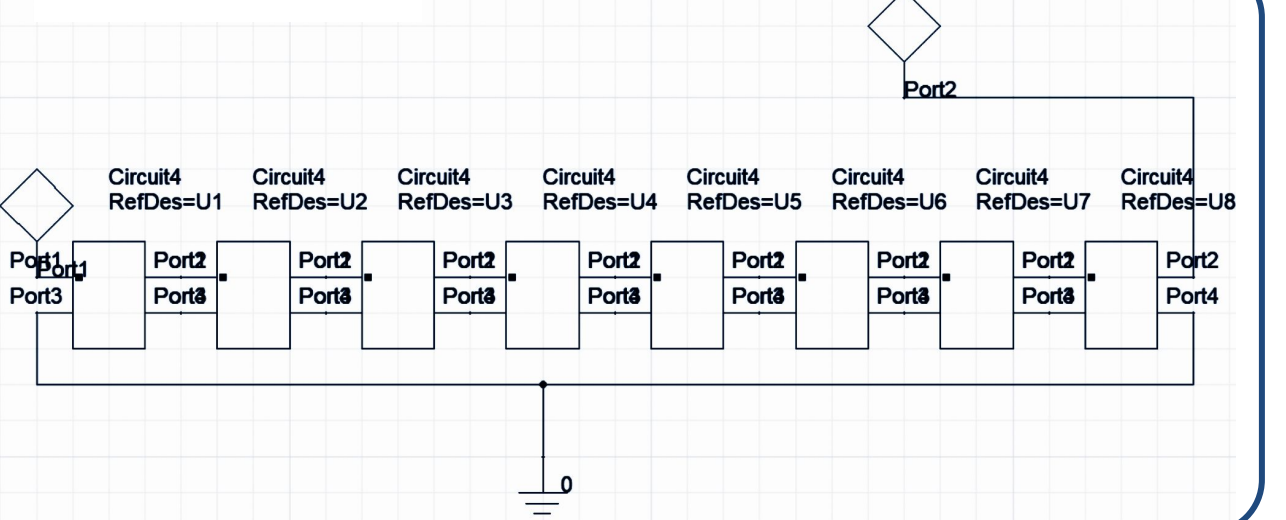
Confirming RLGC Simulation Results:

- Model of transmission line (~8  $\mu\text{m}$ ) with SPICE RLGC circuit in HFSS

Subcircuit



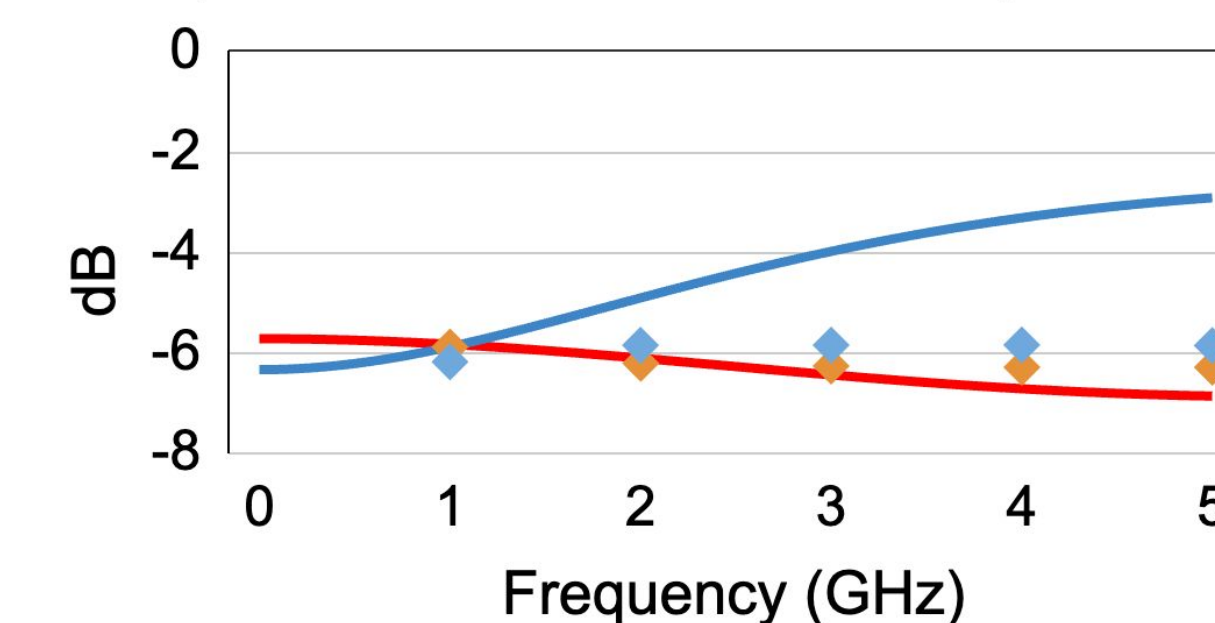
Full Circuit



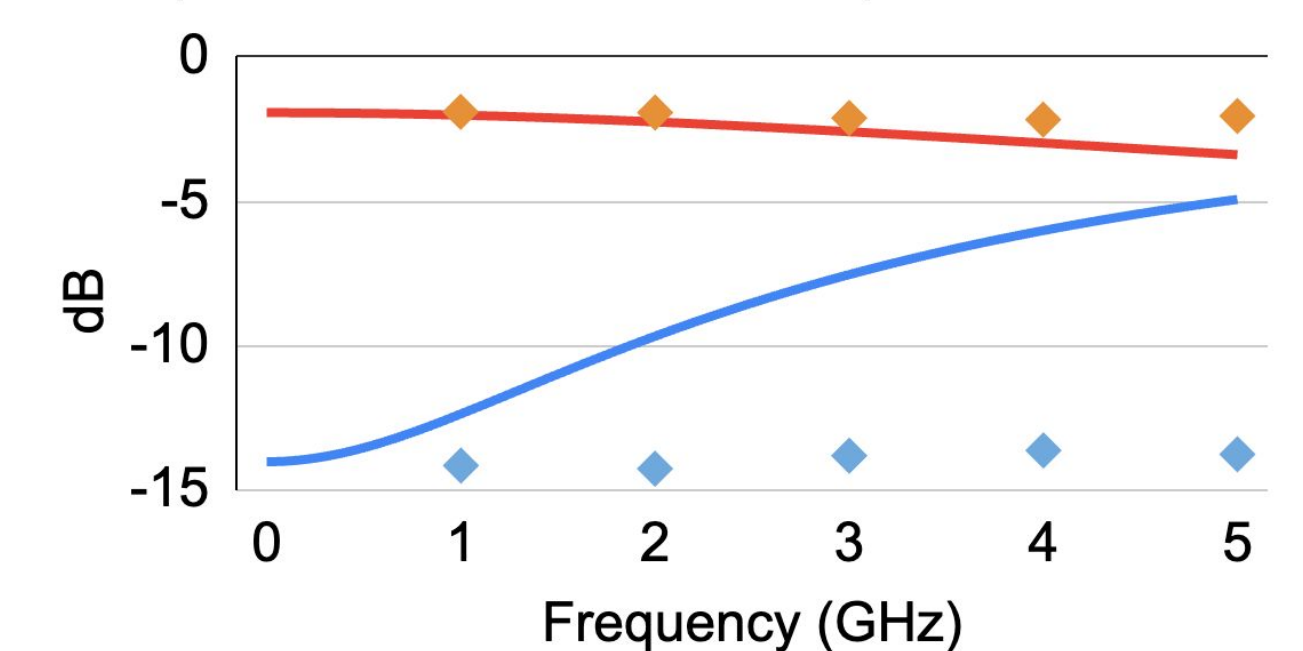
- Circuit solved for S-parameters at 1, 2, 3, 4, and 5 GHz for each wire width/height pair

## Simulation vs SPICE S-Parameters

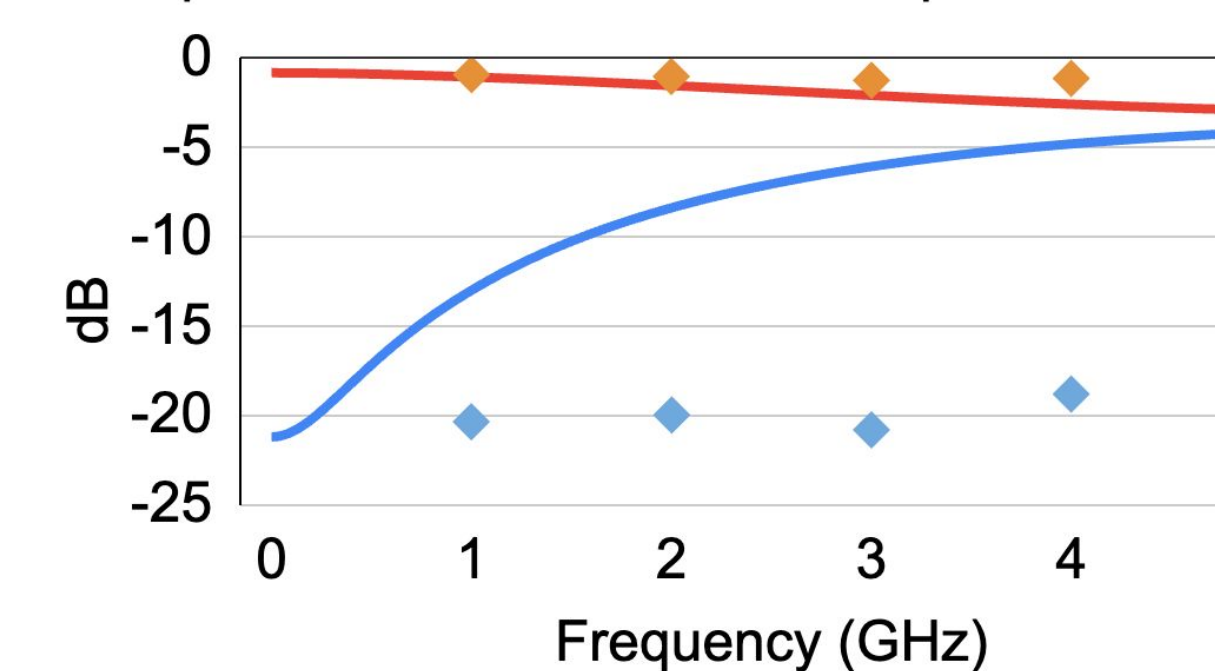
Comparison of S Parameters - 2.5  $\mu\text{m}$



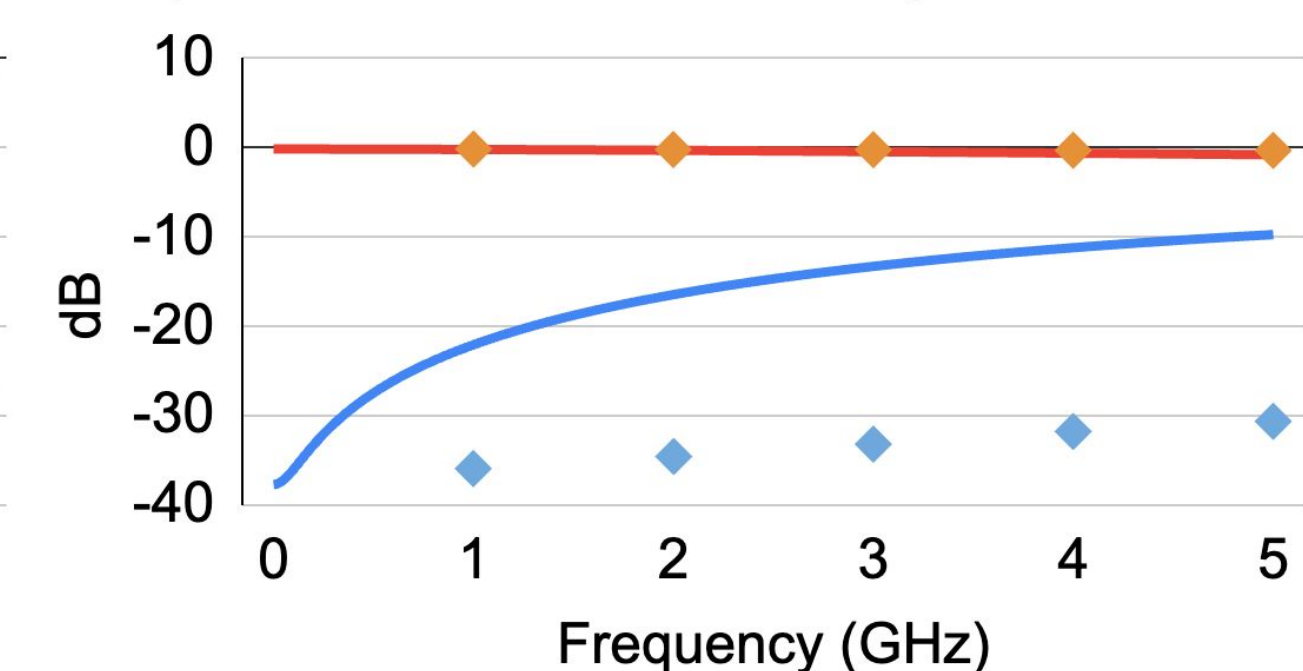
Comparison of S Parameters - 5  $\mu\text{m}$



Comparison of S Parameters - 10  $\mu\text{m}$



Comparison of S Parameters - 20  $\mu\text{m}$



- Insertion loss from the simulation is similar to the SPICE model for all line widths
- Reflection from simulation starts around the same value as SPICE model before large deviation

## Conclusions and Future Work

- The electrical parameters of the interconnects of FlexTrate are reasonably found through simulation and verified through circuits
- Will fabricate samples and measure RLGC experimentally for further verification
- Data is to be applied in Design Manual for FlexTrate

## Acknowledgements

This work is supported by the UCLA CHIPS consortium.