Demonstration of a Power-efficient and Cost-effective Power Delivery Architecture for Heterogeneously Integrated Wafer-scale Systems

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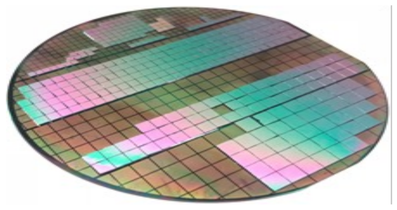
Introduction

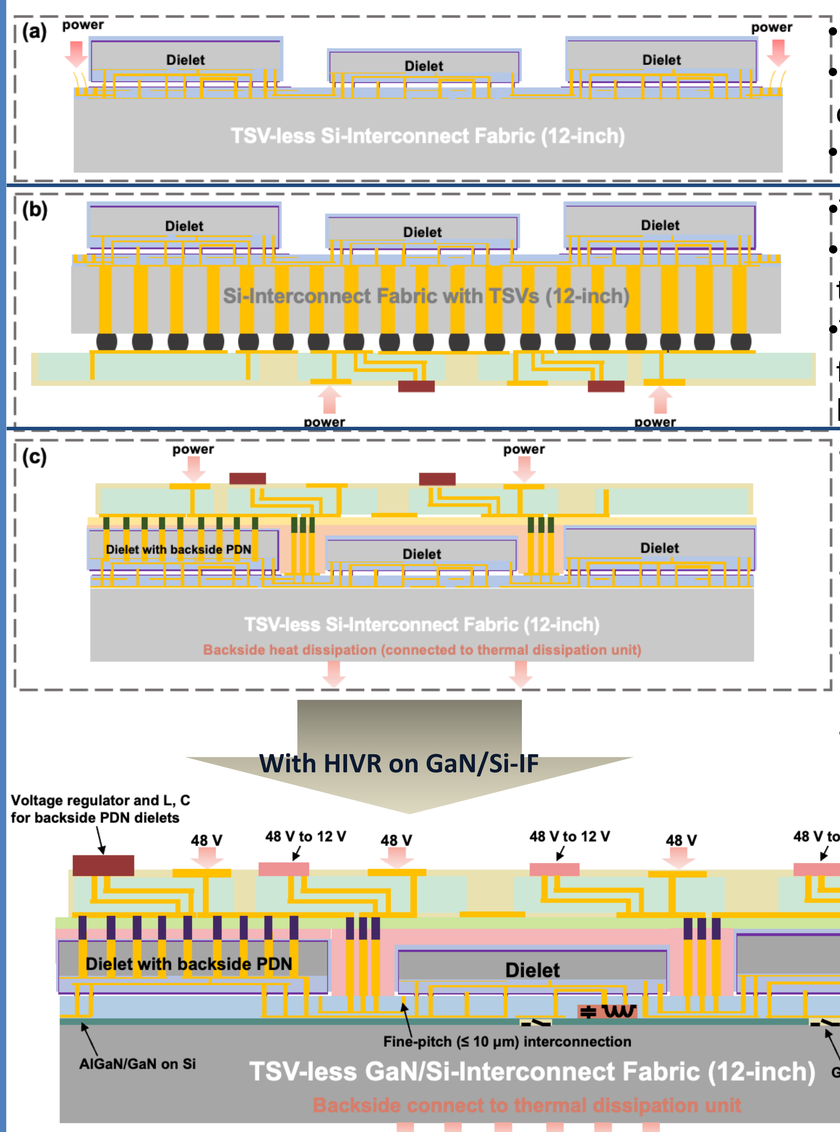
- Advanced packaging paradigms make enormous demands on uniform power delivery at multiple domain voltages. i.e., low PDN impedance at all frequencies.
- Delivering this power through TSVs/TWVs leads to complex and expensive processes and structures.
- In this work, we addressed these two problems through:
  - Front-side power delivery at high voltage via PCB-let
  - Granular step down at the dielet level using intimately connected GaN switching devices connected to control circuits on the chiplet



300 mm Silicon-Interconnect Fabric (Si-IF) based wafer-scale system [1]
Power: 40-60 kW

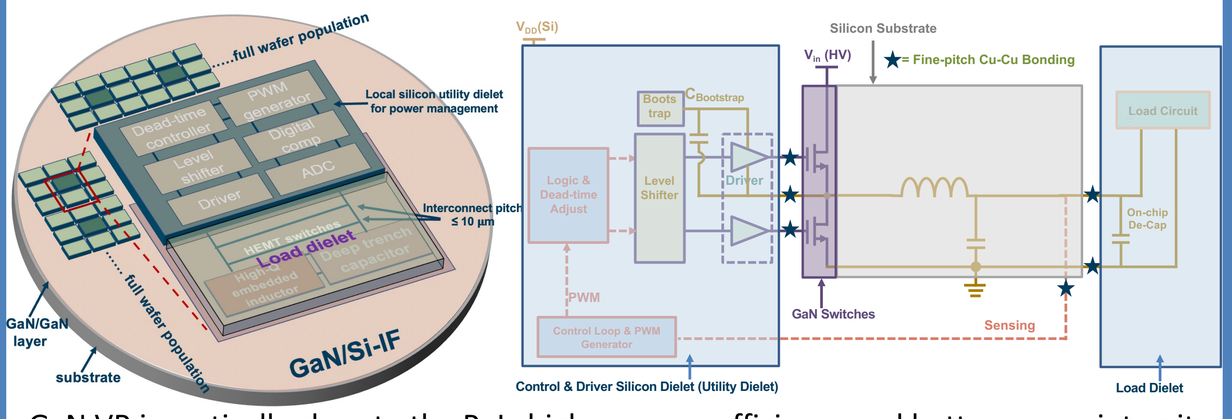
[1] S. Jangam and S. S. Iyer, "Silicon-Interconnect Fabric for Fine-Pitch (≤10 µm) Heterogeneous Integration," IEEE TCPMT, 2021.

Comparison of Different PDNs for Wafer-scale Systems



- Large power loss (I^2R)
- Large voltage drop (IR) – on-chip regulator is needed
- Large Ldi/dt noise
- TSVs are expensive.
- Interposers needs to be thinned limited by TSVs' AR.
- Thinned interposers are fragile and an additional level in hierarchy
- Through-polymer vias (TPVs) are easy and cheap to be fabricated.
- TSV-less Interposers do not require thinning.
- The entire Si substrate helps with heat dissipation.
- GaN integrated voltage regulator (IVR) is close to the point of load (PoL).

GaN/Si-Interconnect Fabric (GaN/Si-IF) with TSV-less Dielet-side PDN: a Compact Power Delivery and Interconnect Platform



- GaN VR is vertically close to the PoL: higher power efficiency and better power integrity
- Compact system: higher power density compared to 2D structure
- Fine-pitch dielet-dielet & dielet-converter bonding interconnection
- Divide PDN into three components: Passives in the silicon substrate; High voltage switches in GaN-on-Si; Control circuits in silicon chiplets

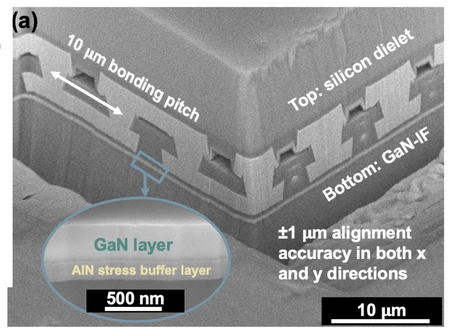
Demonstration of a TSV-less, Dielet-side Power Delivery Network

Integration Process Flow:

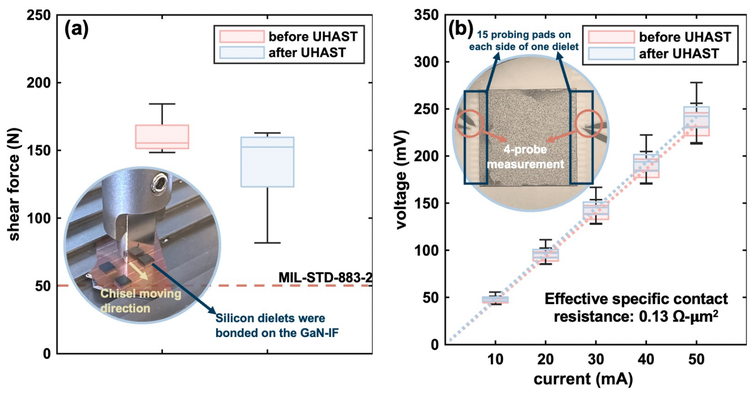
- **Thin dielet design, fabrication, and singulation; substrate design and fabrication; PCB design and fabrication**
- **Dielet-to-substrate Cu-Cu bonding**
- **Deposition of Al_2O_3 for encapsulation by ALD**
- **Deposition of SiO_2 for electrical isolation by PECVD**
- **Deposition and patterning of SU8 in between of dielets**
- **SU8 descum; SiO_2 & Al_2O_3 etching**
- **Cu bottom-up electroplating**
- **Solder paste screen printing and reflow**
- **Flux applying and PCB-to-wafer assembling**
- **Underfill applying (skipped in this work)**

Demonstration:

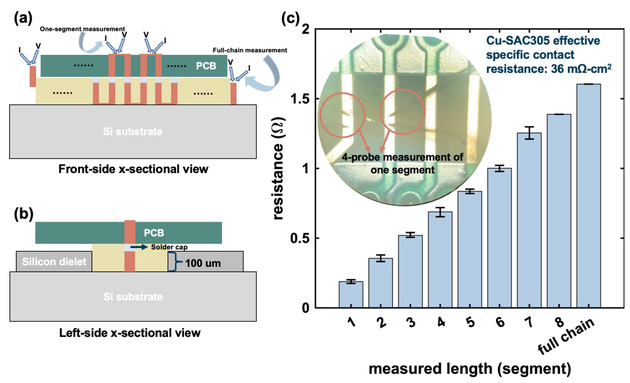
- **Preparation of GaN-on-Si wafers**
- **Fabrication of HEMT devices and their metal contacts (skipped in this work)**
- **Patterning of Cu wires and Cu bonding pillars by the Damascene process (<300℃)**
- **Dielet-to-GaN wafer assembly by Cu-Cu thermal compression bonding (<400℃, <150 MPa)**
- **Deposition of Al_2O_3 for encapsulation by ALD (<200℃)**



Mechanical and Electrical Results:



- A dielet-on-GaN/Si-IF vertical structure was demonstrated with a ≤ 10 µm Cu-Cu bond pitch
- A PCB-on-dielets-on-wafer 3D dielet-side PDN was demonstrated



- Meets the mil-spec shear test requirements
- Excellent Cu-Cu TCB specific contact resistance
- Unchanged GaN quality: XRD, Raman, and PL
- Passed the mil-spec temp/humidity reliability test

Summary

- Developed a low-cost, TSV-less dielet-side PDN architecture for wafer-scale and interposer power delivery.
- Demonstrated a dielet-on-GaN-on-Si platform for granular wafer-scale voltage regulation using Cu-Cu TCB at fine pitch.
- Proposed the three-way distribution of the PDN for high power efficiency and density.

Acknowledgement

This work was supported in part by the Semiconductor Research Corporation (SRC) JUMP ASCENT, SRC JUMP CHIMES, National Science Foundation (NSF), UCOP MRPI MRP-17-454999, and the UCLA CHIPS consortium.

2023 UCLA CHIPS Workshop
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