More-than-Moore 3D Integration With Low Thermal Budget

Han-Wen Hu, Demin Liu, Yi-Chieh Tsai, and Kuan-Neng Chen*,
National Yang Ming Chiao Tung University, *Email: knchen@nycu.edu.tw

Introduction

Background

- 3D integration provides accommodation of more transistors on the same footprint without the need to shrink transistor sizes.
- Controlled thermal budget is the key to vertical integration of multifunctional devices without performance degradation.

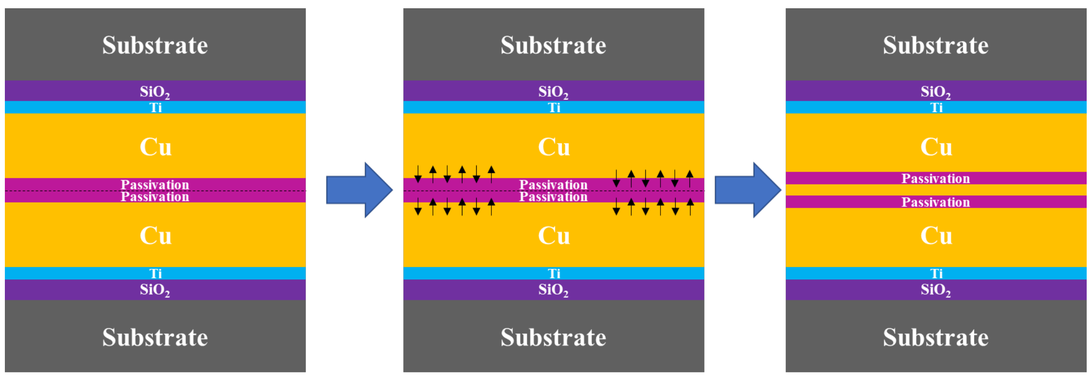
Accomplishments

- Passivated-Cu/SiO_2 hybrid bonding was developed for chip stacking with low thermal budget (120 °C, 1 min).
- Location-controlled-grain (LCG) technique was developed to realize monolithic 3DIC with controlled thermal budget.

Attribute	Cu/SiO_2 Hybrid Bonding	Monolithic 3D
Channel Quality	**Higher**	Lower
Stacking Thickness	Thicker	**Thinner**
Alignment Precision	Lower	**Higher**
Applicability	**Higher**	Lower
Target I/O Pitch	1-10 μm	**< 1 μm**
Thermal Challenges	Bonding temperature	Process for active tiers

Passivated-Cu/SiO_2 Hybrid Bonding

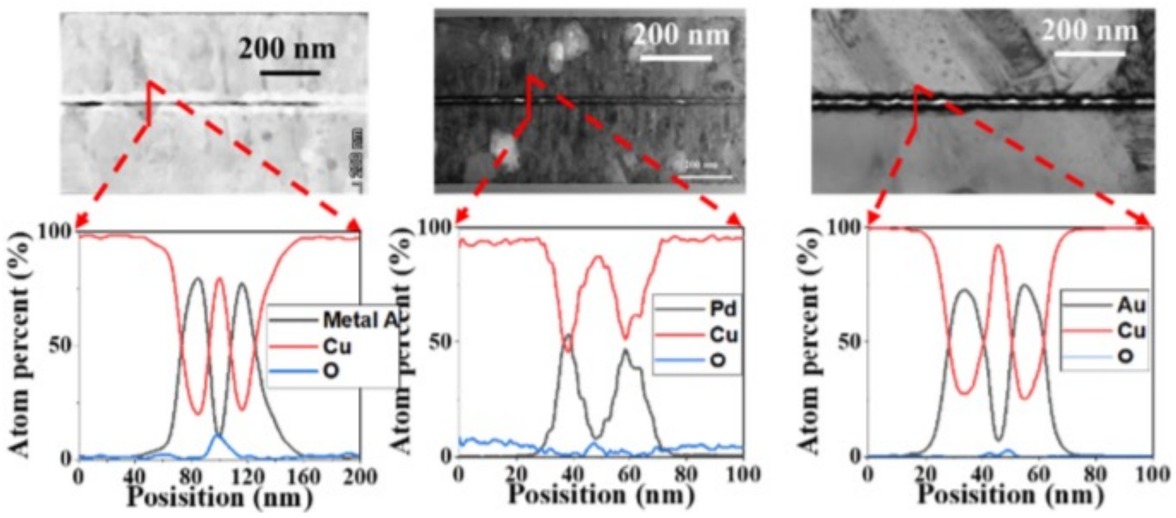
Mechanism of passivated-Cu bonding



(1) Full contact (2) TCB (3) Jointed

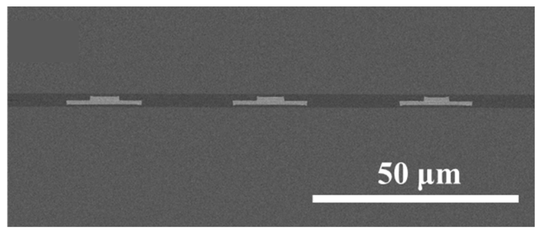
- Candidates of passivation includes 10 nm Au, Pd, or Ag.
- Cu can diffuse through passivation to achieve Cu-Cu bonding

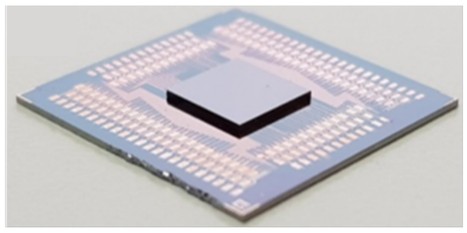
Analyses of passivated-Cu bonding at 150 °C

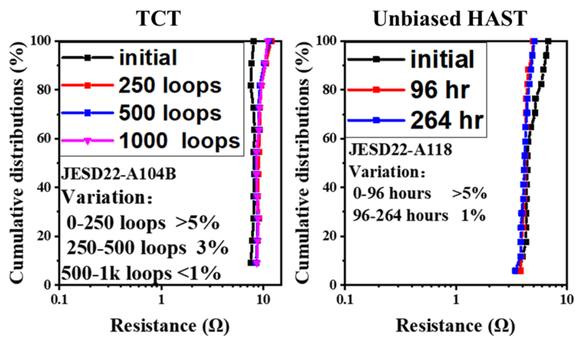


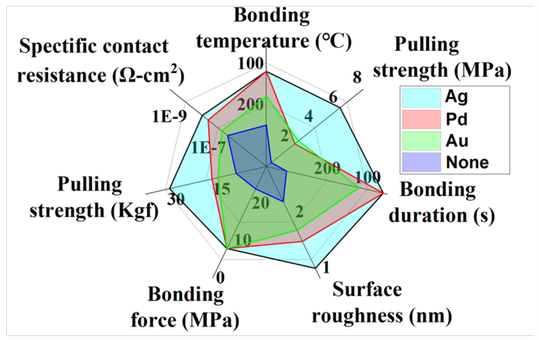
- Passivated-Cu bonding at 150 °C was demonstrated and analyzed by SEM, TEM, and EDX.

Low temperature passivated-Cu/SiO_2 hybrid bonding





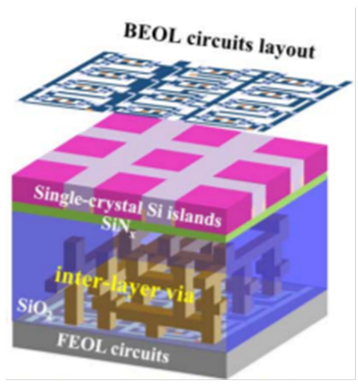


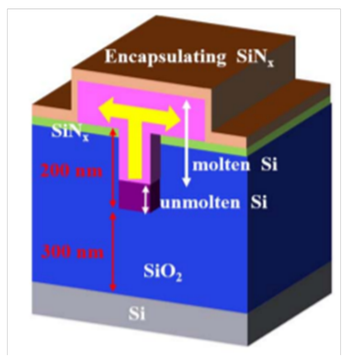


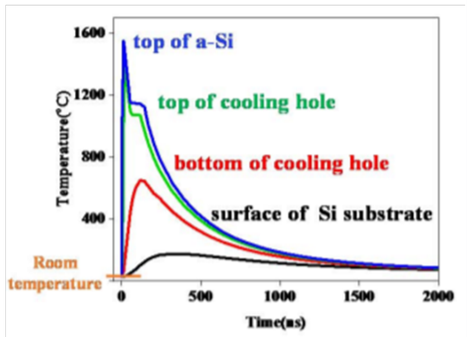
- Passivated-Cu/SiO_2 hybrid bonding can be achieved with low thermal budget (120 °C, 1 min) and excellent reliability.

Monolithic 3DIC based on LCG technique

Controlled thermal budget using LCG technique

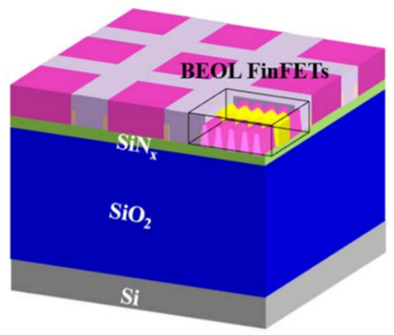


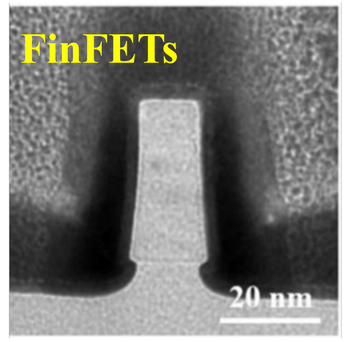


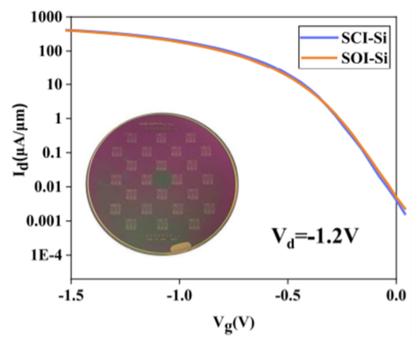


- Based on LCG, single-crystal Si islands were achieve, and the temperature of bottom layers can maintain lower than 200 °C.

Single-crystal Si islands for fabrication of FinFETs







- For single-crystal Si islands, the random grain-boundary effect can be prevented to provide high performance FinFETs.

Conclusions

- Advanced 3D integration technologies with low thermal budget were developed, including passivated-Cu/SiO_2 hybrid bonding and LCG-based monolithic 3DIC.
- Our recent 3D integration: 2019 IEDM, 2020 IEDM, and 2020 VLSI.
- LCG-based monolithic 3DIC for Ge FinFETS will be published in 2021 IEDM.