A Nonvolatile Embedded SRAM based on CTT

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Introduction

Background:

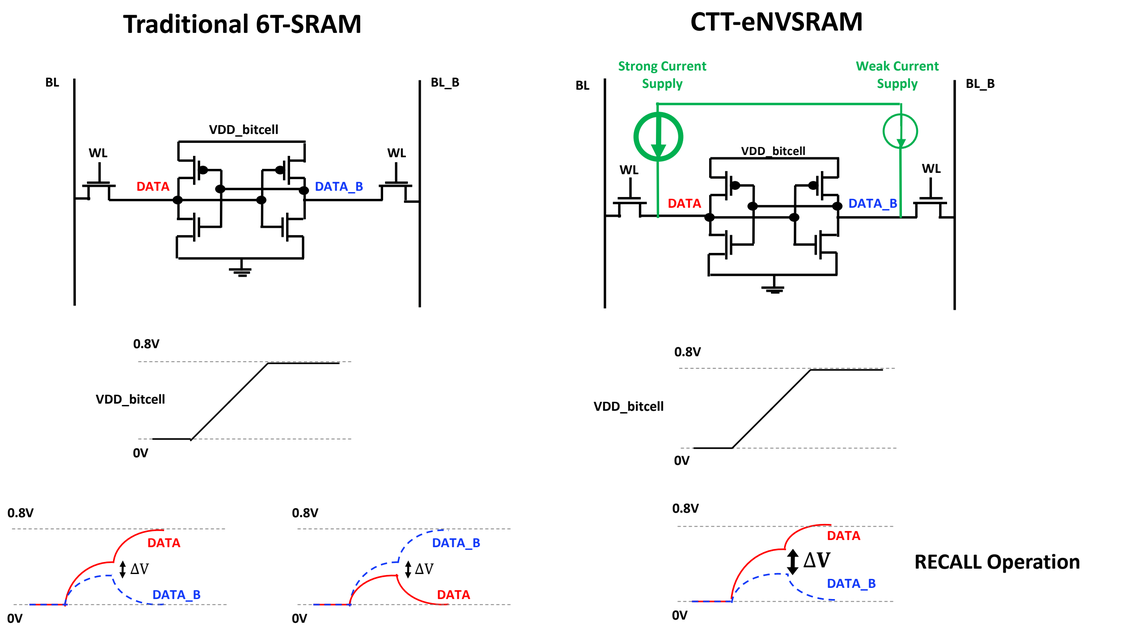
- In traditional SRAM, to prevent data loss: Supply-voltage > Vmin
- Problem: High leakage and static power consumption
- Possible solution: Non-volatile memories
- Limitations of existing non-volatile memories:
  - Require special processes that are not usually CMOS logic compatible.
  - Some of them cannot be implemented in advanced nodes.
  - May need special operating conditions (such as high voltage).
  - When NVM is not embedded, data movement causes extra delay.

Our Solution:

- Designed and taped-out an embedded nonvolatile SRAM (CTT-eNVSRAM) to address the above limitations.
- In this design, when memory is idle, VDD can be turned off to eliminate the leakage power.

Design Overview

Comparison of traditional 6T-SRAM vs. CTT-eNVSRAM During Power-up:

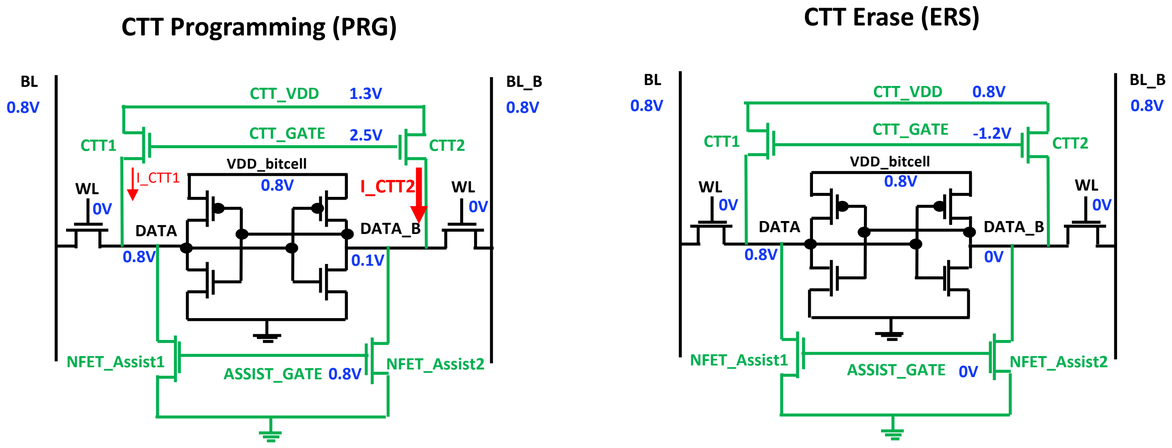


In traditional SRAM, during power-up DATA/DATA_B flip into random states.

In CTT-eNVSRAM, during power-up DATA/DATA_B flip into their last states before power-down.

How do we Create the Strong and Weak Pull-ups in CTT-eNVSRAM?

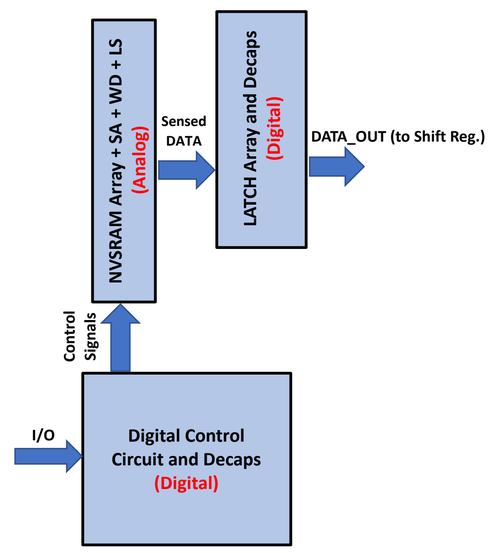
- Before VDD is turned off, we create a nonvolatile mismatch in the bitcells.
- The mismatch is stored as different amounts of ΔV_{th} in two CTTs that are connected to DATA and DATA_B using CTT Programming (PRG) [1].



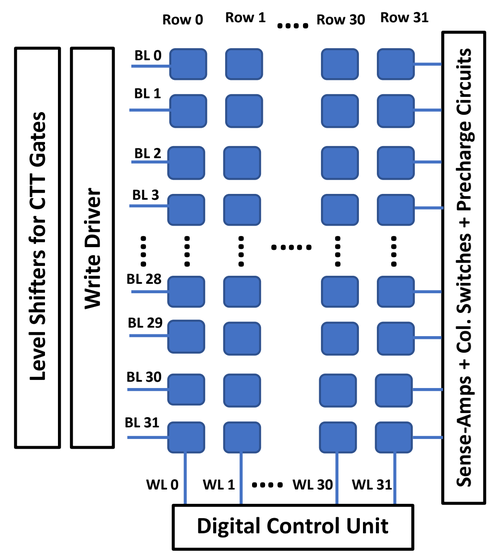
- In the above scenario, the original DATA is 0.8V and DATA_B is 0V.
- CTT2 is programmed more than CTT1, due to having larger V_{GS} and V_{DS} during PRG.
- Therefore, CTT2 becomes a weaker pull-up during power-up and the original DATA/DATA_B are restored (RECALL).
- After RECALL, we erase CTTs to reduce the Vth mismatch between them, so we can program them again in the next cycle.

Tapeout Summary

Digital and Analog Blocks



1Kb Array and Peripheries



Design Layout:

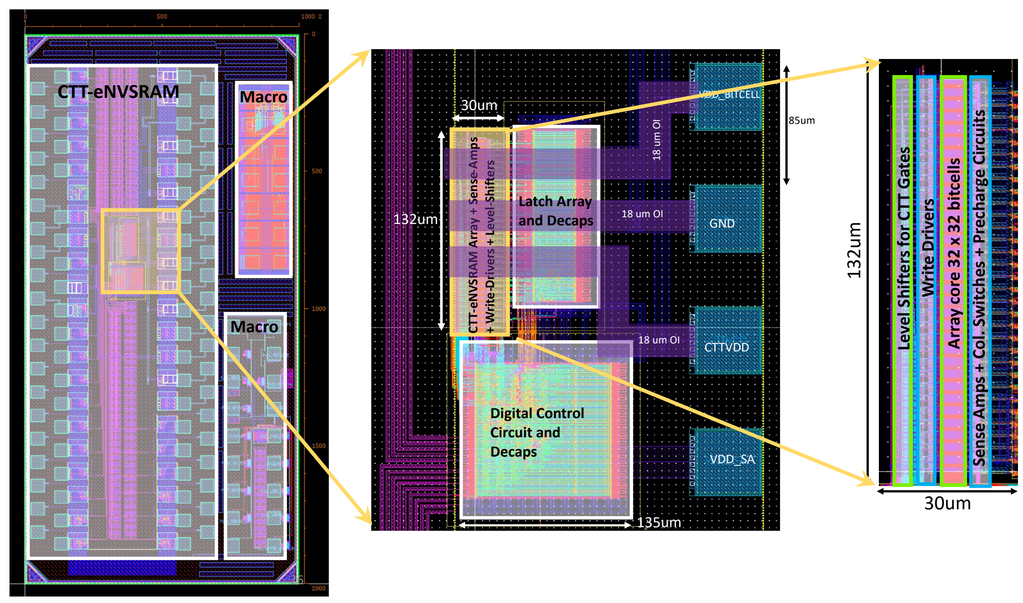


Table of Comparison:

Volatile/Nonvolatile	Volatile	Nonvolatile	Nonvolatile	Nonvolatile	Volatile + Nonvolatile	Volatile + Nonvolatile
Reference	**GF- SRAM IP**	**IMW-2017 [6]**	**ISSCC-2020 [7]**	**ISSCC-2019[8]**	**NVSMW-2008 [9]**	**This work**
Technology	SRAM: 22FDSOI CMOS (GF)	eFLASH: 40nm CMOS (GF)	MRAM: 22nm CMOS (TSMC)	ReRAM: 22nm FinFET (Intel)	SONOS-NVSRAM: 130nm CMOS (Cypress)	CTT-eNVSRAM: 22FDSOI CMOS (GF)
Memory size	4Kb	20Mb	1Mb	3.6Mb	4Mb	1Kb
Cell Size (um²)	0.11 (HD), 0.15 (LV) (SRAM only)	Not reported* (NVM only)	0.0456 (NVM only)	0.1 (NVM only)	Not Reported (6T NMV+6T SRAM)	0.858 (4T NVM+ 6T SRAM)
Average read current/CLK_freq	5.2uA/MHz (peak)	53uA/MHz	0.8uA/MHz	1.4uA/MHz	61mA/MHz	5uA/MHz (includes pads+ ESD)
Read Time (nsec)	0.23ns	8ns	10ns (decoder excluded)	5ns	15-25ns (Read from SRAM) 20ms (Recall from NVM)	0.8ns (Read from SRAM) 10ns (Recall from CTT)
Stand-by power	7.7uW (VDD=0.8V)	712uW	140uW	Not Reported	Not Reported	9uW (VDD=0.8V)
PRG Current	N/A	1mA for 20Mb	10mA for 1KBytes/ms	Not Reported	Not Reported	64mA for 64 bits/ms
PRG Time	N/A	10usec (for 8 bits)	~80ns	10us	1ms	1ms (for 64 bits)
PRG Voltage	N/A	10.5V	2V	Not Reported	11V	CTT-Gate: 2.5V, CTT-VDD: 1.3V
PRG Energy-per-bit	N/A	105pJ	2.5nJ	0.1pJ	10nJ	1.3uJ
VDD (V)	0.8V	2.5V	0.8V	0.7V	2.7V-5.5V	0.8V
Extra mask required?	No	Yes	Yes. 2-5 BEOL masks	Yes. BEOL at Via2	Yes. 2-3 extra masks	No
Other Limitations	Volatile	>10V PRG/ERS voltage	Extra Shield Required	Resistance variability	None	None
Data transfer method to SRAM	N/A	Bus required	Bus required	Bus required	No bus required (All at once)	No bus required (All at once)

* TSMC eflash Cell Size: 0.17um²

Summary

- Designed an embedded non-volatile SRAM using CTT.
- This design is implemented in a CMOS logic process, with no additional fabrication steps.
- CTT-eNVSRAM can be used as both regular SRAM and an embedded-NVM.
- Potential Applications: Systems that have a low power budget, such as IoT sensors, implantable medical devices, and intermittent computing.
- The design has been submitted for fabrication in GF 22FDX and will be back in December 2021.

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We would like to thank GlobalFoundries for fabrication of the chip.

References:

1. F. Khan, *et. al*, "Charge Trap Transistor (CTT): An Embedded Fully Logic-Compatible Multiple-Time Programmable Non-Volatile Memory Element for High-k-Metal-Gate CMOS Technologies," IEEE Electron Device Letters, Jan. 2017.