Feasibility studies and optimization of μ-channel cooling for 3D IC

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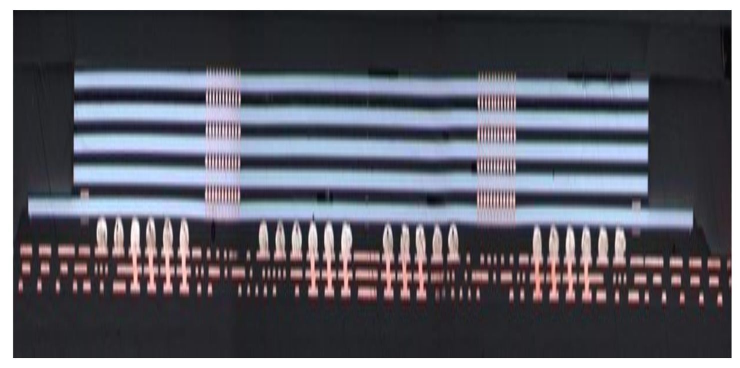
Motivation

- **3-Dimensional Stacking** is one of the key advanced packaging approaches
  - This work focuses on 3D IC
- **Low power 3D stacks** for memory applications
  - Successfully deployed in last decade (HBM, HMC, NAND) supported by TSVs



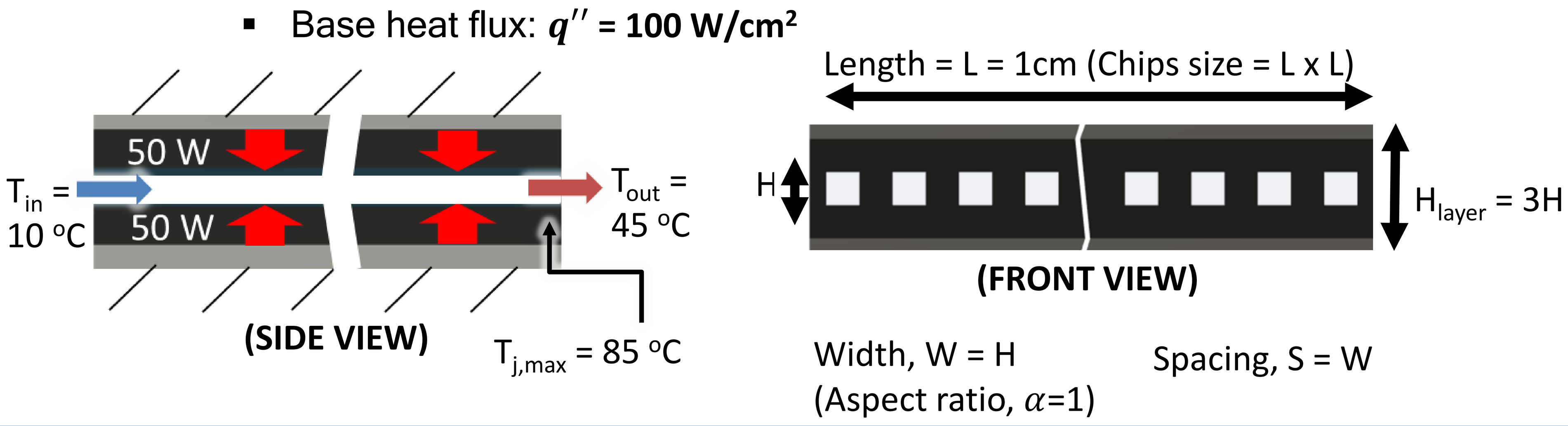
HMC stack (Courtesy: Micron/IBM)

- **High-power 3D stacks** with heterogeneous integration are being developed:
  - High temperatures, thermal gradients and cross-talk lead to reliability issues
  - Internal layers require direct cooling path
- **Micro(μ)-channel cooling** with water is the primary candidate:

Q. What is the minimum μ-channel height (H) and layer height (H_{layer}) needed to support it?

Simplified μ-channel analysis with Jupyter

- **Single adiabatic layer**: All heat produced within the layer needs to be taken out by the μ-channel
  - Base heat flux: q'' = 100 W/cm²

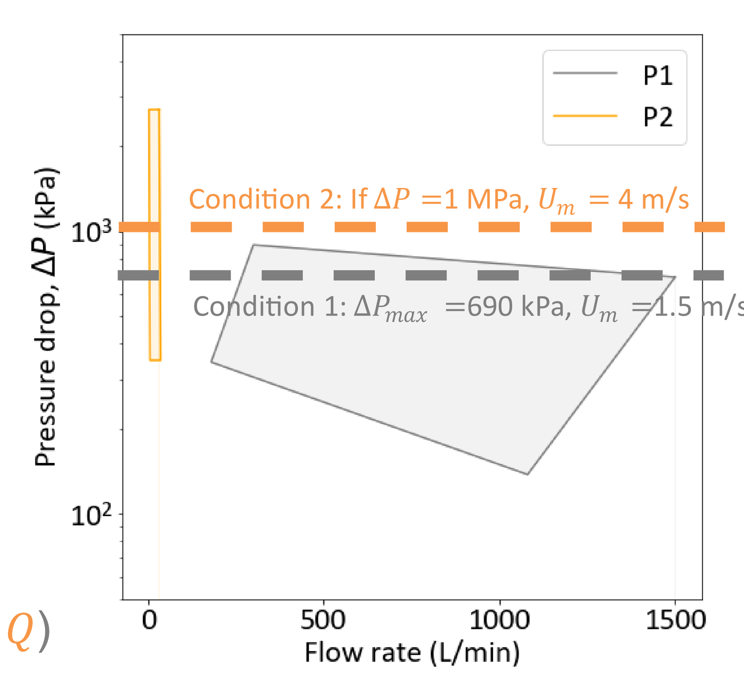


Flow considerations

- **Fully Developed laminar flow:**
  - Caloric limit (sensible heating): $Q_{min} = \frac{q'' L^2}{\rho C_p (T_{out} - T_{in})}$; $U_m = \frac{Q_{min}}{WH}$
  - Pressure drop: $\Delta P = 2 * (fRe(\alpha)) * \frac{\mu u_m L}{D_h^2} + K(\alpha) * \frac{\rho u_m^2}{2}$ +40 kPa
  - Heat Transfer limit: $q''_{max} = \bar{h} A_s (\overline{T_j} - \overline{T_m}) * \frac{N}{L^2} > q''$ (100 W/cm²)

Operational considerations

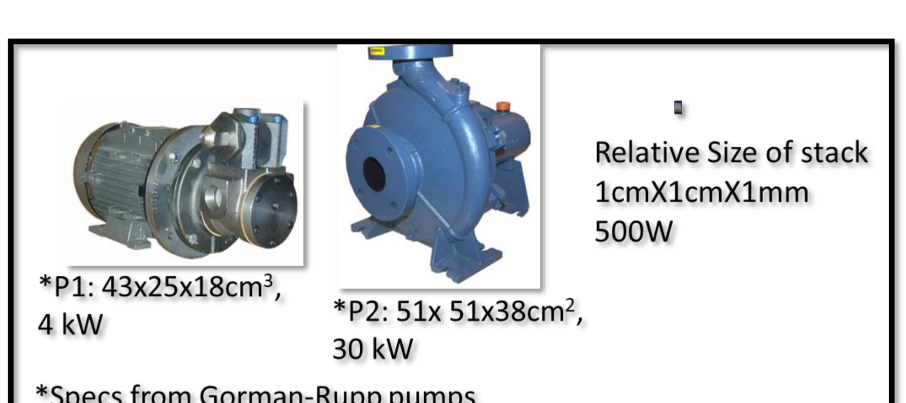
- **Operational limits:** Temperature, pressure drop and velocity limits
  - Examples:
    1. Condition 1 (ASHRAE W4#)
    2. Condition 2 (Hypothetical)
- **Pump curves:** Decides number of pumps and pumping power necessary
  - P1: Centrifugal (Low ΔP, high Q)
  - P2: Positive displacement (High ΔP, low Q)



#Thermal Guidelines for Data Processing Environments (3rd Edition), Table 3.1

Electrical and packaging co-design constraints

- **Fabrication limits:**
  - Examples - $H < H_{max}$, $\alpha < 10$
- **3D stack constraints:**
  - Form factor (<1 mm high)
  - TSV aspect ratio and placement
  - Coupling of μ-channel to pump
  - Reliability and cost

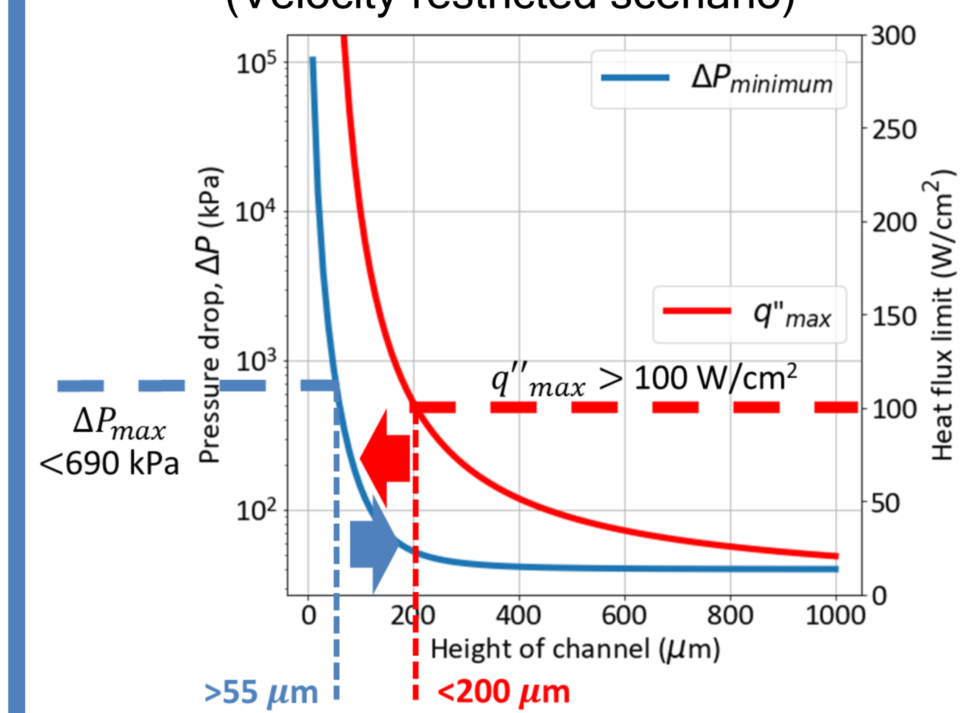


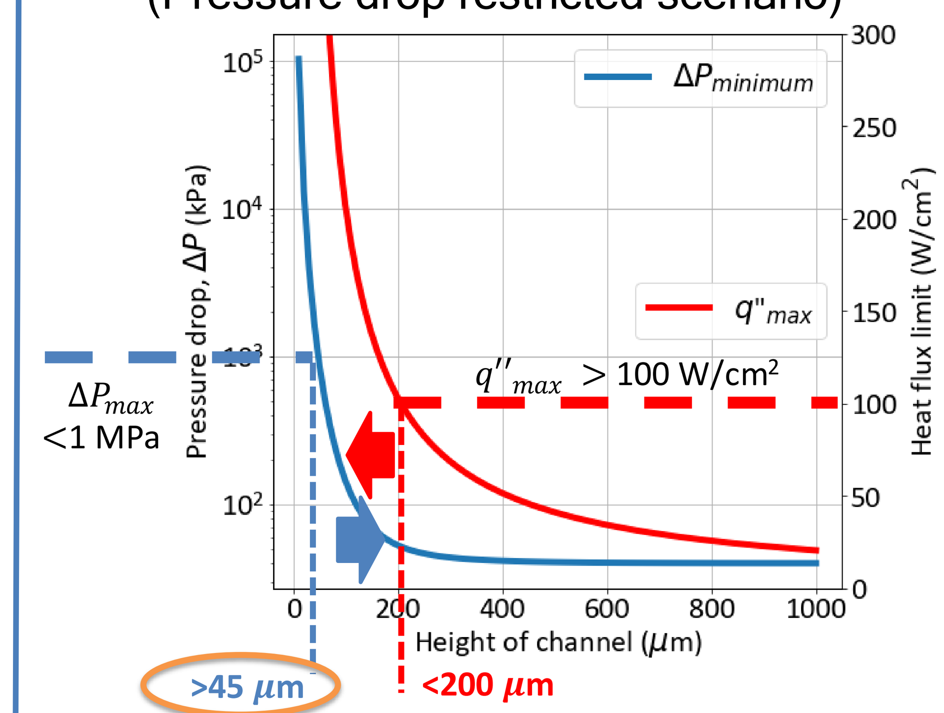
Optimization under sample conditions

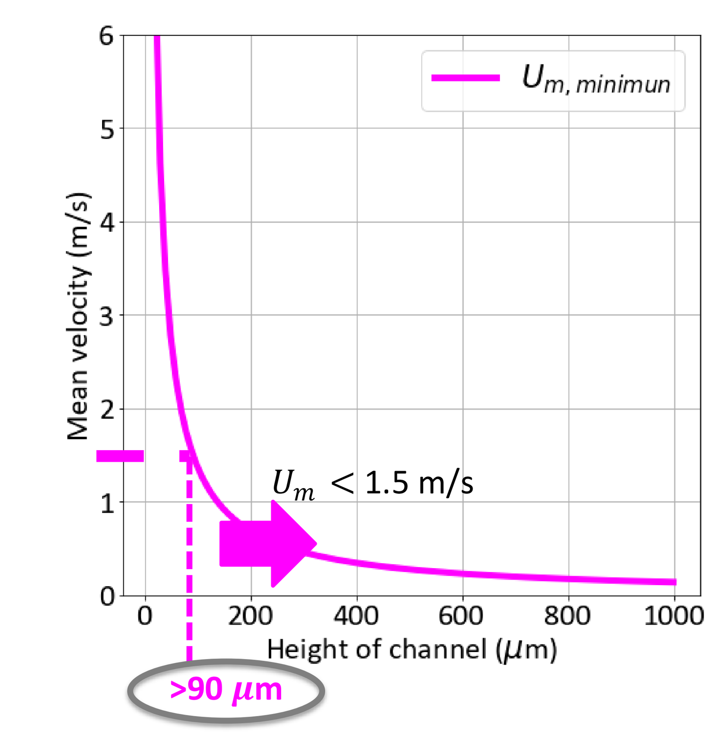
Operating condition 1 | Operating condition 2

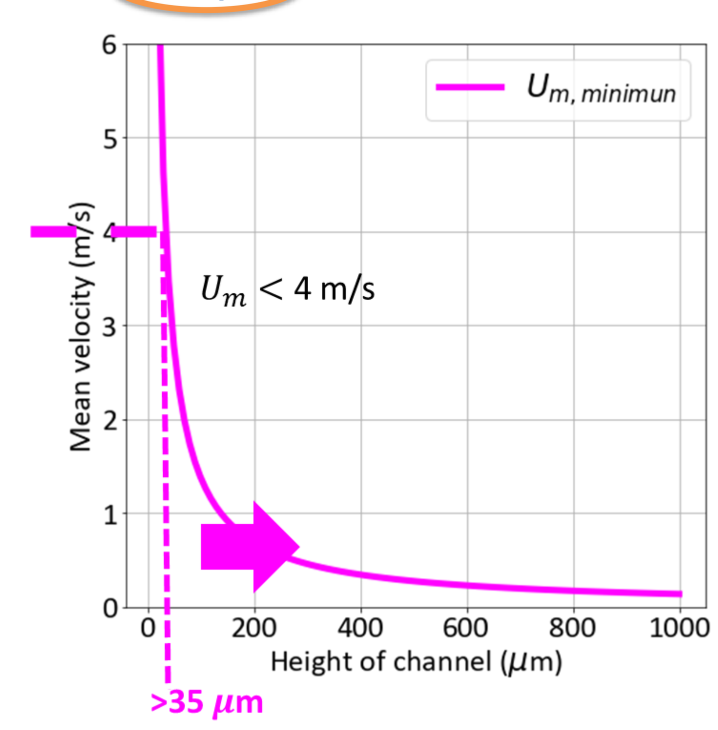
- Application of flow limits to identify allowable heights

(Velocity restricted scenario) | (Pressure drop restricted scenario)

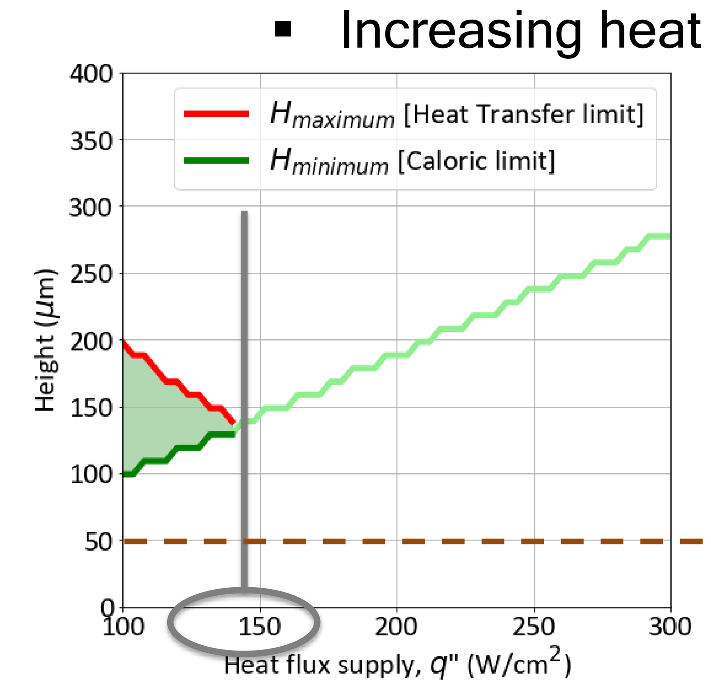




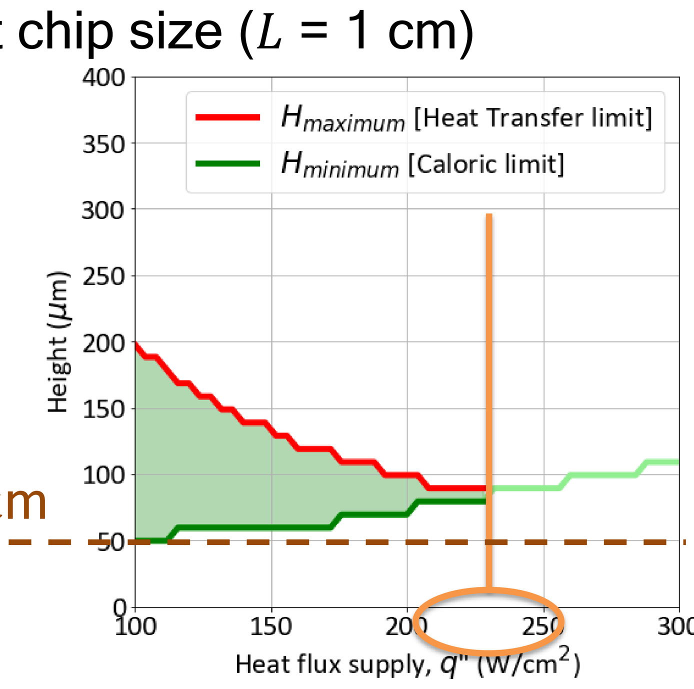




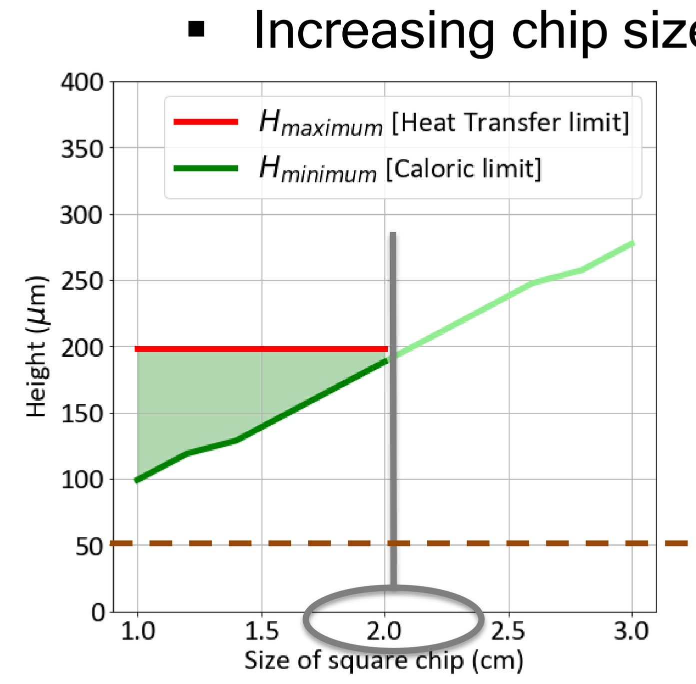
- Increasing heat flux at constant chip size (L = 1 cm)



$H < 50\ \mu m$, $H_{layer} < 150\ \mu m$



- Increasing chip size at constant heat flux (q''= 100 W/cm²)



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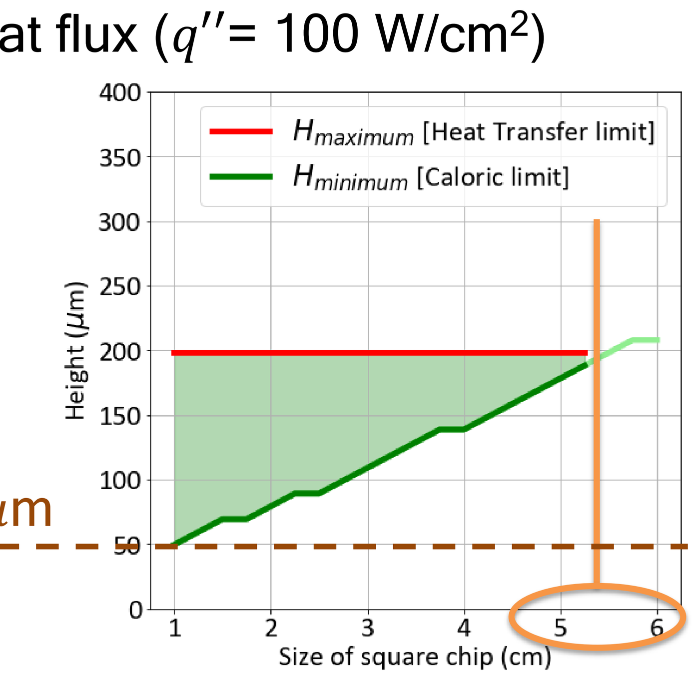

Conclusions

- **Micro(μ)-channel cooling for 3D IC** presents a formidable challenge when all dies are high-power (>100 W/cm²)
  - Key limitation is the channel height required to sustain high flow rates with practical pressure drops (<1 MPa)
  - Significant temperature gradient within 1 cm die length
- Experimental studies needed for reliability constraints for high-pressure flow within stack
- If the maximum layer height is restricted to 150 μm:
  - No operating points for heat flux, $q'' > 100$ W/cm²

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