Fine-Pitch (≤10 μm) Nb-based Superconducting Silicon Interconnect Fabric (Superconducting-IF) for Large-Scale Quantum System Application

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1. Motivation & background

- **Two-million** cabling & I/O count will be required for large-scale quantum systems (one million qubits) with current μWave system setup and using solders for integration.
- **Four-order** magnitude of reduction in cabling & I/O count can be achieved through multiplexing and compact integration adopting Superconducting-IF.

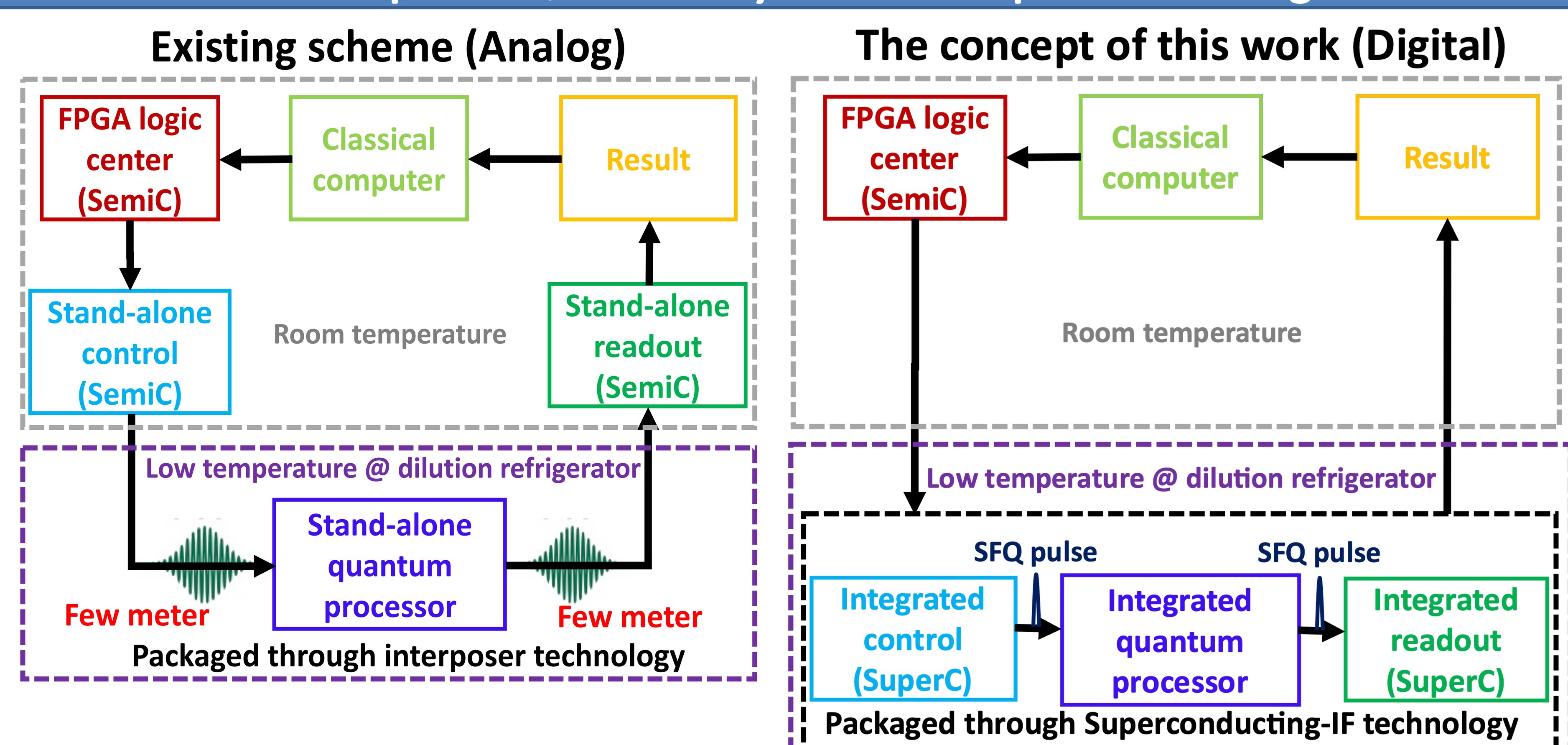
Rent's rule for quantum circuits [1]

Qubit count	μWave control	SFQ control
100	200	31
1,000	2,000	76

Compared to Si-IF technology, there are four main changes:

- Interconnect material: niobium (Nb)
- Nb passivation layer: iridium (Ir)
- Au-Au bonding to adhere superconducting dies
- Low-temperature (< 150℃) fabrication process

2. Concept for Quantum System On Superconducting-IF

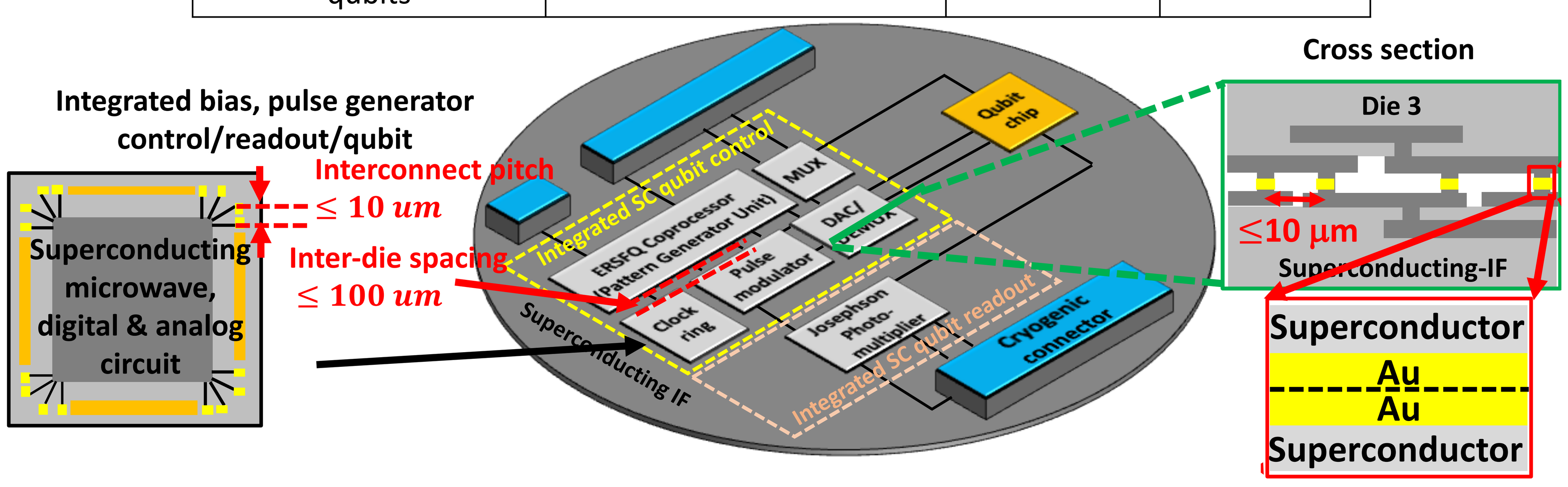


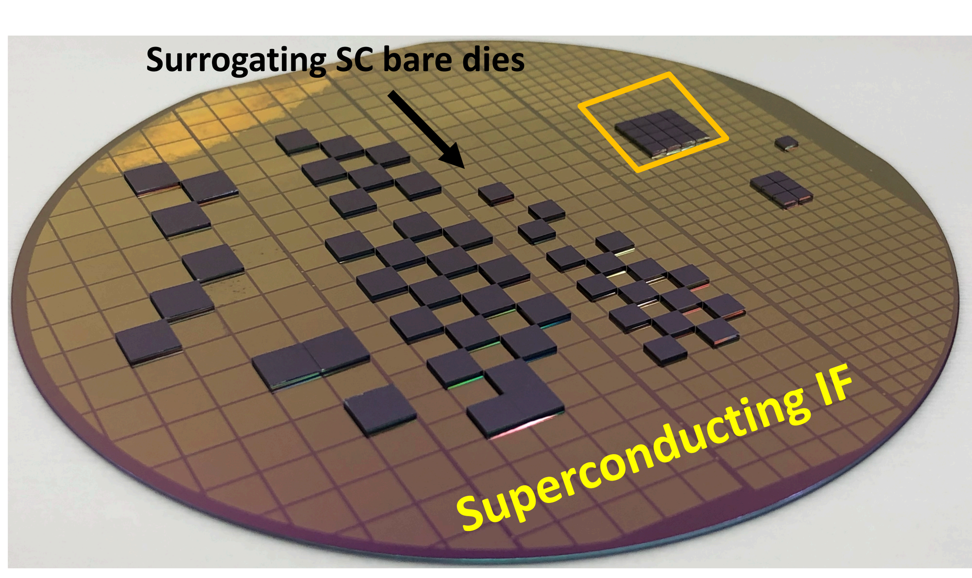
Three main changes:

(1) Superconducting control/readout (2) Wafer-level compact integration (3) Digital control

Comparison table between the two schemes

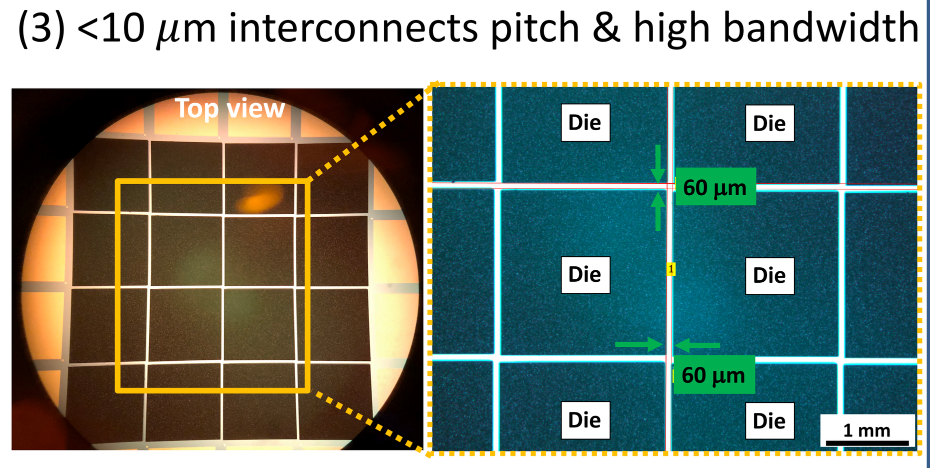
[1, 2]	μWave Analog	SFQ Digital	Improvement
Qubit-controlling signals	Microwave sinusoidal waveforms	Quantized pulses pattern	Variable pulse control
Error rate	$10^{-2}-10^{-3}$ [1]	10^{-4} [2]	10
Latency: interconnects readout/control cycle	ns ms	ps few ns	10^3 10^5
Maximum clock speed	2 GHz	40 GHz	20
Power dissipation per qubit inside DR	20 mW (now) 2 mW (with CryoCMOS)	0.2 μW	10^4
Maximum allowable qubits	360 (optimistically)	100M	~10^5



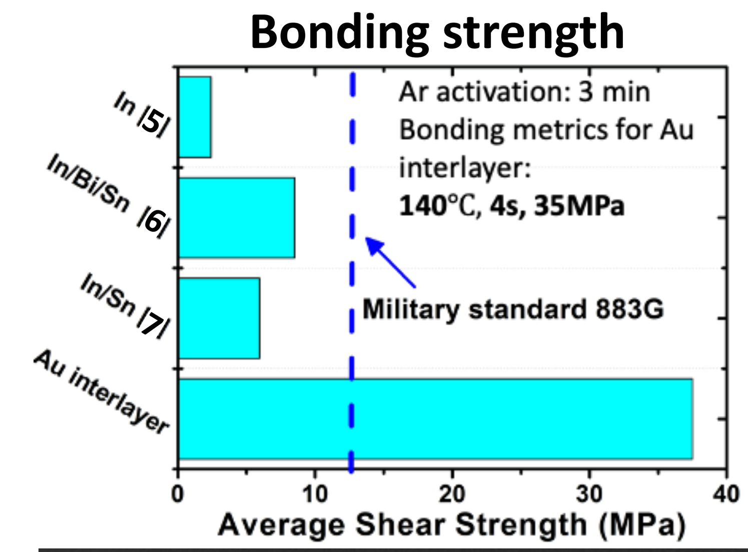


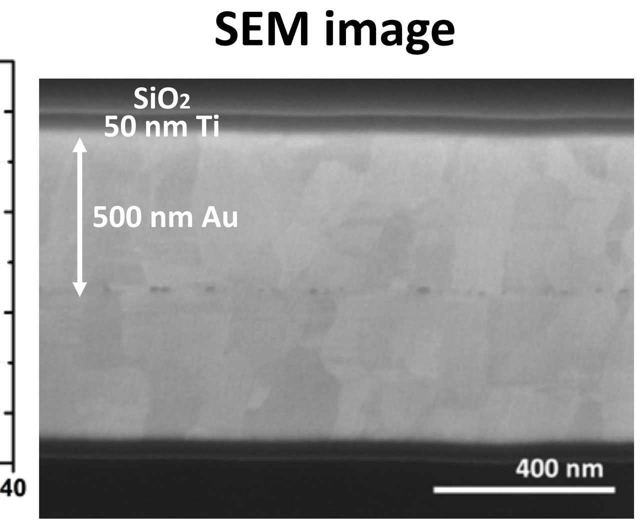
Major advantages :

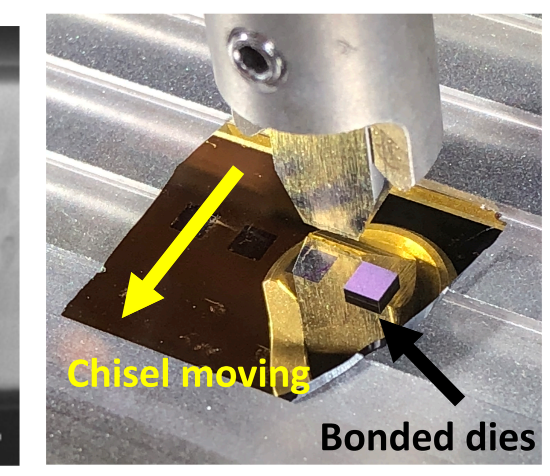
(1) Large Si area for millions of qubit & circuits
(2) Ultra low latency
(3) <10 μm interconnects pitch & high bandwidth

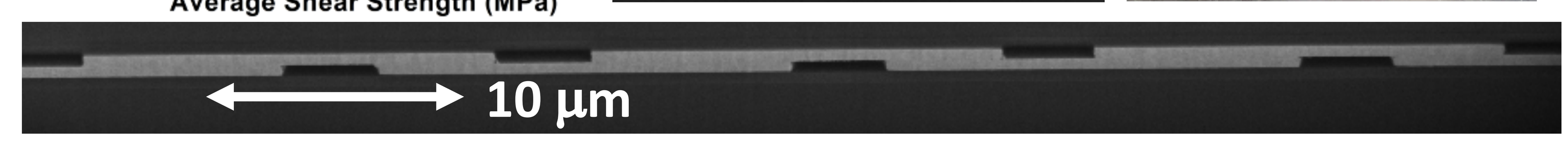


3. Au interlayer demonstration



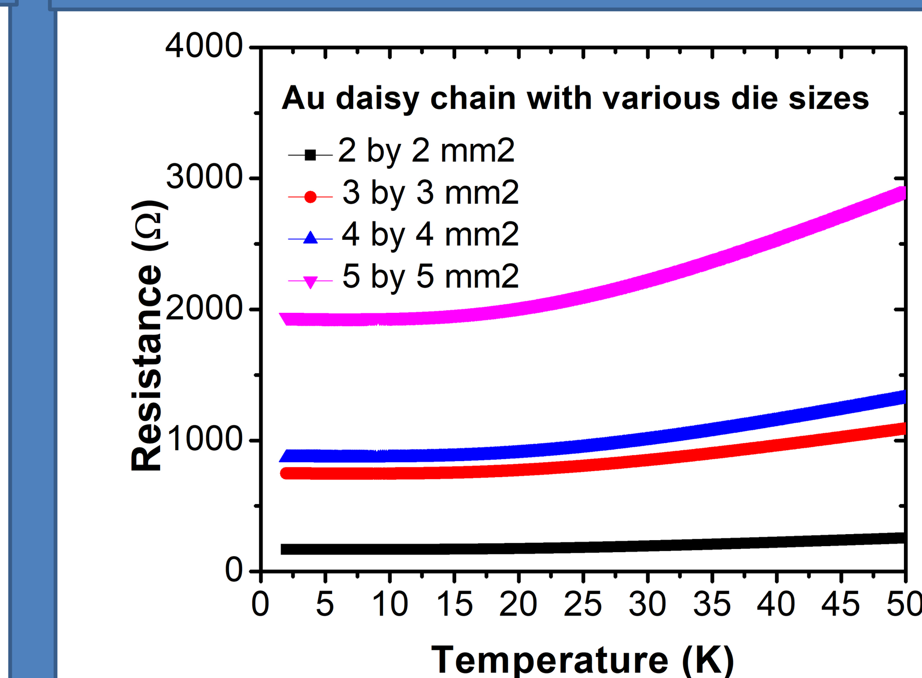


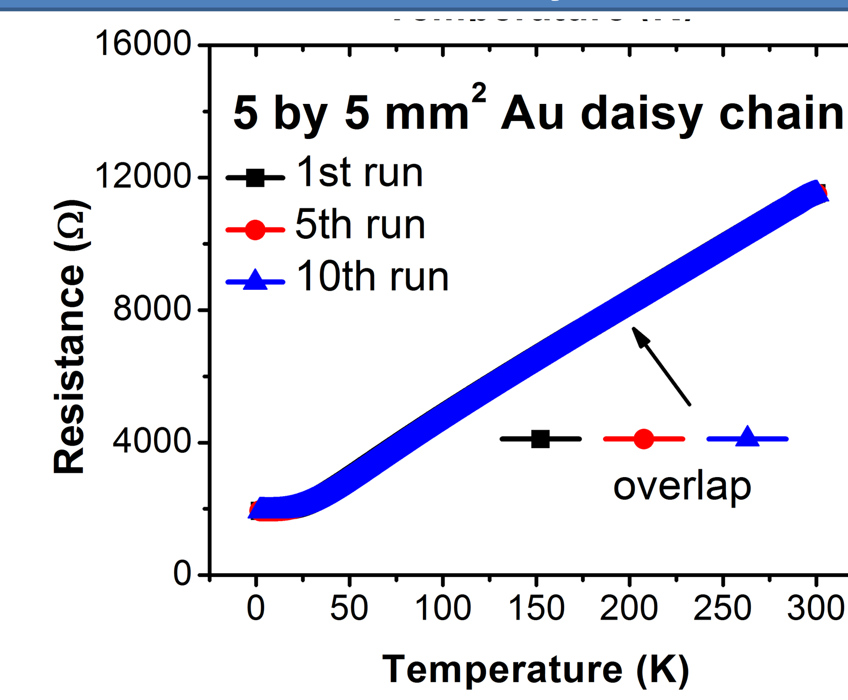




- Bonding strength of Au interlayer is 3X stronger than solder bumps

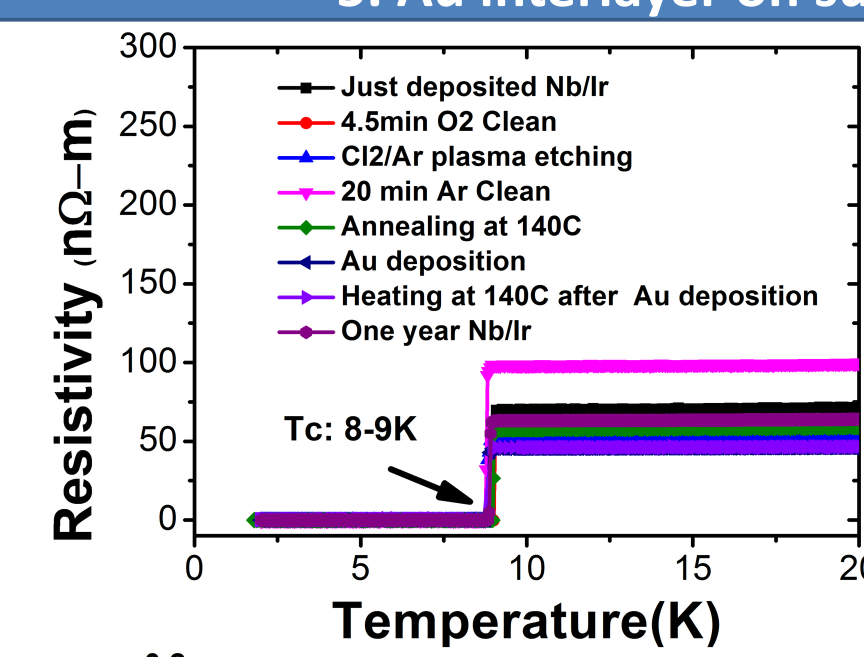
4. Electrical measurements of Au interlayer

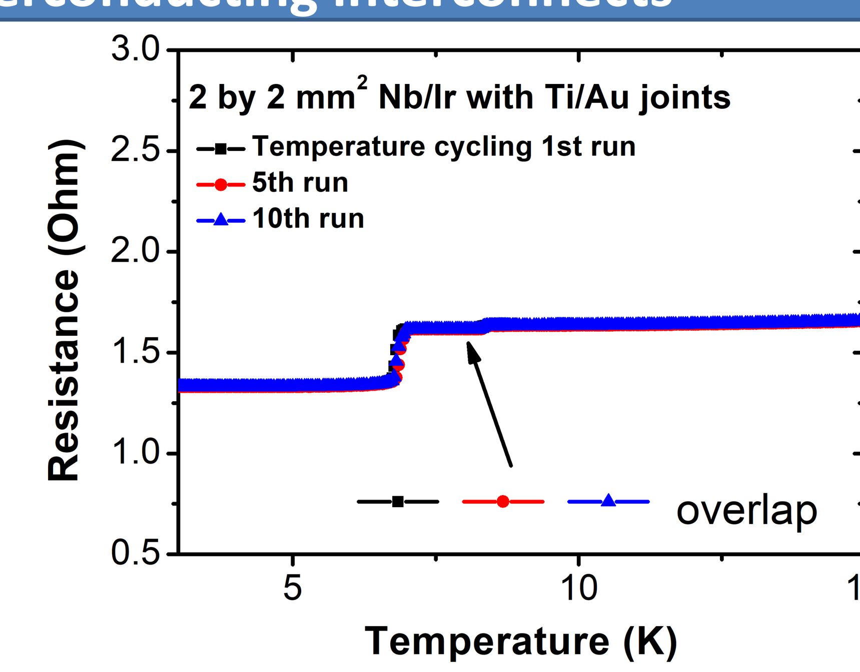


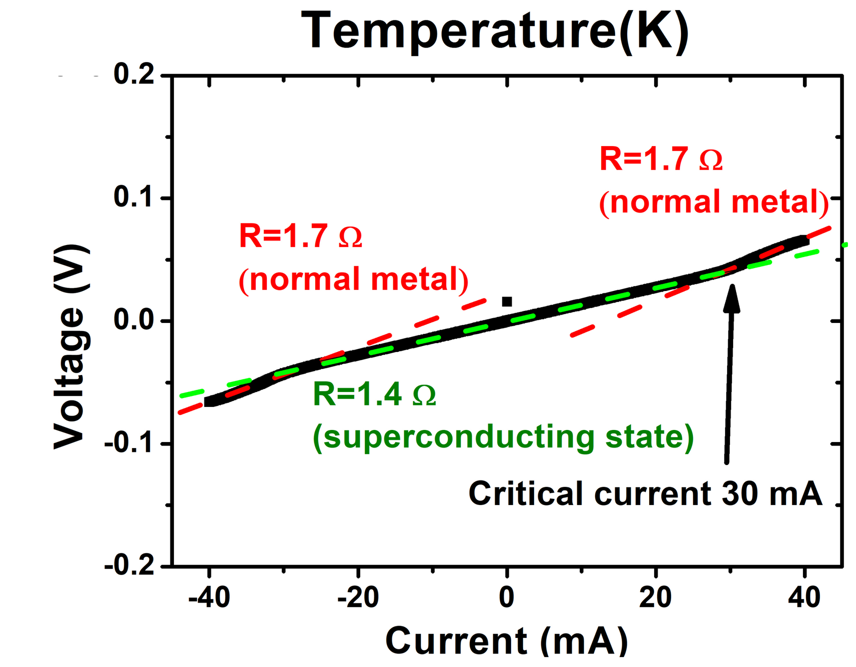


- Electrically connected at 2 K on various sizes of dies from 2X2 mm² to 5X5 mm²
- Au interlayer is reliably connected with temperature cycling from 300K to 2K.

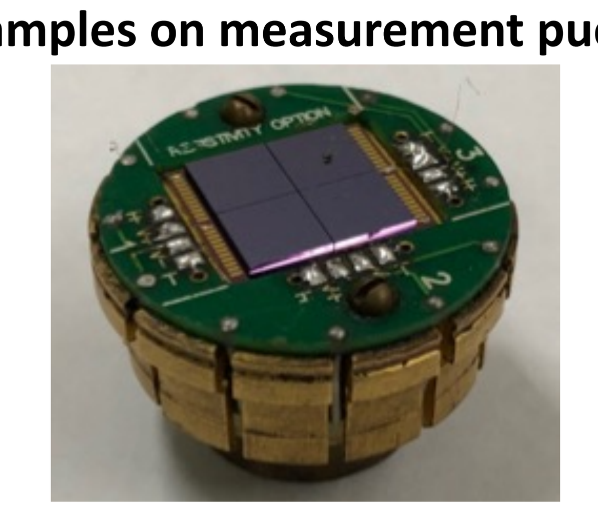
5. Au interlayer on superconducting interconnects







Samples on measurement puck



- Measured critical current density:
  Nb/Ir Control: 13.2 MA/cm2, 46% of the theoretical value.
  Nb/Ir/Ti/Au: 4 MA/cm², 14% of the theoretical value (comparison: Nb/In bumps [5], 6%)
- The process is confirmed to be quantum-compatible

6. Conclusions & Future work

- Proposed and demonstrated an architecture for quantum systems on superconducting Si-IF
- Demonstrated Au interlayer to be **fine pitch** (≤10 um), **quantum-compatible process** (<150℃), **mechanically robust** (> 30 MPa), and **electrically reliable** at 2 K
- Future work: RF characterization (impedance & loss)

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Reference:

1. O. Mukhanov, NY CREATES Seminar, 2020. **2.** A. J.-Salim – SeeQC. ECTC special session, 2020 **3.** Z. Chen, Ph.D. thesis, 2018. **4.** P. J. Liebermann, PRA, 2016.. **5.** Rabindra, ECTC 2017