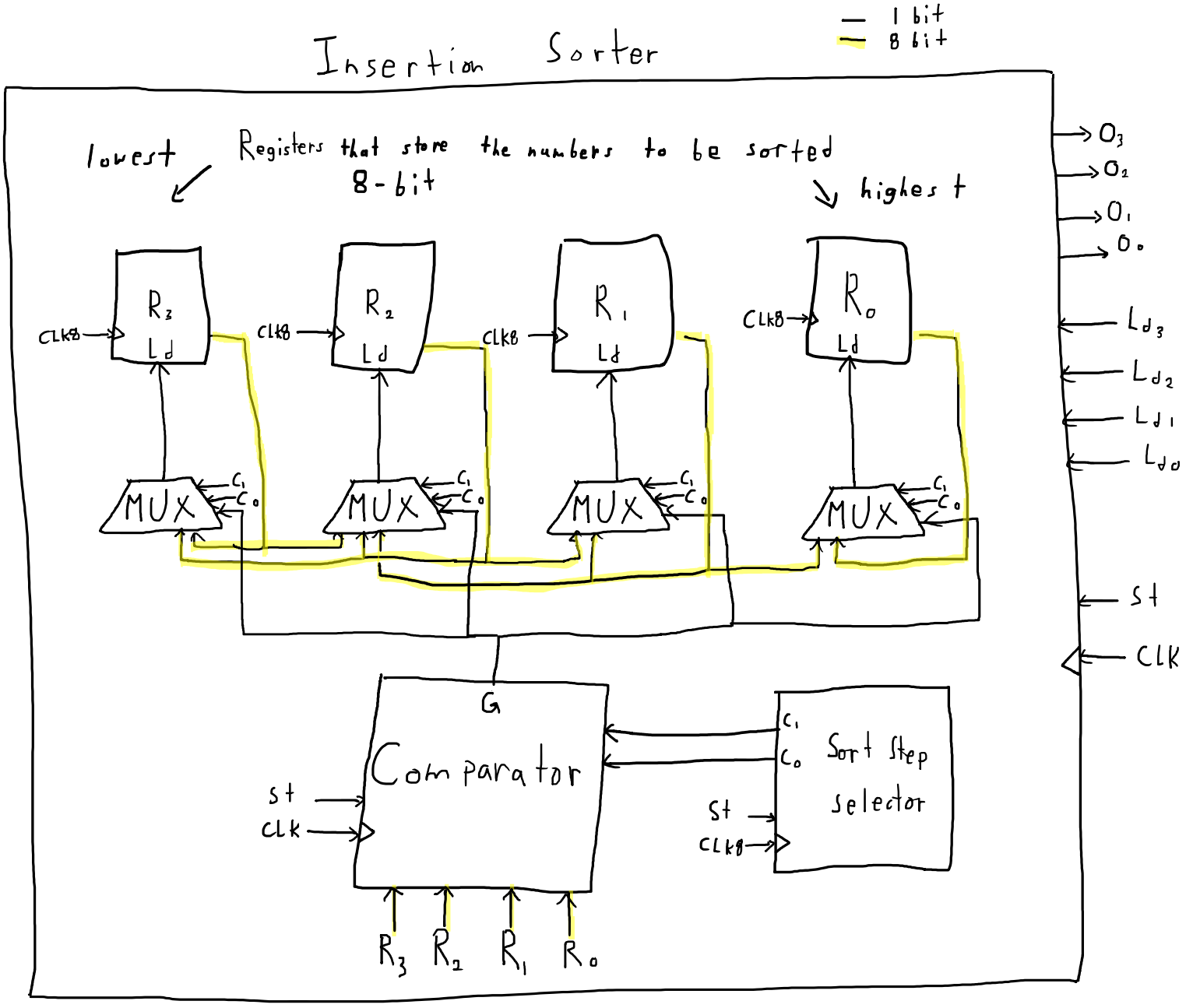
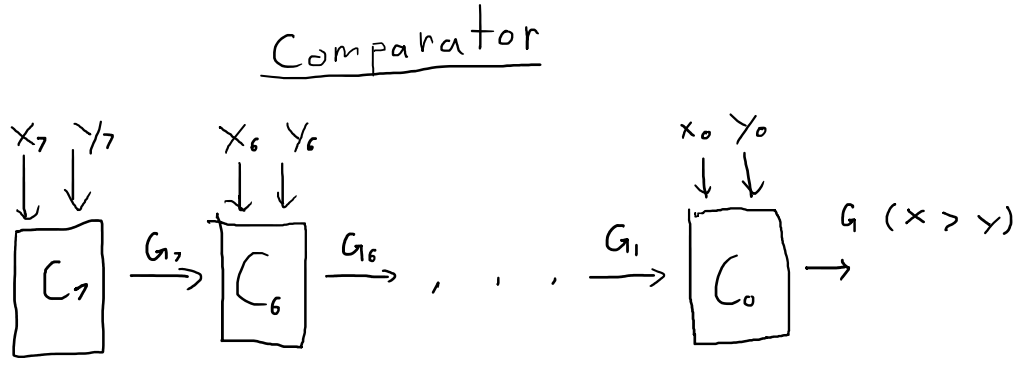
Block Diagram

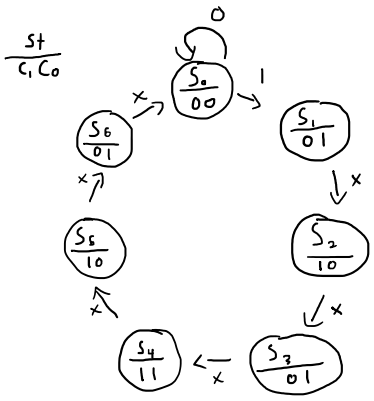
Name: Jon Case





State Design (Sort Step Selector)

State	Description
S_0	Reset / Wait to start sort
S_1	Compare R_3 and R_2 ; Pass 1
S_2	Compare R_2 and R_1 ; Pass 2
S_3	Compare R_3 and R_2 ; Pass 2
S_4	Compare R_1 and R_0 ; Pass 3
S_5	Compare R_2 and R_1 ; Pass 3
S_6	Compare R_3 and R_2 ; Pass 3



State	Next state St=0	Next state St=1	C_1	C_0
S_0	S_0	S_1	0	0
S_1	S_2	S_2	0	1
S_2	S_3	S_3	1	0
S_3	S_4	S_4	0	1
S_4	S_5	S_5	1	1
S_5	S_6	S_6	1	0
S_6	S_0	S_0	0	1

State Assignments

(1)

State	Next state St=0	Next state St=1	C_1	C_0
S_0	S_0	S_1	0	0
S_6	S_0	S_0	0	1
S_1	S_2	S_2	0	1
S_2	S_3	S_3	1	0
S_3	S_4	S_4	0	1
S_4	S_5	S_5	1	1
S_5	S_6	S_6	1	0

(2)

State	Next state St=0	Next state St=1	C_1	C_0
S_1	S_2	S_2	0	1
S_0	S_0	S_1	0	0
S_6	S_0	S_0	0	1
S_2	S_3	S_3	1	0
S_3	S_4	S_4	0	1
S_4	S_5	S_5	1	1
S_5	S_6	S_6	1	0

③

$D_2D_1D_0$	State	Next state St=0	Next state St=1	C_1	C_0
000	S_1	S_2	S_2	0	1
001	S_0	S_0	S_1	0	0
011	S_6	S_0	S_0	0	1
010	S_3	S_4	S_4	0	1
110	S_4	S_5	S_5	1	1
111	S_2	S_3	S_3	1	0
101	S_5	S_6	S_6	1	0

D_2^+

D_1D_0 \ St D_2	00	01	11	10
00	1	X	X	1
01	0	0	0	0
11	0	0	0	0
10	1	1	1	1

$D_2^+ = D_0'$

D_1^+

D_1D_0 \ St D_2	00	01	11	10
00	1	X	X	1
01	0	1	1	0
11	0	1	1	0
10	1	0	0	1

$D_1^+ = D_2' D_0' + D_2 D_0$

D_0^+

D_1D_0 \ St D_2	00	01	11	10
00	1	X	X	1
01	1	1	1	0
11	1	0	0	1
10	0	1	1	0

$D_0^+ = (St' + D_2 + D_1 + D_0')(D_2' + D_1' + D_0')(D_2 + D_1' + D_0)$

C_1

D_1D_0 \ D_2	0	1
00	0	X
01	0	1
11	0	1
10	0	1

$C_1 = D_2$

C_0

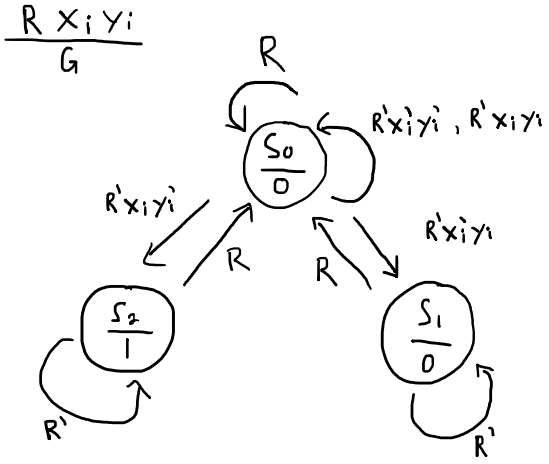
D_1D_0 \ D_2	0	1
00	1	X
01	0	0
11	1	0
10	1	1

$C_0 = D_0' + D_2' D_1$

State Design (Comparator)

State	Description
S_0	Reset, $X = Y$
S_1	$X < Y$
S_2	$X > Y$

Occurs for each bit in the 8-bit registers



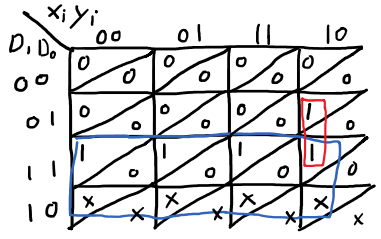
State S_i	Next State (RX_iY_i) 000	001	010	011	1XX	Output G
S_0	S_0	S_1	S_2	S_0	S_0	0
S_1	S_1	S_1	S_1	S_1	S_0	0
S_2	S_2	S_2	S_2	S_2	S_0	1

State Assignments

D_1 D_0	State S_i	Next State (RX_iY_i) 000	001	010	011	1XX	Output G
00	S_1	S_1	S_1	S_1	S_1	S_0	0
01	S_0	S_0	S_1	S_2	S_0	S_0	0
11	S_2	S_2	S_2	S_2	S_2	S_0	1

R %1

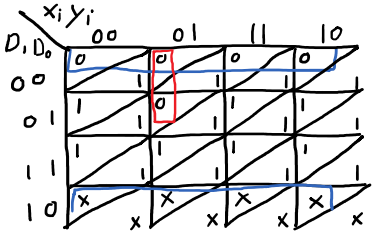
D_1^+



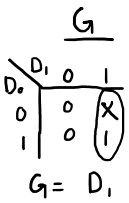
$D_1^+ = R'D_1 + R'x_iy_i'D_0$

R %1

D_0^+

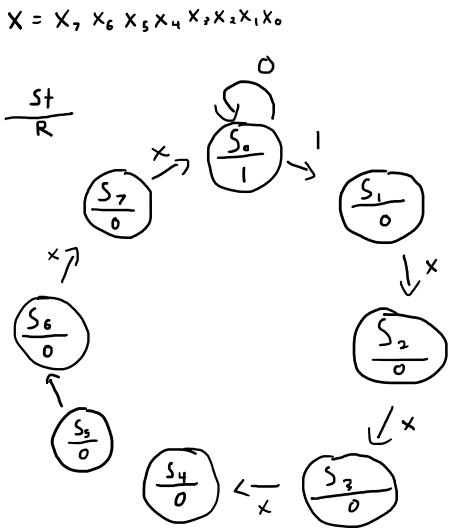


$D_0^+ = (R + D_0)(R + x_i + y_i' + D_1)$


G
D1
D0
0
1
0
0
X
1
0
1
G1 = D1

State Design (Comparator Bit Selector)

State	Description
S_0	Reset / Compare X_7
S_1	Compare X_6
S_2	Compare X_5
S_3	Compare X_4
S_4	Compare X_3
S_5	Compare X_2
S_6	Compare X_1
S_7	Compare X_0



State	Next state St=0	Next state St=1	R
S_0	S_0	S_1	1
S_1	S_2	S_2	0
S_2	S_3	S_3	0
S_3	S_4	S_4	0
S_4	S_5	S_5	0
S_5	S_6	S_6	0
S_6	S_7	S_7	0
S_7	S_0	S_0	0

State Assignments

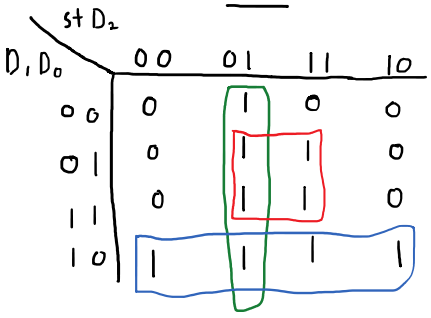
$D_2 D_1 D_0$	State	Next state St=0	Next state St=1	R
0 0 0	S_1	S_2	S_2	0
0 0 1	S_2	S_3	S_3	0
0 1 1	S_3	S_4	S_4	0
0 1 0	S_4	S_5	S_5	0
1 1 0	S_5	S_6	S_6	0
1 1 1	S_6	S_7	S_7	0
1 0 1	S_7	S_0	S_0	0
1 0 0	S_0	S_0	S_1	1

R

D_1 / $D_1 D_0$	0	1
0 0	0	1
0 1	0	0
1 1	0	0
1 0	0	0

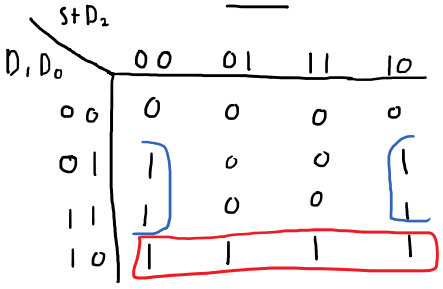
$R = D_2 D_1' D_0'$

D_2^+



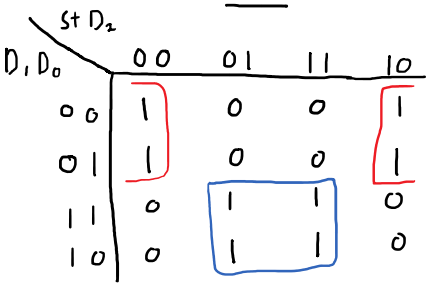
$D_2^+ = D_1 D_0' + D_2 D_0 + St' D_2$

D_1^+



$D_1^+ = D_1 D_0' + D_2' D_0$

D_0^+



$D_0^+ = D_2 D_1 + D_2' D_1'$