Execution of Multi-Cycle Processor

Fetch, Decode, Execute, Write-Back.

1. When the Processor is Reset, the Control Address Register (CAR) points to the first instruction in Control Memory (CM) and the Program Counter (PC) points to the first micro program in Main Memory (MM).
2. The first instruction in CM will be Instruction Fetch (IF).
3. The first instruction is loaded from MM into the Instruction Register (IR), with mux M and the Instruction Load Flag (IL) set by IF.
4. The PC is incremented, preparing the CPU for the next Fetch.
5. IR splits the micro program into 7bit Opcode and 3x3bit Destination (DR), Source A (SA) and Source B (SB) registers.
6. The next instruction is Execute (EX0), which simply sets mux C = 1 so that the opcode in the IR can be loaded into the CAR to index into CM and lead to the Execute phase.
7. Opcode is fed into the Control Address Register (CAR) where it is used to index into the Control Memory (CM). The Next Address (NA) from the CM is fed back into the CAR to get the next IF, which will bring the CPU into the next Fetch.
8. The registers specified by SA and SB in the Register File (RFILE) appear on the A Data Bus and B Data Bus respectively.
9. The CM outputs a 28 bit control word.
10. The Function Select (FS) field specifies what operation the Function Unit (FU) should perform on the data on the A Data Bus and B Data Bus.
11. The Status Bits from the FU are set as inputs to mux S which is used for incrementing the CAR's current value, if = 0, instead of loading it with NA or from the IR, if = 1. This is used in conditional statements. The MS field specifies which status bit (or none at all) to depend on.
12. The MB field controls mux B, which controls the use of a register or an immediate value on the B Data Bus.
13. The MD field controls Mux D, which sets the output of the FU to be written to the RFILE or MM.
14. In the case of an operation which requires the use of temporary values, the Temporary Destination (TD), Temporary Source A (TA) and Temporary Source B (TB) fields allows the use of register 8 in the RFILE.
15. The Program Counter Increment (PI) and Program Counter Load (PL) fields are used to either increment the PC or to add to the PC with an offset from the addition of the SB and DR values from the IR.
16. The Register Write (RW) and Memory Write(MW) fields, when set, allow the writing of data to a register in the RFILE or to an address in MM respectively in the Write-Back stage
17. On the next clock cycle the output of the FU or the data on Data Bus B is written to either the RFILE or MM as specified above.