Homework #3

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ME 374 - Digital Control

May 22nd

Question 1

Analyze the control of a servomotor controlling the azimuth angle of a radar antena.

a. Find $G(z)$ with the ZOH of $P(s)$.
Using matlab's c2d(P,T,'zoh') with T = 0.05,

$$G(z) = \frac{4.014e-05z^2 + 0.0001547z + 3.724e-05}{z^3 - 2.856z^2 + 2.717z - 0.8607}$$

Here we can see 2 sampling zeros where added.

b. For $D(z) = K$ for constant gain $K > 0$, draw root locus wrt K and determine which values of K yield a stable closed loop system.

$D(z)$ was chosen to be $K = 1$ such that the characteristic equation was directly $1 + K * G(z) = 0$ and rltool() was used on the loopgain $KG(z)$ which produced the following root locus plot. Upon analysis of the step response and tracing what kept the poles inside of the unit circle in the z-plan $K < 2$ keeps the system stable, while $.1 < K < .5$ produces a closed loop unity feedback system with generally reasonable characteristics.

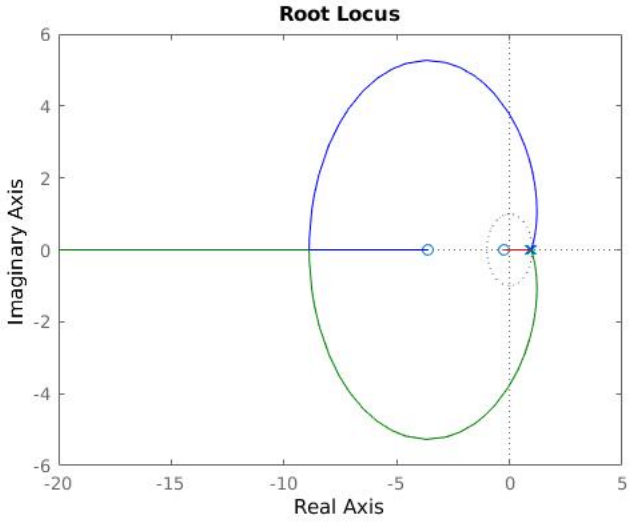

Figure 1: Root Locus wrt parameter K

c. Find time constant of the slowest closed-loop pole when $D(z) = 1$.

Analogous to slower poles corresponding to poles closer to the imaginary axis in the continuous time complex domain, the slowest poles are those closest to the unit circle in the z-plane. The time constant of the complex pair is $4.37s$.

d. Design a lead controller $D(z)$ with unity DC gain such that the time constant of the slowest closed loop pole is $< 1.2s$.

Using rltool() we were able to design the following controller: $D(z) = 8.0678\frac{z-0.951}{z-0.607}$. This controller has a DC gain of 1 such that $D(1) = 1$ and we placed it in the feedback path of the system. The effect on the slowest poles time constant of placing a lead zero at 0.951 and a lead pole at 0.607 is that the slowest time constant becomes $1.18s$.

Question 2

For the given regulator control system with unit step input disturbance, plant transfer function, constant zero valued reference signal, and sampling rate of T=0.1s. For a controller $D(z) = 2$ what is the steady state value of the sampled output? What would the steady state value be if $D(z) = 2 + \frac{0.2z}{z-1}$?

a. Calculate the DC gain of the transfer function from $R(s)$ to $C_e(s)$ assuming $D(z) = 1$.

One must simply calculate the forward path over the loop gain in this case. Fortunately With a digital controller of 1 we can effectively ignore this block and the DAC immediately after it. This gives us a TF of:

$$H(s) = \frac{\frac{2}{s+0.5}0.004}{1 + \frac{2}{s+0.5}0.004} = \frac{0.08s + 0.04}{s^2 + 1.08s + 0.29}$$

Evaluating this for the DC gain at $H(0)$ we get **0.1397** for the DC gain of the TF.

b. For $D(z) = K$ with constant $K > 0$, draw root locus wrt K and determine values of K that lead to a stable closed loop system.

To do this we represented out plant as $P(s) = G_p(s)H$. Which we can convert to the digital domain using c2d(P,T,'zoh'). Choosing $K = 1$ we can send the loopgain $KG(z)$ to rltool(). Find the point closest to being on the unit circle yields $K \approx 41.8$ as the largest gain in which the system remains stable. Therefore the system is stable for $0 < K < 41.5$

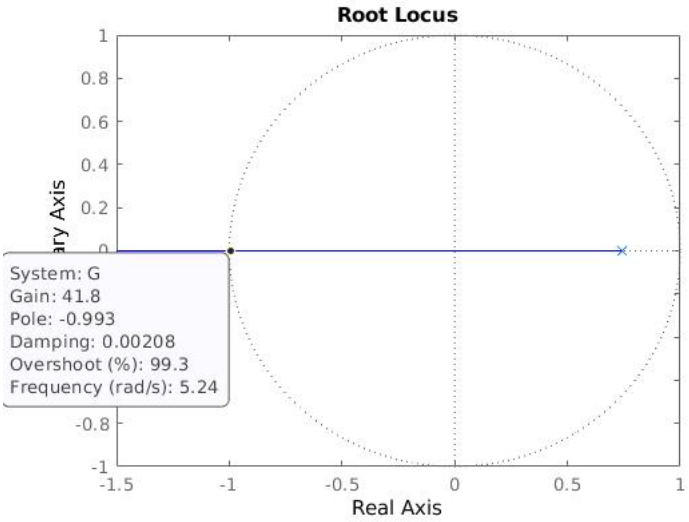

Figure 2: Root Locus wrt parameter K

c. Find the time constant for the system with $D(z) = 1$

Incorporating the constant unity controller $D(z) = 1$ in to the feedback system yields a system with the transfer function $H(z) = \frac{G(z)}{1+G(z)}$ where $G(z)$ was computed as the ZOH equivalent of $P(s)$. Using damp() to find the tmie constant associated with this system we get: **1.68s**.

d. Design a phase lag controller such that the characteristic eq. has similar roots to $1 + G(z)$ but with a controller DC gain of 3.

Using rltool() this process isn't too dificult to implement a satisfactory controller that incorporates phase lag with the appropriate DC gain:

$$D(z) = \frac{1.3569(z - 0.002479}{z - 0.5488}$$

, by using the handy evalfr(D,1) we can see that the DC gain is 3 and by calling damp() on the new TF that incorporates our phase lag controller we can see that while the pole(s) have moved off the real axis, their time constants are still similar to our initial single pole at 1.33s.

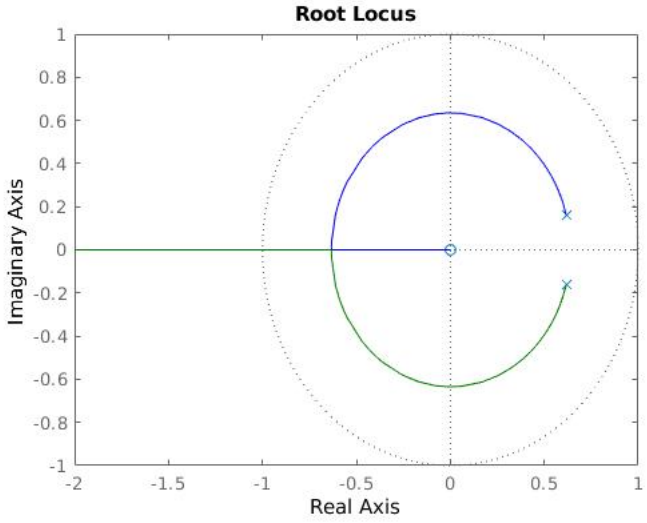

Figure 3: Phase Lag Root Locus

e. Find the steady-state value of the output due to a step disturbance using the phase lag controller designed in c).

To do so we designed a simulink schematic after the presented system model, with our controller substituted for $D(z)$.

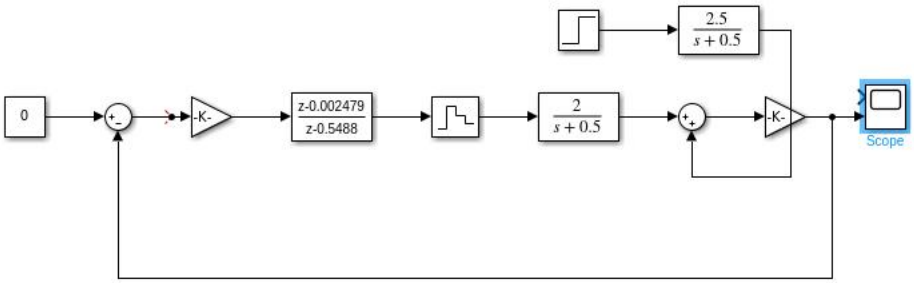

Figure 4: System Model in Simulink

The response to step disturbance was as follows, as it can be seen the system is over-damped and settles to a value of ~ 0.135.

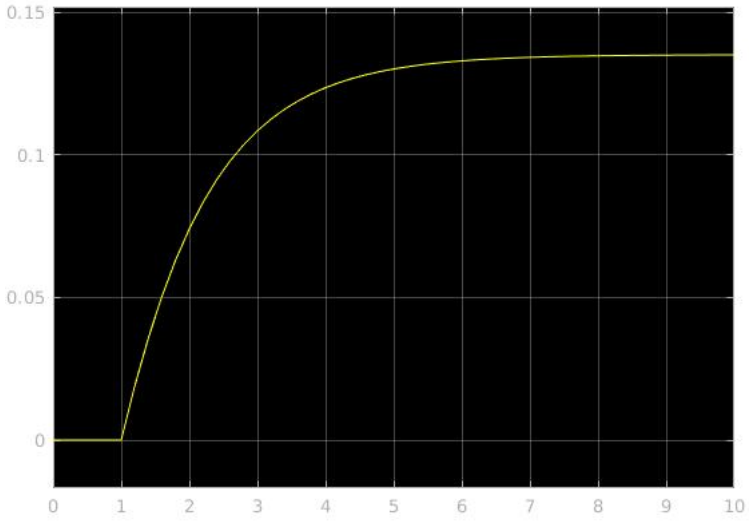

Figure 5: Response to Step Disturbance