

ScienceDirect



Neural interface systems with on-device computing: machine learning and neuromorphic architectures [∞]

Jerald Yoo^{1,2} and Mahsa Shoaran³



Development of neural interface and brain-machine interface (BMI) systems enables the treatment of neurological disorders including cognitive, sensory, and motor dysfunctions. While neural interfaces have steadily decreased in form factor, recent developments target pervasive implantables. Along with advances in electrodes, neural recording, and neurostimulation circuits, integration of disease biomarkers and machine learning algorithms enables real-time and on-site processing of neural activity with no need for power-demanding telemetry. This recent trend on combining artificial intelligence and machine learning with modern neural interfaces will lead to a new generation of lowpower, smart, and miniaturized therapeutic devices for a wide range of neurological and psychiatric disorders. This paper reviews the recent development of the 'on-chip' machine learning and neuromorphic architectures, which is one of the key puzzles in devising next-generation clinically viable neural interface systems.

Addresses

¹ Department of Electrical and Computer Engineering, National University of Singapore, Singapore, 117585, Singapore

Corresponding author: Shoaran, Mahsa (mahsa.shoaran@epfl.ch)

Current Opinion in Biotechnology 2021, 72:95-101

This review comes from a themed issue on **Tissue**, **cell and pathway engineering**

Edited by Mahsa Shoaran and Stéphanie P Lacour

For a complete overview see the Issue and the Editorial

Available online 1st November 2021

https://doi.org/10.1016/j.copbio.2021.10.012

0958-1669/© 2021 The Author(s). Published by Elsevier Ltd. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

Introduction

Innovation in neurotechnology has greatly accelerated over the past decade, targeting long-term therapeutic efficacy. The number of electrodes is growing steadily [1–4] and the integrated circuits used for neural signal acquisition continue to improve in power consumption, size, and robustness [5,6]. A driving force for these technological advances is the lack of effective pharmacological treatments for most chronic brain disorders that necessitate the development of new device-based solutions.

Recent wireless head-mounted neural interface systems paired the neural interface with external processing devices [7–9]. For example, Neurochip-2 [7] adopts three adjustable sensing channels (for spike, LFP, ECoG, or EMG recording) and three programmable stimulation channels. The PennBMBI [8] is a general-purpose battery-powered wireless system with 4-Ch. programmable sensing, feature/spike detection, compression, and 8-Ch. stimulation capabilities. To overcome the limitations of current BMIs with modest channel counts, high-channel-count neural interface system-on-chips (SoCs) are also being developed as researchbased systems [2] and by companies like Paradromics [1] and Neuralink [3]. However, most of the current interfaces rely on external signal processing, requiring the streaming of high-density neural data (or spikes) off the body; This approach increases the power consumption of the system, and as a result, the number of channels and the overall data rate is limited to minimize heat dissipation near the tissue (e. g. reported power of 750 mW for Neuralink BMI [3], which is above the safe limit for human use if implanted). In addition, closed-loop neuromodulation systems that employ remote computing for symptom tracking (e.g. for epilepsy and movement disorders) impose long latencies that could jeopardize the real-time therapeutic feedback [10,11]. Such systems could cause privacy and security concerns as they wirelessly transmit patient's private data to an external system for subsequent processing. The alternative approach that implements a machine learning-based classifier or decoder on the receiver side or in the cloud (rather than on the implant) similarly suffers from high power consumption due to wireless transmission and long feedback latency (several hundreds of millisecond) caused by the wireless link. This approach could degrade the efficacy of closedloop stimulation and require more frequent battery replacements. Therefore, developing low-power closed-loop systems and BMIs with AI on the edge is the most promising approach to enable effective therapeutic devices for brain disorders, as reviewed in this paper.

Neural interface systems with on-chip computing

Digital and mixed-signal machine learning SoCs

Neural interfaces with Machine-Learning (ML) on the edge reduce uplink/downlink data communication

² The N.1 Institute for Health, Singapore, Singapore, 117456, Singapore ³ Institute of Electrical Engineering, Center for Neuroprosthetics, École polytechnique federal de Lausanne (EPFL), 1202, Geneva, Switzerland

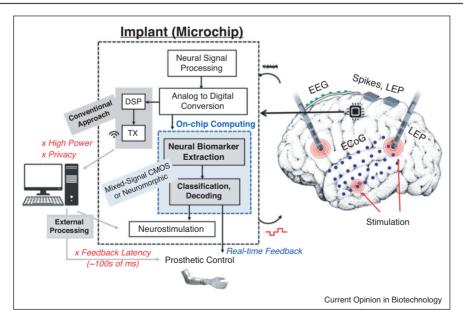
[☆] Full responsibility for the editorial process of this article was delegated to Stéphanie P. Lacour.

burdens, and hence power and form factor of the implant are also reduced; On-chip ML allows real-time prediction of disease symptoms (e.g. epileptic seizures, Parkinson's tremor, mood change or anxiety) to trigger therapeutic stimulation in a closed-loop system, or to enable motor decoding for prosthetic control in a BMI (Figure 1). As the on-chip environment is highly resource- and power-limited, various low-power and area-efficient digital/mixedsignal system-on-chips with embedded ML have been reported in literature. Recent work implemented a dedicated patient-specific feature extraction and classification engine with low-power online adaptive tuning [12°°] (Figure 2(a)), power-efficient regularization techniques for oblique decision tree algorithms [13°], and an exponentially decaying-memory support vector machine (EDM-SVM) classifier combined with a neural network autoencoder to reduce dimensionality of input data [14]. Similarly, the work in Ref. [15] integrated approximate entropy and spectral power features with a ridge regression classifier. Alternatively, the system proposed in Ref. [16°] implemented a two-level classifier based on coarse/ fine detectors to reduce power consumption during interictal (non-seizure) state. A second DSP chip integrating more complex features and a least-squares SVM classifier was turned on in case of seizure-like events captured by the primary detector. The majority of these systems were verified offline on human epilepsy data, and in closedloop seizure control in animal models of epilepsy.

While most current system-on-chips have only been designed and optimized for epilepsy (thus benefiting a relatively small population), there is a pressing need for novel sensing, stimulation, and AI-powered closed-loop devices for other pharmaco-resistant brain disorders. Advances in this domain will be crucially important to meet the needs of the global population suffering from an increasing rate of neurological and psychiatric disorders.

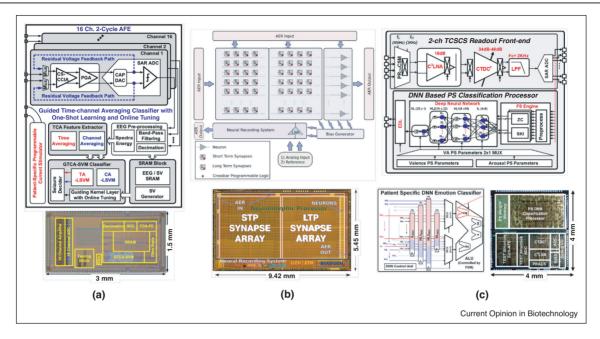
Neuromodulation (e.g. deep-brain and cortical stimulation) has shown promising effects in treating psychiatric disorders such as Obsessive-Compulsive Disorder (OCD) and major depression [17], as well as memory disorders [18,19]. Despite promising early results, a key limitation is the open-loop delivery of stimulation in standard DBS, which is not efficient in modulating target brain structures in diseases such as Alzheimer's and depression [20-23]. In contrast, closed-loop stimulation approaches based on disease biomarkers and ML are being investigated to treat various intractable brain disorders. For example, electrophysiological features linked to vocal tic onset in patients with Tourette's syndrome have been successfully used to treat patients when compared to conventional DBS [24]. Disorders such as Alzheimer's arise from multi-region network abnormalities and require highdensity neural recording. A subject-specific logistic regression model was used to predict memory encoding state from brain-wide ECoG recordings and activate

Figure 1



A neural microchip integrating conventional processing pipeline versus on-chip computing. Neural signals recorded as scalp EEG, surface ECoG, spikes, or LFP are conditioned and digitized by the microchip. In the conventional approach, digital data is wirelessly transmitted to an external processor, posing latency, power dissipation, and privacy concerns. With on-chip computing, feature extraction and neural decoding are performed directly on the neural device. Therapeutic stimulation or prosthetic control is subsequently activated.

Figure 2



Neural interface SoCs with on-chip ML. (a) A 16-channel closed-loop epilepsy management system with online tuning and one-shot learning, achieving state-of-the-art energy efficiency of 0.97 µJ/class and area of 0.13 mm²/Ch [12**]. (b) A neural interface with on-chip neuromorphic computing for BMI applications, occupying an area of 51.4 mm² and consuming 4 mW of power [35,36]. (c) A 2-channel DNN classifier for fourstate emotion detection in Autism, achieving energy efficiency of 10.1 µJ/class and total area of 16 mm² [26].

closed-loop stimulation to enhance recall in humans [18]. ML SoCs have also been developed for sleep stage classification [25], four-state emotion detection in Autism using a Deep Neural Network (DNN) [26] (Figure 2(c)), or emotion detection from EEG with a Convolutional Neural Network (CNN) with online training [27]; In another work, an Artificial Neural Network (ANN) processor was developed for migraine state detection using somatosensory evoked potentials [28]. Early prediction of migraine attacks could enable more effective treatment based on pharmacological or simulation-based therapies.

ML approaches are also increasingly being used to detect motor symptoms in patients with Parkinson's disease (PD) and essential tremor [29-31] to enable closed-loop (i.e. adaptive) DBS. This emerging stimulation strategy improves therapeutic efficacy, power consumption, and side effects of conventional DBS [32]. An ML approach combining multiple biomarkers of tremor in LFP such as multi-band spectral power, phase-amplitude coupling, and high-frequency oscillations ratio, with a smoothing Kalman filter achieved 89.2% sensitivity in detecting reststate tremor in PD patients [29,33]. Another recent study used a classifier to detect voluntary movements and postural tremor in patients with essential tremor [30]. More progress in AI-embedded neural interface design for movement disorders is expected in the future.

Neuromorphic SoCs

Brain-inspired neuromorphic architectures are also being used in neural interfaces and BMIs, thanks to their low power and high adaptability [34]. Neuromorphic designs emulate the function of nervous systems in analog, digital, or mixed-signal CMOS hardware. For example, the event-based neuromorphic system in Ref. [35] forms a two-layer Spiking Neural Network (SNN) with online learning that converts neural signals into asynchronous streams of pulses encoded with address event representation for classifying auditory stimuli. The neuromorphic processor [36] was adopted in a modular closed-loop BMI for decoding motor intentions and delivering sensory stimuli to the brain in anesthetized rats, achieving a robust decoding performance [37] (Figure 2(b)). A similar method was used to deliver somatosensory feedback stimulation in a closed-loop BMI in rodents, based on spiking activity, features of LFP, or behavioral events [38]. In Ref. [39], a 4-Ch. wireless and battery-powered implant [40,41] stimulated the somatosensory cortex in response to spikes detected in the premotor cortex in a rat model of focal brain injury. This approach could potentially enhance the functional connectivity between target brain regions and facilitate recovery after traumatic brain injury (TBI). Neural prostheses with more complex computations, on-chip ML and neural decoding, and higher number of recording and stimulation channels are expected to emerge in future to permanently replace damaged brain circuits.

Neuromorphic chips can be used in closed-loop bidirectional prostheses to treat neurological disorders such as epilepsy. For example, a tree-based AdaBoost model with 1024 trees with a depth of one was reported for closedloop seizure suppression [42]. The neuromorphic feature extraction module in this system enabled an excellent energy efficiency for intracranial EEG processing. A mixed-signal multi-core neuromorphic processor was reported in Ref. [43], exploiting an event-based communication. This SNN processor was used to detect High-Frequency Oscillations (HFO) as biomarkers of seizure events, consuming 614.3 µW of power for 8-Ch [44**].

Neuromorphic systems can efficiently adapt their structure to time-varying dynamics of neural signal, using methods such as spike-timing-dependent plasticity (STDP). In addition, inspired by the sparse nature of synaptic connections in the human brain, SNN accelerators that exploit weight sparsity can efficiently reduce model size, computational and data transfer energy. The work in Ref. [45] improved the energy efficiency of SNN using a reconfigurable processor with 4096-neuron and 1M-synapse in 10 nm FinFET process. Weight sparsity, near-threshold optimization, power and clock gating were employed to achieve state-of-the-art energy efficiency. while supporting on-chip unsupervised STDP learning. Several other SNN accelerators have been implemented as an ASIC, either with offline [46,47] or on-chip learning architectures [48–50].

Sensory prostheses such as retinal and cochlear implants may also benefit from asynchronous neuromorphic computing. A typical retinal prosthesis has an external device that translates incident light into electrical signals, then transmits the data into an implant that stimulates the retinal cells accordingly. Such setup inevitably has a bulky form factor, limiting the patient's quality of life. In contrast, an on-pixel neuromorphic image processor with a stimulator mimics human retinal operation and eliminates the need for an external device [51°], consuming only 56.3 nW/Ch. Such techniques could enable a new generation of high-channel-count and high-performance sensory prostheses. It should be noted that convolutional neural network (CNN) is also widely used in neural signal processing and in edge applications implemented on FPGA, GPU or CPU [27,52,53]. However, in area-constrained implantable devices, it is crucial that the power density of the system is kept at a minimum level to satisfy safety concerns. This motivates the need for low-power neuromorphic processing rather than a power-hungry inference engine such as CNN.

CNNs can also be implemented as a neuromorphic computing platform (e.g. SNN). For instance, IBM's

brain-inspired TrueNorth processor (4.3 cm², maximum power of 70 mW) is capable of implementing convolutional networks and has been used in a number of electrophysiological studies [54–56], dissipating tens of milliwatts for 2-Ch. EEG classification [56]. For resource-constrained neural implants or wearables, a more miniaturized and power-efficient realization of the classifier is desired.

In addition, efforts have been made to develop biomimetic cognitive prostheses for disorders of memory and learning [57]. The system in Ref. [57] used a neuromorphic multi-input/multi-output (MIMO) nonlinear model implemented in VLSI hardware to restore formation of long-term memory after hippocampal damage. This 16-input/16-output MIMO predicts the spike train output of the hippocampus that represents coded memories, based on presynaptically recorded spike train inputs in behaving rats. The low-power and miniaturized integration of MIMO model for this application remains as future work.

Commercial devices

In addition to the systems described above, neurotechnology research has witnessed substantial growth in the number of startups and companies in this space in the past decade (e.g. Neuralink, Paradromics, Newronika, Bioinduction, etc). However, on-chip computation is currently limited to simple signal processing and feature extraction. Example platforms include the Responsive Neurostimulator (RNS, NeuroPace) for intractable epilepsy that implements feature thresholding on 4 channels to predict seizures [58], the Summit RC + S [59] and Percept PC systems by Medtronic that implement 4-Ch. spectral power and a linear classifier for adaptive DBS in movement disorders. Such devices may require external systems with advanced machine learning algorithms for accurate symptom tracking [11]. These systems have paved the way for multiple feasibility studies and clinical trials to explore closed-loop stimulation for various neurological indications.

Despite significant improvements in channel count and spatiotemporal resolution in BMI systems developed by companies such as Paradromics [1] and Neuralink [3], on-chip neural decoding is a missing feature and remains as future work. For instance, the 1024-channel closed-loop BMI chip developed by Neuralink [60] integrates neural recording and spike detection circuitry on the implantable microchip, while relying on external devices for motor intention decoding. The breakthrough findings of these studies encourage the design of next-generation intelligent neuromodulation systems and BMIs with more advanced on-chip computing as well as improved energy efficiency and miniaturization [21].

Design tradeoffs, channel count, and scalability

The exploratory use of closed-loop stimulation in established and emerging indications has demonstrated promising results. However, the type and number of feedback signals and candidate biomarkers linked to pathological brain states vary across the distribution of patients for each indication under study. Thus, simple thresholding of a single biomarker can be suboptimal in tracking the underlying disease state [29]; Hence, we need advanced machine learning techniques to improve classification accuracy. To enable real-time feedback, ML algorithms need to be implemented on the implant, and under extreme power and area constraints to allow high-resolution symptom tracking. Implants with low channel count, high power, and bulky design are inefficient in treating brain disorders. Similarly, the on-chip integration of spike/ECoG/LFP processing and motor decoding algorithms is an urgent need for the next-generation low-latency, high-channelcount, and high-performance BMIs.

Indeed, future brain implants will inevitably incorporate large numbers of sensing electrodes to improve diagnostic accuracy and neural decoding performance. We should note that the complexity of the on-chip feature extraction and machine learning hardware will dramatically increase for arrays of 100–1000 s electrodes. Current brain implants with fully integrated ML hardware (both standard CMOS and neuromorphic architectures) are capable of processing up to 32 channels under implantable power and area constraints [61]; High channel counts can be obtained by integrating dimensionality reduction (e.g. autoencoders [14]), time-channel averaging [12**], or by using ML algorithms that inherently select relevant features to reduce the burden on feature extraction and ML hardware [13°,61].

Similarly, the number of stimulation channels in future implants will increase to enhance spatial resolution and selectivity of neuromodulation. For instance, recent DBS leads use segmented designs with large numbers of small contacts (16, 40, 1760 [62]) to precisely activate target regions. It has been shown that stimulation outside the target region (e.g. by large cylindrical contacts in the conventional 4-Ch. DBS lead) could result in chronic mental or motor side effects [62]. These technologies are not vet adopted in current neural prostheses and require novel high-density and programmable stimulation circuits, new DBS programming techniques, as well as more complex stimulation paradigms controlled by onimplant machine learning algorithms.

Chronic performance

On the algorithm front, brain implants require machine learning algorithms with improved sensitivity, lower false alarm rate, and higher classification/regression performance. In addition, there is a pressing need for algorithms with efficient online learning capability to address the non-stationarity of neural signals in chronic settings. Recent work has reported online tuning algorithms for SVM [12^{••}] and logistic regression [63] in seizure detection tasks with negligible hardware cost, as well as motor decoding algorithms with online update for BMIs [64]. More progress in this domain is expected in the future, particularly for disorders with fast-transient dynamics. For instance, the commonly used features of pathology in PD (e.g. the beta-band power within 13-30 Hz) are highly non-stationary and not present in all patients [29,32] necessitating the need for adaptive machine learning algorithms.

Conclusions and future outlook

Effective combination of AI and machine learning with modern neural interface circuits could lead to a new generation of brain implants with unprecedented therapeutic efficacy for a wide range of neurological and mental disorders. This paper reviewed the most recent developments in this domain, with a focus on neural devices with fully on-chip computation. Merging the ongoing developments on high-density probes [1,2] and flexible cortical grids [65] with smart processing circuits and edge AI could further advance such implants. Other future directions include the development of hybrid, multi-modal systems (e.g. the use of optical [66], acoustic, or magnetic sensing and/or stimulation), developing generic, configurable, and multi-purpose neural processors for different (or multi-symptom) brain disorders, and improving the energy efficiency, compactness, and adaptability of the on-chip algorithms. Brain-inspired neuromorphic computing offers an attractive solution, although current implementations for neuroprosthetic applications are still limited. The integration of emerging in-memory computing and memristive devices in neuromorphic architectures and improving the decoding accuracy and training of SNN algorithms could further enhance their efficiency and potential for therapeutic applications. Advances in this domain will benefit other implantable systems such as peripheral and spinal cord prostheses.

Conflict of interest statement

Nothing declared.

Acknowledgement

We acknowledge funding from the National Institute of Mental Health Grant R01-MH-123634.

References and recommended reading

Papers of particular interest, published within the period of review, have been highlighted as:

- · of special interest
- of outstanding interest
- Obaid A, Hanna M-E, Wu Y-W et al.: Massively parallel microwire arrays integrated with CMOS chips for neural recording. Sci Adv 2020, 6:eaay2789.

- Steinmetz NA, Aydin C, Lebedeva A et al.: Neuropixels 2.0: a miniaturized high-density probe for stable, long-term brain recordings. Science 2021, 372.
- Musk E, Neuralink and: An integrated brain-machine interface platform with thousands of channels. bioRxiv 2019, 21:e16194.
- Kaiju T, Inoue M, Hirata M et~al.: High-density mapping of primate digit representations with a 1152-channel μ ECoG array. J Neural Eng 2021, 18:036025.
- Uehlin JP, Smith WA, Pamula VR et al.: A 0.0023 mm²/ch. Deltaencoded, time-division multiplexed mixed-signal ECoG recording architecture with stimulus artifact suppression. IEEE Trans Biomed Circuits Syst 2019, 14:319-331.
- De Dorigo D, Moranz C, Graf H et al.: Fully immersible subcortical neural probes with modular architecture and a delta-sigma ADC integrated under each electrode for parallel readout of 144 recording sites. IEEE J Solid State Circuits 2018, **53**:3111-3125.
- Zanos S, Richardson AG, Shupe L et al.: The neurochip-2: an autonomous head-fixed computer for recording and stimulating in freely behaving monkeys. IEEE Trans Neural Syst Rehabil Eng 2011, 19:427-435.
- Liu X, Zhang M, Subei B et al.: The PennBMBI: design of a general purpose wireless brain-machine-brain interface system. IEEE International Symposium on Circuits and Systems (ISCAS) 2014:248-258.
- Zhou A, Santacruz SR, Johnson BC et al.: A wireless and artefact-free 128-channel neuromodulation device for closedloop stimulation and recording in non-human primates. Nat Biomed Eng 2019, 3:15-26.
- 10. Zhu B, Shin U, Shoaran M: Closed-loop neural interfaces with embedded machine learning. Proc. IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2020:1-
- 11. Kremen V. Brinkmann BH. Kim Let al.: Integrating brain implants with local and distributed computing devices: a next generation epilepsy management system. IEEE J Transl Eng Health Med 2018, 6:1-12.
- 12. Zhang M, Zhang L, Park JH et al.: A one-shot learning, onlinetuning, closed-loop epilepsy management SoC with 0.97 µJ/ Classification and 97.8% vector-based sensitivity. Proc. IEEE Symposium on VLSI Circuits, June 2021:1-2

This paper introduced a closed-loop epilepsy monitoring system, the first SoC with both online tuning and one-shot learning, achieving a record energy efficiency.

Zhu B, Farivar M, Shoaran M: ResOT: resource-efficient oblique trees for neural signal classification. IEEE Trans Biomed Circuits Syst 2020, 14:692-704

An oblique decision tree algorithm with energy-efficient regularization and weight-pruned structure, improving energy efficiency for seizure detection, tremor tracking, and BMI systems.

- O'Leary G, Groppe DM, Valiante TA et al.: NURIP: neural interface processor for brain-state classification and programmable-waveform neurostimulation. IEEE J Solid State Circuits 2018. 53:3150-3162.
- 15. Cheng C-H, Tsai P-Y, Yang T-Y et al.: A fully integrated 16channel closed-loop neural-prosthetic CMOS SoC with wireless power and bidirectional data telemetry for real-time efficient human epileptic seizure control. IEEE J Solid State Circuits 2018, 53:3314-3326.
- 16. Wang Y, Luo H, Chen Y et al.: A closed-loop neuromodulation chipset with 2-level classification achieving 1.5-Vpp CM interference tolerance, 35-dB stimulation artifact rejection in 0.5 ms and 97.8%-sensitivity seizure detection. IEEE Trans Biomed Circuits Syst 2021, **15**:802-819

A closed-loop neuromodulation chipset for epilepsy with high commonmode Interference tolerance that integrates a 2-level classifier, achieving a low average classification power.

17. Figee M, Mayberg H: The future of personalized brain stimulation. *Nat Med* 2021, **27**:196-197.

- 18. Ezzyat Y, Wanda PA, Levy DF et al.: Closed-loop stimulation of temporal cortex rescues functional networks and improves memory. Nat Commun 2018, 9:1-8.
- 19. Mankin EA, Fried I: Modulation of human memory by deep brain stimulation of the entorhinal-hippocampal circuitry. Neuron 2020, 106:218-235.
- 20. Lozano AM, Lipsman N, Bergman H et al.: Deep brain stimulation: current challenges and future directions. Nat Rev Neurol 2019, 15:148-160.
- 21. Krauss JK, Lipsman N, Aziz T $et\ al.$: Technology of deep brain stimulation: current status and future directions. Nat Rev Neurol 2021, 17:75-87.
- 22. Sullivan CR, Olsen S, Widge AS: Deep brain stimulation for psychiatric disorders: from focal brain targets to cognitive networks. Neurolmage 2020:117515.
- 23. Lo M-C, Widge AS: Closed-loop neuromodulation systems: next-generation treatments for psychiatric illness. Int Rev Psychiatry 2017, 29:191-204.
- 24. Molina R, Okun MS, Shute JB et al.: Report of a patient undergoing chronic responsive deep brain stimulation for Tourette syndrome: proof of concept. J Neurosurg 2017, **129**:308-314.
- 25. Chang S-Y, Wu B-C, Liou Y-L et al.: An ultra-low-power dualmode automatic sleep staging processor using neuralnetwork-based decision tree. IEEE Trans Circuits Syst I Regul Pap 2019, 66:3504-3516.
- 26. Aslam AR, Igbal T, Aftab M et al.: A 10.13uJ/classification 2channel deep neural network-based SoC for emotion detection of autistic children. IEEE Custom Integrated Circuits Conference (CICC) 2020:1-2.
- 27. Fang W-C, Wang K-Y, Fahier N et al.: Development and validation of an EEG-based real-time emotion recognition system using edge AI computing platform with convolutional neural network system-on-chip design. IEEE J Emerg Sel Top Circuits Syst 2019, 9:645-657.
- 28. Taufique Z, Zhu B, Coppola G et al.: A low power multi-class migraine detection processor based on somatosensory evoked potentials. IEEE Trans Circuits Syst II Express Briefs 2021,
- 29. Yao L, Brown P, Shoaran M: Improved detection of Parkinsonian resting tremor with feature engineering and Kalman filtering. Clin Neurophysiol 2020, 131:274-284
- 30. He S, Baig F, Mostofi A et al.: Closed-loop deep brain stimulation for essential tremor based on thalamic local field potentials. Mov Disord 2021, 36:863-873.
- 31. Watts J, Khojandi A, Shylo O et al.: Machine learning's application in deep brain stimulation for Parkinson's disease: a review. Brain Sci 2020, 10:809.
- Meidahl AC, Tinkhauser G, Herz DM et al.: Adaptive deep brain stimulation for movement disorders: the long road to clinical therapy. Mov Disord 2017, 32:810-819.
- 33. Yao L, Brown P, Shoaran M: Resting tremor detection in Parkinson's disease with machine learning and Kalman filtering. Proc. IEEE Biomedical Circuits and Systems Conference, June 2019:1-4.
- 34. Broccard FD, Joshi S, Wang J et al.: Neuromorphic neural interfaces: from neurophysiological inspiration to biohybrid coupling with nervous systems. J Neural Eng 2017, 14.
- 35. Corradi F, Indiveri G: A neuromorphic event-based neural recording system for smart brain-machine-interfaces. IEEE Trans Biomed Circuits Syst 2015, 9:699-709.
- 36. Qiao N, Mostafa H, Corradi F et al.: A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128K synapses. Front Neurosci 2015, 9:141.
- 37. Boi F, Moraitis T, Feo VDe et al.: A bidirectional brain-machine interface featuring a neuromorphic hardware decoder. Front Neurosci 2016, 10:563.

- 38. Venkatraman S, Elkabany K, Long JD et al.: A system for neural recording and closed-loop intracortical microstimulation in awake rodents. IEEE Trans Biomed Eng 2008, 56:15-22
- Guggenmos DJ. Azin M. Barbay S et al.: Restoration of function after brain damage using a neural prosthesis. Proc Natl Acad Sci U S A 2013, 110:21177-21182.
- 40. Azin M, Guggenmos DJ, Barbay S et al.: A battery-powered activity-dependent intracortical microstimulation IC for brainmachine-brain interface. IEEE J Solid State Circuits 2011, 46:731-745
- 41. Azin M, Guggenmos DJ, Barbay S et al.: A miniaturized system for spike-triggered intracortical microstimulation in an ambulatory rat. IEEE Trans Biomed Eng 2011, 58:2589-2597
- 42. O'Leary G, Xu J, Long L et al.: A neuromorphic multiplier-less bit-serial weight-memory-optimized 1024-tree brain-state classifier and neuromodulation SoC with an 8-channel noiseshaping SAR ADC array. IEEE International Solid-state Circuits Conference (ISSCC) 2020:402-404.
- 43. Moradi S, Qiao N, Stefanini F et al.: A scalable multicore architecture with heterogeneous memory structures for dynamic neuromorphic asynchronous processors (DYNAPs). IEEE Trans Biomed Circuits Syst 2017, 12:106-122.
- 44. Sharifshazileh M, Burelo K, Sarnthein J et al.: An electronic neuromorphic system for real-time detection of high frequency oscillations (HFO) in intracranial EEG. Nat Commun

Authors present a neuromorphic spiking neural network (SNN) approach to High Frequency Oscillations (HFO) extraction for seizure detection in enilensy

- Chen GK, Kumar R, Sumbul HE et al.: A 4096-neuron 1Msynapse 3.8-pJ/SOP spiking neural network with on-chip STDP learning and sparse weights in 10-nm FinFET CMOS. IEEE J Solid State Circuits 2018, 54:992-1002.
- 46. Merolla PA, Arthur JV, Alvarez-Icaza R et al.: A million spikingneuron integrated circuit with a scalable communication network and interface. Science 2014, 345:668-673.
- 47. Benjamin BV, Gao P, McQuinn E et al.: Neurogrid: a mixedanalog-digital multichip system for large-scale neural simulations. Proc IEEE 2014, 102:699-716.
- 48. Knag P, Kim JK, Chen T et al.: A sparse coding neural network ASIC with on-chip learning for feature extraction and encoding. IEEE J Solid State Circuits 2015, 50:1070-1079.
- Cruz-Albrecht JM, Derosier T, Srinivasa N: A scalable neural chip with synaptic electronics using CMOS integrated memristors. Nanotechnology 2013, 24:384011.
- Seo J-S, Brezzo B, Liu Y et al.: A 45nm CMOS neuromorphic chip with a scalable architecture for learning in networks of spiking neurons. IEEE Custom Integrated Circuits Conference (CICC)
- 51. Park JH, Tan JSY, Wu H et al.: 1225-channel neuromorphic retinal-prosthesis SoC with localized temperature-regulation. IEEE Trans Biomed Circuits Syst 2020, 14:1230-1240

A high-density retinal implant with in-pixel neuromorphic image processing and temperature- regulation circuits, leading to a low power consumption without any local hot spots.

- 52. Truong ND, Nguyen AD, Kuhlmann Let al.: Integer convolutional neural network for seizure detection. IEEE J Emerg Sel Top Circuits Syst 2018, 8:849-857.
- 53. Lee S-Y, Hung Y-W, Chang Y-T et al.: RISC-V CNN coprocessor for real-time epilepsy detection in wearable application. IEEE Trans Biomed Circuits Syst 2021, 15:679-691.
- 54. Kiral-Kornek I. Mendis D. Nurse ES et al.: TrueNorth-enabled real-time classification of EEG data for brain-computer interfacing. IEEE EMBC 2017:1648-1651.
- Nurse E, Mashford BS, Yepes AJ et al.: Decoding EEG and LFP signals using deep learning: heading TrueNorth. ACM International Conference on Computing Frontiers 2016:259-266.
- 56. Mashford BS, Yepes AJ, Kiral-Kornek I et al.: Neural-networkbased analysis of EEG data using the neuromorphic TrueNorth chip for brain-machine interfaces. IBM J Res Dev 2017, 61:7 1-
- 57. Berger TW, Song D, Chan RH et al.: A hippocampal cognitive prosthesis: multi-input, multi-output nonlinear modeling and VLSI implementation. IEEE Trans Neural Syst Rehabil Eng 2012. 20:198-211.
- 58. Jarosiewicz B, Morrell M: The RNS system: brain-responsive neurostimulation for the treatment of epilepsy. Expert Rev Med Devices 2021, 18:129-138.
- 59. Stanslaski S, Herron J, Chouinard T et al.: A chronically implantable neural coprocessor for investigating the treatment of neurological disorders. IEEE Trans Biomed Circuits Syst 2018, 12:1230-1245.
- 60. Yoon D-Y, Pinto S, Chung S et al.: A 1024-channel simultaneous recording neural SoC with stimulation and real-time spike detection. Proc. IEEE Symposium on VLSI Circuits 2021:1-2.
- 61. Shoaran M, Haghi BA, Taghavi M et al.: Energy-efficient classification for resource-constrained biomedical applications. IEEE J Emerg Sel Top Circuits Syst 2018, 8:693-707.
- 62. Anderson DN, Osting B, Vorwerk J et al.: Optimized programming algorithm for cylindrical and directional deep brain stimulation electrodes. J Neural Eng 2018, 15:026005.
- 63. Chua A, Jordan MI, Muller R: A 1.5 nJ/cls unsupervised online learning classifier for seizure detection. Proc. IEEE Symposium on VLSI Circuits 2021:1-2.
- 64. Shaikh S, So R, Sibindi T et al.: Lightweight reinforcement algorithms for autonomous, scalable intra-cortical brain machine interfaces. bioRxiv 2020.
- 65. Schiavone G, Fallegger F, Kang X et al.: Soft, implantable bioelectronic interfaces for translational research. Adv Mater 2020, 32:1906512.
- 66. Gagnon-Turcotte G, Keramidis I, Ethier C et al.: A wireless electro-optic headstage with a 0.13-μm CMOS custom integrated DWT neural signal decoder for closed-loop optogenetics. IEEE Trans Biomed Circuits Syst 2019, 13:1036-1051.