ECE 622 Lab 1
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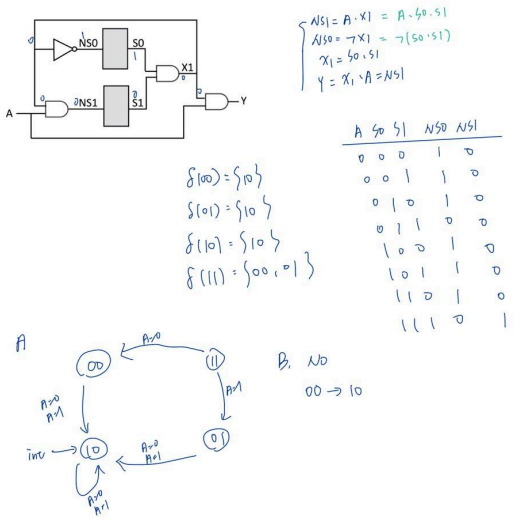
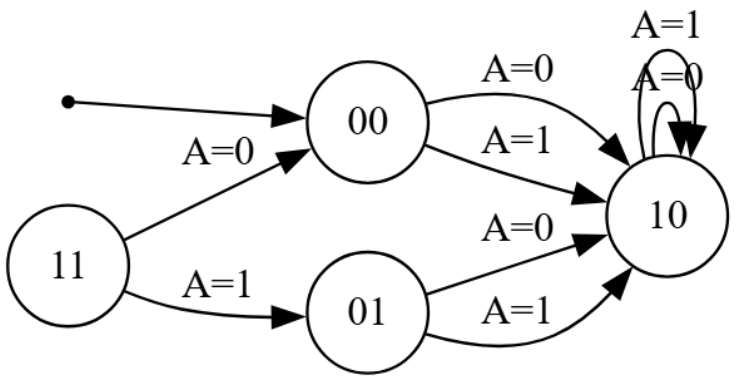
A.1

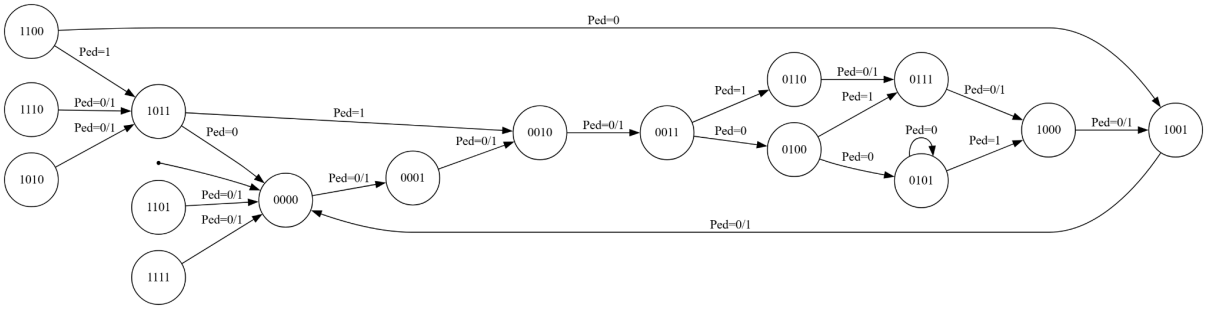
ex1: use the following method to draw ex1 transition state graph





stoplight1: write a testbench for stoplight module, used to test all state transitions and display the results based on changes in ped

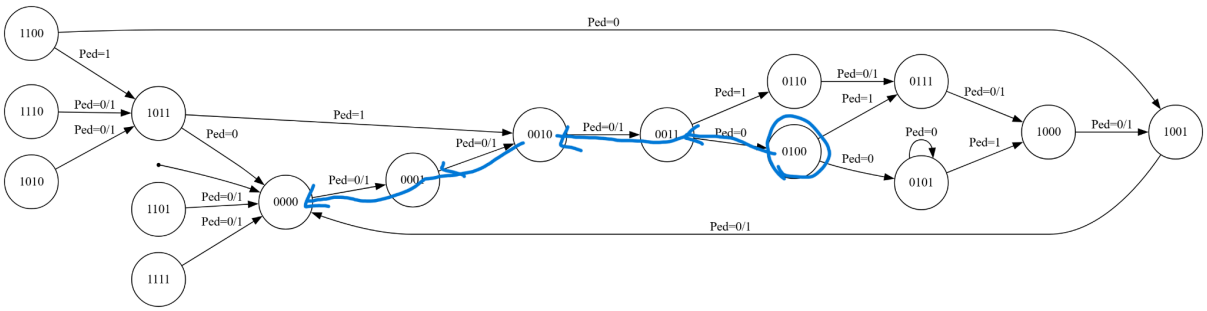
```
S=0000  Ped=0 -> 0001   Ped=1 -> 0001
S=0001  Ped=0 -> 0010   Ped=1 -> 0010
S=0010  Ped=0 -> 0011   Ped=1 -> 0011
S=0011  Ped=0 -> 0100   Ped=1 -> 0110
S=0100  Ped=0 -> 0101   Ped=1 -> 0111
S=0101  Ped=0 -> 0101   Ped=1 -> 1000
S=0110  Ped=0 -> 0111   Ped=1 -> 0111
S=0111  Ped=0 -> 1000   Ped=1 -> 1000
S=1000  Ped=0 -> 1001   Ped=1 -> 1001
S=1001  Ped=0 -> 0000   Ped=1 -> 0000
S=1010  Ped=0 -> 1011   Ped=1 -> 1011
S=1011  Ped=0 -> 0000   Ped=1 -> 0010
S=1100  Ped=0 -> 1001   Ped=1 -> 1011
S=1101  Ped=0 -> 0000   Ped=1 -> 0000
S=1110  Ped=0 -> 1011   Ped=1 -> 1011
S=1111  Ped=0 -> 0000   Ped=1 -> 0000
```



A.2

ex1: according to transition state graph 00 will never reach target state 11

stoplight1: 0000(ped=0/1)->0001(ped=0/1)->0010(ped=0/1)->0011(ped=0)->0100



A.3 (not sure : should we add initial state?)

ex1:

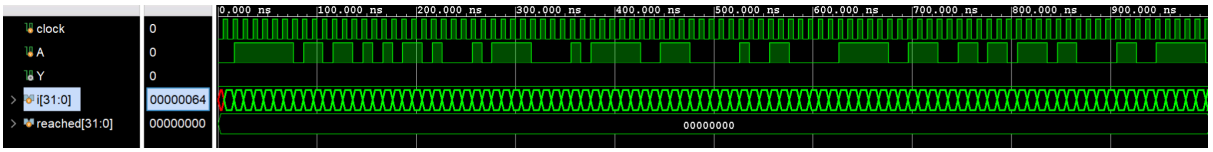
A	B
1	1
2	1
3	1
4	1
5	1
6	1
7	1
8	1
9	1
10	1
11	1
12	1
13	1
14	1
15	1
16	1
17	1
18	1
19	1
20	1

stoplight1:

1	1
2	2
3	3
4	5
5	7
6	8
7	9
8	9
9	9
10	9
11	9
12	9
13	9
14	9
15	9
16	9
17	9
18	9
19	9
20	9

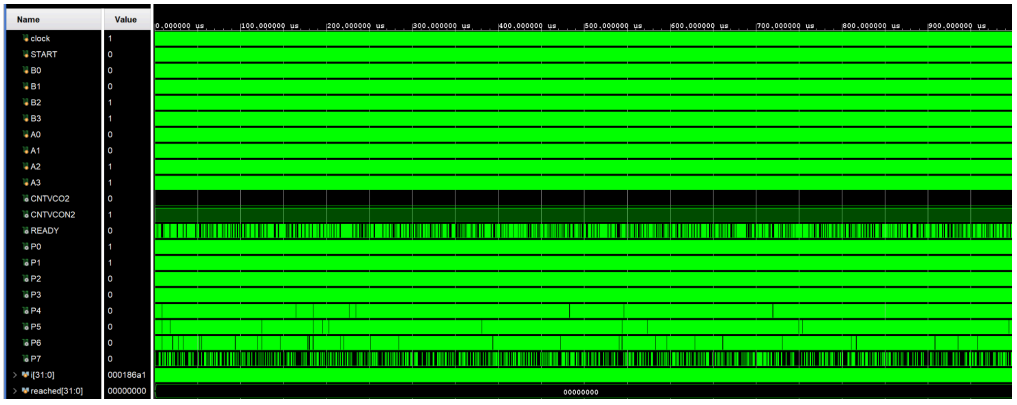
A.4

ex1: initial state will never reach target state



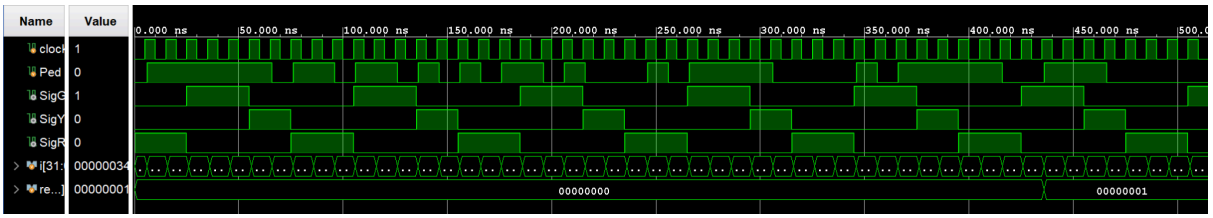

```
ex1: Target state 11 NOT reached within 100000 cycles (TIMED OUT)
$finish called at time : 1000006 ns : File "C:/Users/maxf2/Desktop/embedded system/lab1_files/tb_ex1.v" Line 51
```

ex2:initial state will never reach target state



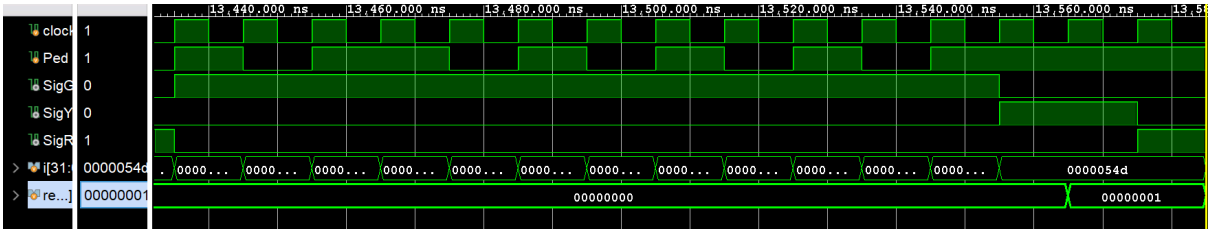

```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_ex2_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:10 . Memory (MB): peak = 25
run -all
ex2: Target state 11111111111111 NOT reached within 100000 cycles (TIMED OUT)
```

stoplight1:




```
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:10 . Memory (MB): peak = 2562.023 ; gain = 0.000
ERROR: [Common 17-180] Spawn failed: No error
run -all
stoplight1: Target state 0100 REACHED at cycle 52
$finish called at time : 516 ns : File "C:/Users/maxf2/Desktop/embedded system/lab1_files/tb_soptlight1.v" Line 39
```

stopligh2:




```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_stoplight2_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:12 ; elapsed = 00:00:11 . Memory (MB): peak = 2658.184 ; gain = 0.000
run -all
stoplight2: Target state 01000 REACHED at cycle 1357
$finish called at time : 13585 ns : File "C:/Users/maxf2/Desktop/embedded system/lab1 files/tb stoplight2.v" Line 41
```

stoplight1 testbench

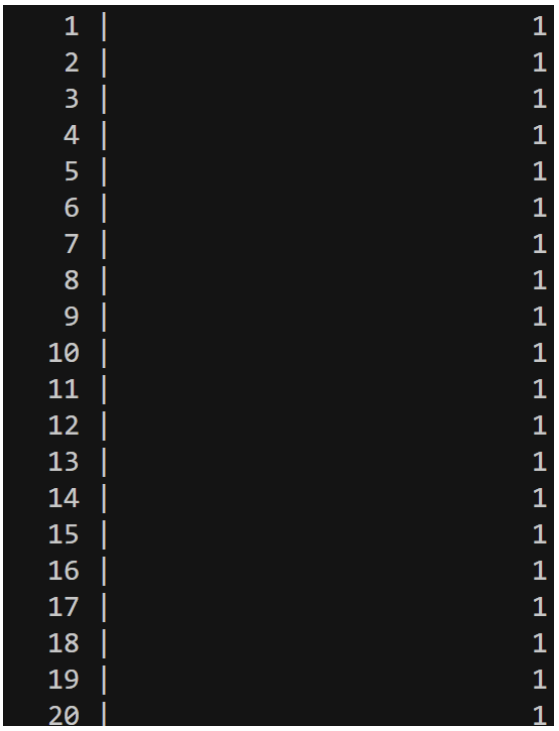
```
`timescale 1ns/1ps

module tb_stoplight1;
    reg clock, Ped;
    wire SigG, SigY, SigR;
    integer i;
    integer reached;

    stoplight1 spotlight1 (
        .clock(clock),
        .Ped(Ped),
        .SigG(SigG),
        .SigY(SigY),
        .SigR(SigR)
    );

    initial clock = 0;
    always #5 clock = ~clock;

    initial begin
        reached = 0;
        Ped = 0;
        spotlight1.S3 = 0;
        spotlight1.S2 = 0;
        spotlight1.S1 = 0;
        spotlight1.S0 = 0;

        for (i = 1; i <= 100000; i = i + 1) begin
            Ped = $random % 2;
            @(posedge clock);

            // Target:0100
            if (spotlight1.S3 === 0 && spotlight1.S2 === 1 && spotlight1.S1 === 0 && spotlight1.S0 === 0) begin
                $display("stoplight1: Target state 0100 REACHED at cycle %0d", i);
                reached = 1;
                @(posedge clock);
                @(posedge clock);
                $finish;
            end
        end

        if (reached == 0)
            $display("stoplight1: Target state 0100 NOT reached within 100000 cycles (TIMED OUT)");

        $finish;
    end

endmodule
```

A.5

The result for stoplight1 is consistent with the result from A.2. We know that stoplight1 will reach the target state 0100 in A.2 and A.4 simulation shows the same result.

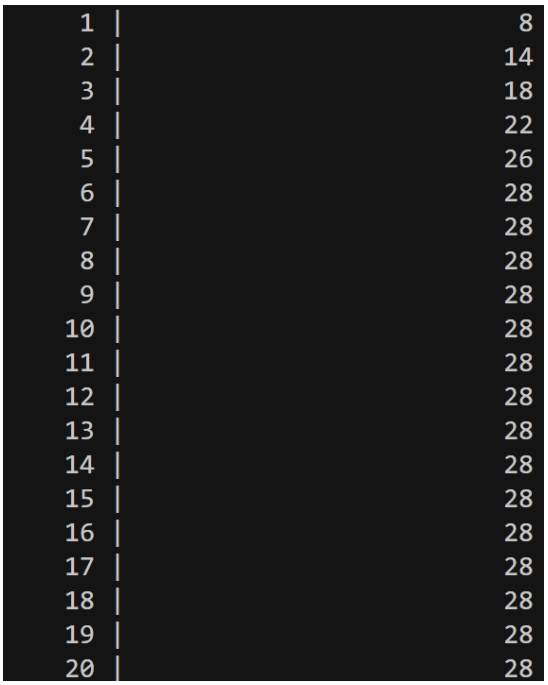
C

ex1:



1	1
2	1
3	1
4	1
5	1
6	1
7	1
8	1
9	1
10	1
11	1
12	1
13	1
14	1
15	1
16	1
17	1
18	1
19	1
20	1

ex5:



1	8
2	14
3	18
4	22
5	26
6	28
7	28
8	28
9	28
10	28
11	28
12	28
13	28
14	28
15	28
16	28
17	28
18	28
19	28
20	28