TO: Prof. Pierre-Emmanuel Gaillardon, Course Instructor
FROM: David Venegas
DATE: February 9th, 2024
SUBJECT: Post-Lab 02 (Interrupts)

1. **Why can't you use both pins PA0 and PC0 for external interrupts at the same time?**

Because they are inputs to the same multiplexer, as they belong to the same pin group.

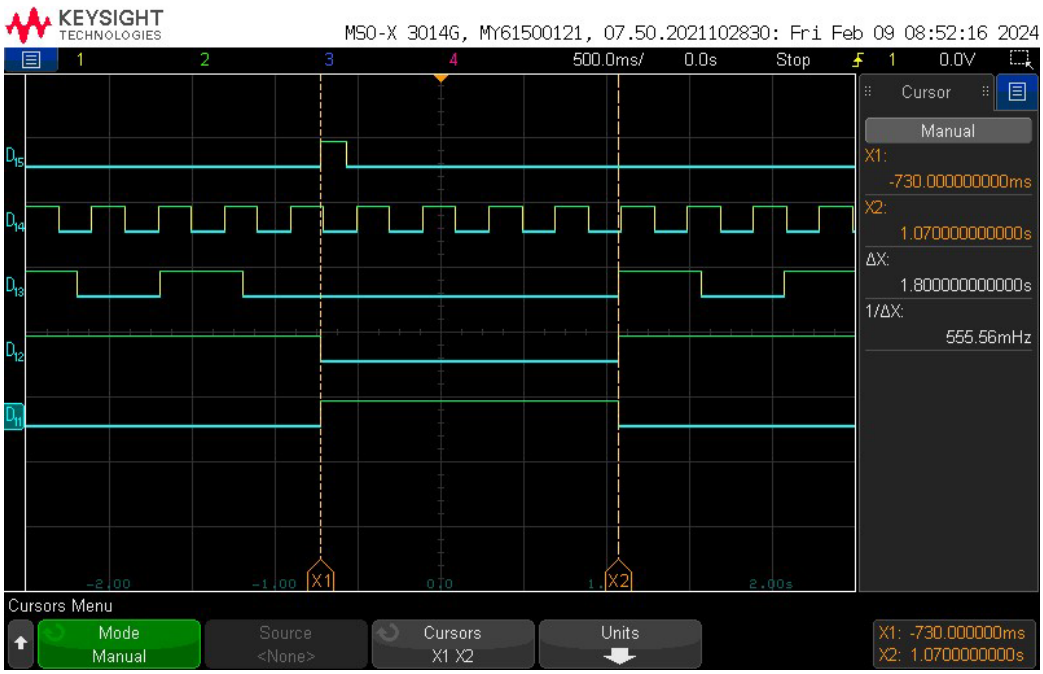
2. **What software priority level gives the highest priority? What level gives the lowest?**

Four software priorities are available [0-3] where 0 is top priority and 3 will be the lowest.

3. **How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?**

Each IPR register contains four 8-bit regions to set the priority of an interrupt; the NVIC within the STM32F0 only has the uppermost two bits from these regions implemented, giving four possible configurable priority levels (0-3).

4. **What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.**



D_{15} (PA0) – Button
D_{14} (PC7) – Blue LED
D_{13} (PC6) – Red LED
D_{12} (PC9) - Green LED
D_{11} (PC8) – Orange LED

From the Oscilloscope/Logic Analyzer: ~1.8 sec of delay

5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

Most peripherals have a status register containing flag bits for pending interrupt requests; however, even in those without dedicated registers, most interrupts set status flags within their peripheral. These flags are necessary to generate interrupt requests. Typically, you will need to clear the matching status bit manually for the interrupt condition that you are handling; otherwise, the interrupt will repeat continuously because the request never acknowledges as complete.