TO: Prof. Pierre-Emmanuel Gaillardon, Course Instructor
FROM: David Venegas
DATE: February 2nd, 2024
SUBJECT: Post-Lab 01 (Intro/GPIO)

1. What are the GPIO control registers that the lab mentions? Briefly describe each of their functions.

Each of the GPIO ports has four 32-bit memory-mapped control registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR) to configure up to 16 I/Os. The GPIOx_MODER register is used to select the I/O mode (input, output, AF, analog). The GPIOx_OTYPER and GPIOx_OSPEEDR registers are used to select the output type (push-pull or open-drain) and speed. The GPIOx_PUPDR register is used to select the pull-up/pull-down whatever the I/O direction.

2. What values would you want to write to the bits controlling a pin in the GPIOx_MODER register in order to set it to analog mode?

[11]: Analog mode

3. Examine the bit descriptions in GPIOx_BSRR register: which bit would you want to set to clear the fourth bit in the ODR?

BR[19] = (1 << 19)

4. Perform the following bitwise operations:

- **0xAD | 0xC7** = 0xEF
- **0xAD & 0xC7** = 0x85
- **0xAD & ~(0xC7)** = 0x28
- **0xAD ^0xC7** = 0x6A

5. How would you clear the 5th and 6th bits in a register while leaving the other's alone?

```
&= ~((1 << 5) | (1 << 6))
```

6. What is the maximum speed the STM32F072R8 GPIO pins can handle in the lowest speed setting?

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	

7. What RCC register would you manipulate to enable the following peripherals: (use the comments next to the bit defines for better peripheral descriptions)

- **TIM1 (TIMER1):** RCC_APB2ENR
- **DMA1:** RCC_AHBENR
- **I2C1:** RCC_APB1ENR