Lab 2 Report

Name: Joshua Dong

UT EID: jid295

Section: Wed. 11 - 12p. (16420)

Problem No: 8.C

Checklist:

1. Karnaugh Map + detailed work done to get the Final Equation (handwork)
2. Logic Circuit drawing with all NANDs or all NORs (handwork)
3. Truth Table and Minimized equations from LogicAid
4. Circuit in SimUaid implemented with all NANDs or all NORs
    a. Should meet the number of gates specified in textbook
    b. Use virtual connections
    c. Use the minimum number of input inverters