

Lab 2 Report

Name: Joshua Dong

UT EID: jid295

Section: Wed. 11 - 12p. (16420)

Problem No: 8.C

Checklist:

1. Karnaugh Map + detailed work done to get the Final Equation (handwork)
2. Logic Circuit drawing with all NANDs or all NORs (handwork)
3. Truth Table and Minimized equations from LogicAid
4. Circuit in SimUaid implemented with all NANDs or all NORs
 - a. Should meet the number of gates specified in textbook
 - b. Use virtual connections
 - c. Use the minimum number of input inverters

Problem Statement

Design a circuit which will yield the product of two binary numbers, n_2 and m_2 , where $00_2 \leq n_2 \leq 11_2$ and $000_2 \leq m_2 \leq 101_2$. For example, if $n_2 = 10_2$ and $m_2 = 001_2$, then the product is $n_2 \times m_2 = 10_2 \times 001_2 = 0010_2$. Let the variables A and B represent the first and second digits of n_2 , respectively (i.e., in this example $A = 1$ and $B = 0$). Let the variables C, D, and E represent the first, second, and third digits of m_2 , respectively (in this example $C = 0$, $D = 0$, and $E = 1$). Also let the variables W, X, Y, and Z represent the first, second, third, and fourth digits of the product. (In this example $W = 0$, $X = 0$, $Y = 1$, and $Z = 0$.) Assume that $m_2 > 101_2$ never occurs as a circuit input.

Karnaugh Map

In the tables that follow, $a = 1$ on the left, $a = 0$ on the right.

de \ bc	00	01	11	10
00	0000	0010	0110	0100
01	1000	1010	xxxx	xxxx
11	1100	1111	xxxx	xxxx
10	0000	0011	1001	0110

de \ bc	00	01	11	10
00	0000	0000	0000	0000
01	0000	0000	xxxx	xxxx
11	0100	0101	xxxx	xxxx
10	0000	0001	0011	0010

We can break this k-map down for each component W, X, Y, Z:

W

de \ bc	00	01	11	10
00	0	0	0	0
01	1	1	x	x
11	1	1	x	x
10	0	0	1	0

de \ bc	00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	0	0	x	x
10	0	0	0	0

$$W = A(B + C)(C + D)(C + E).$$

(continued from previous page)

X

bc \ de	00	01	11	10
	00	01	11	10
00	0	0	1	1
01	0	0	x	x
11	1	1	x	x
10	0	0	0	1

bc \ de	00	01	11	10
	00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	1	1	x	x
10	0	0	0	0

$$X = (B + D)(C + D)(B' + C + E')(A + C)$$

Y

bc \ de	00	01	11	10
	00	01	11	10
00	0	1	1	0
01	0	1	x	x
11	0	1	x	x
10	0	1	0	1

bc \ de	00	01	11	10
	00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	0	0	x	x
10	0	0	1	1

$$Y = A'BD + AB'E + AD'E + BDE'.$$

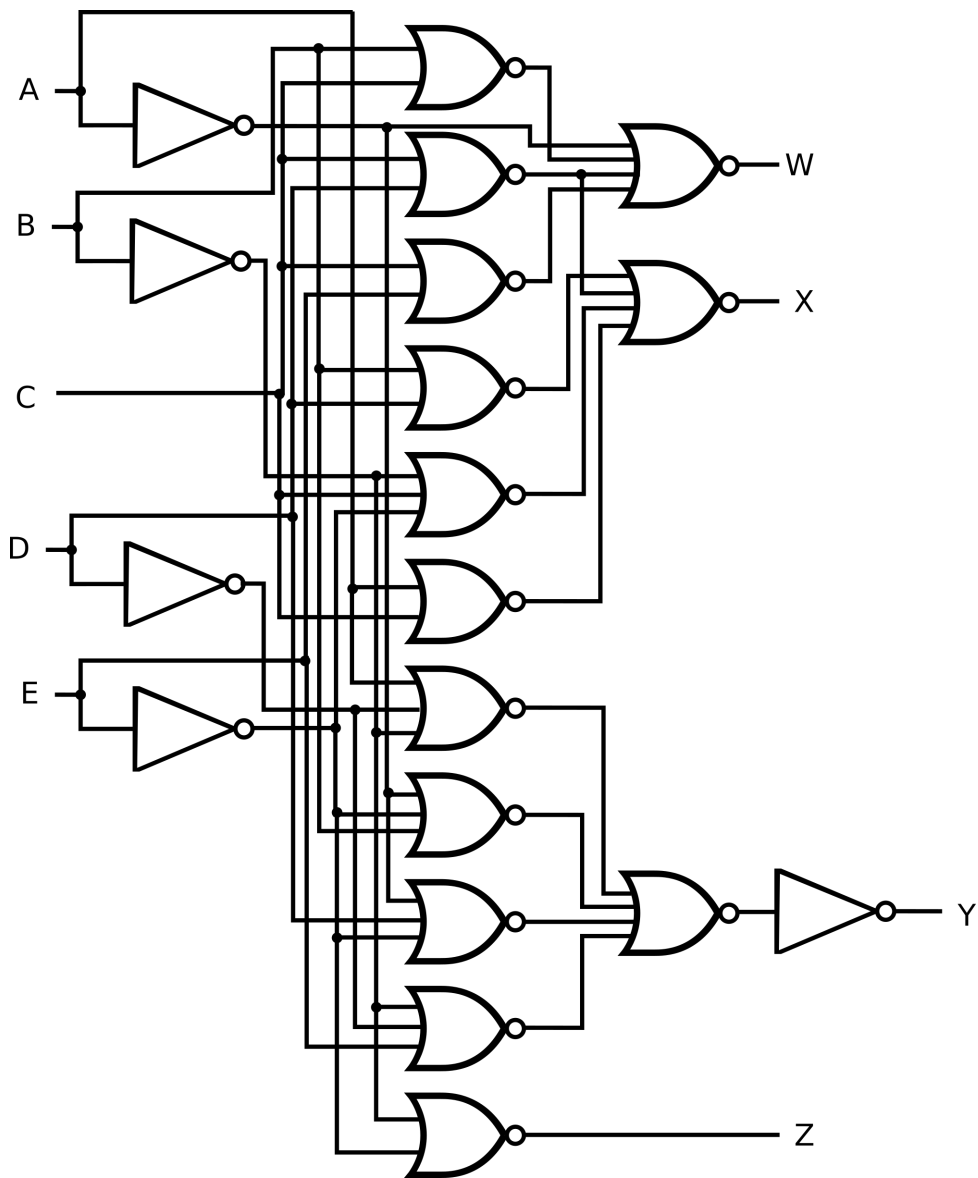
Z

bc \ de	00	01	11	10
	00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	0	1	x	x
10	0	1	1	0

bc \ de	00	01	11	10
	00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	0	1	x	x
10	0	1	1	0

$$Z = BE$$

Gate Drawings



LogicAid

LogicAid - TT_O

File Input Routine View Window Help

TT

Input Variable Names: A B C D E
Output Function Names: W X Y Z

00000	0000
00001	0000
00010	0000
00011	0000
00100	0000
00101	0000
00110	----
00111	----
01000	0000
01001	0001
01010	0010
01011	0011
01100	0100
01101	0101
01110	----
01111	----
10000	0000
10001	0010
10010	0100
10011	0110
10100	1000
10101	1010
10110	1100
10111	1110
11000	0000
11001	0011
11010	0110
11011	0101
11100	1100
11101	1111
11110	----
11111	----

TT_O

Simplification Routine: Petrick 5

W = $\langle A \rangle \langle C \rangle$

X = $\langle B + D \rangle \langle C + D \rangle \langle A + D' \rangle$

X = $\langle B + D \rangle \langle C + D \rangle \langle A + C \rangle$

Y = $\langle A + B \rangle \langle A + D \rangle \langle B + E \rangle \langle D + E \rangle \langle A' + B' + D' + E' \rangle$

Z = $\langle B \rangle \langle E \rangle$

SimuAid

