Lab 3.1 Report

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Section: MW 11-12 AM

Problem No: 12.10.D

Submission CheckList

- Answer the preparatory questions.
- Submit the cover sheet
- Karnaugh maps and simplification for each input of the D FlipFlop. [20] points
- Attach a screenshot of your SimUAid circuit
- The SimuAid circuit file

Problem Statement

Design a counter which counts in the sequence that has been assigned to you. Use D flip-flops and NAND gates. Simulate your design using SimUaid. Given sequence: 000, 100, 001, 110, 101, 111, (repeat) 000, ...

Preparatory Questions

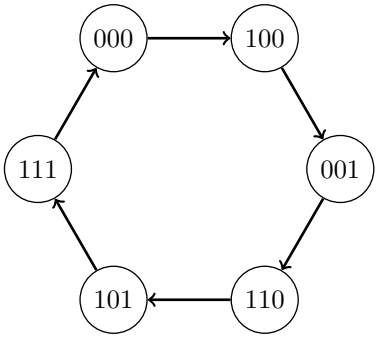
1. Explain the term Asynchronous input?
   Asynchronous input refers to input that is not constrained by the clock signal. In this context, an asynchronous input could set or reset the flip-flop regardless of the status of the clock signal.

2. How can you set the output of a D Flip-Flop to logic 0 without using its clock input?
   The flip-flop would need to be reset using its asynchronous reset function (R) pin. Simply send the a logical 0 to the R pin. Take care that the S pin does not have logical high.

3. How can you set the output of a D Flip-Flop to logic 1 without using its clock input?
   Similar to setting a D flip-flop to logic 0, simply send a logical 0 to pin S.

State Graph

We can represent the solution to implement using the state graph below:



State Table

We shall start by writing the state table for the sequence above. We shall be using D-Flip Flops for this exercise. Since its a 3 bit counter, we need 3 D FlipFlops to implement the sequence. Next, we create a truth table for the D-Input of the flip-flops:

Present state			Next State		
A	B	C	A+	B+	C+
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	X	X	X
0	1	1	X	X	X
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	0	0	0

We now have the truth table for next states. This table can get Boolean expressions for logic.

Karnaugh Map

For a three-bit counter, the Karnaugh maps for the next state are as follows:

A+

a \ bc	00	01	11	10
0	1	1	X	X
1	0	1	0	1

B+

a \ bc	00	01	11	10
0	0	1	X	X
1	0	1	0	0

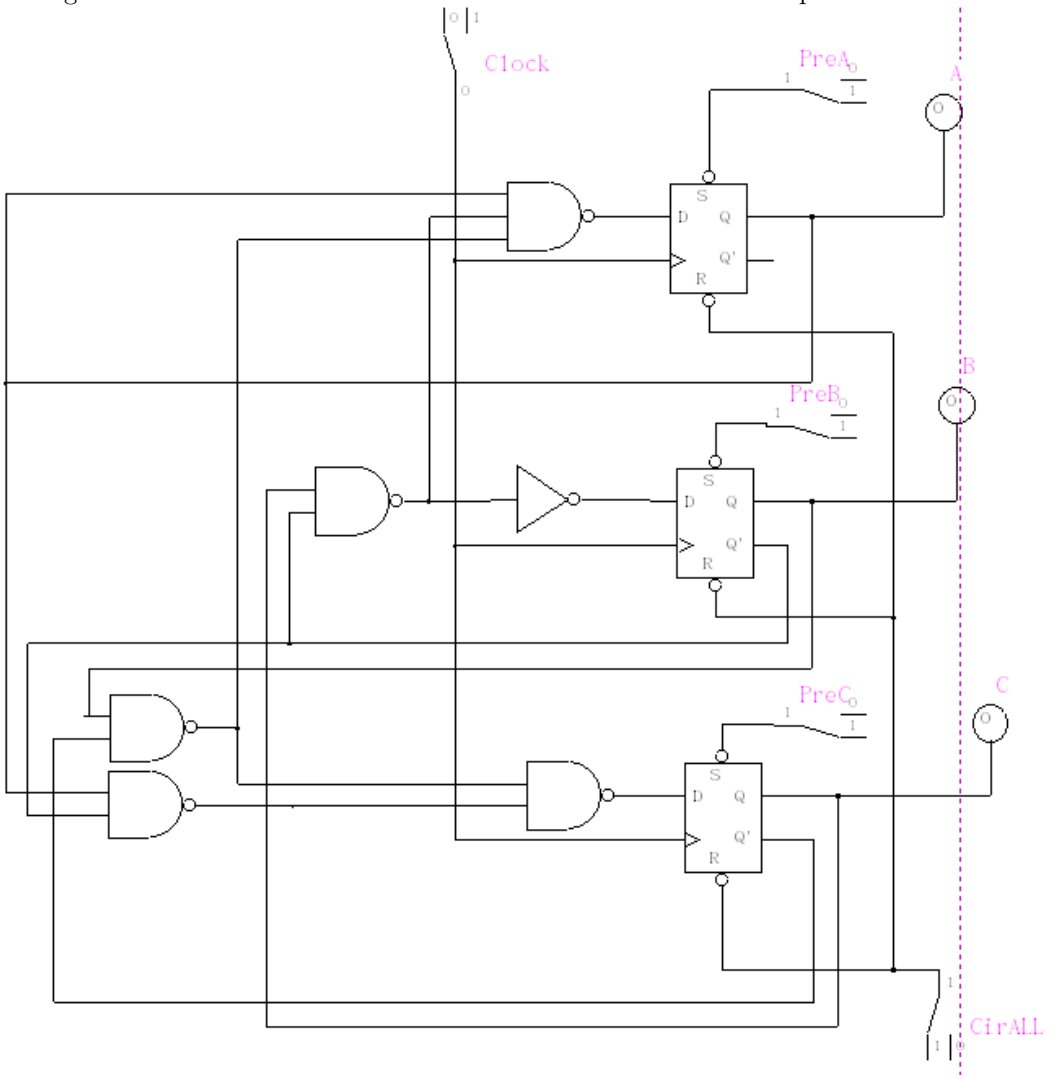
C+

a \ bc	00	01	11	10
0	0	0	X	X
1	1	1	0	1

After minimization, we get the following equations:
$A+ = A' + B'C + BC'$
$B+ = B'C$
$C+ = AB' + BC'$

Circuit

It's time to draw the circuit in SimUAid using only D-Flip-Flops, NAND gates, and inverters. Here is a logic circuit for the above truth tables. Note that the S and R inputs are active low.



Note that if needed, the single inverter used could be substituted with a single NAND gate.