Lab 2 Report

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Section: Wed. 11 - 12p. (16420)

Problem No: 8.C

Checklist:

- 1. Karnaugh Map + detailed work done to get the Final Equation (handwork)
- 2. Logic Circuit drawing with all NANDs or all NORs (handwork)
- 3. Truth Table and Minimized equations from LogicAid
- 4. Circuit in SimUaid implemented with all NANDs or all NORs
 - a. Should meet the number of gates specified in textbook
 - b. Use virtual connections
 - c. Use the minimum number of input inverters

Problem Statement

Design a circuit which will yield the product of two binary numbers, n_2 and m_2 , where $00_2 \le n_2 \le 11_2$ and $000_2 \le m_2 \le 101_2$. For example, if $n_2 = 10_2$ and $m_2 = 001_2$, then the product is $n_2 \times m_2 = 10_2 \times 001_2 = 0010_2$. Let the variables A and B represent the first and second digits of n_2 , respectively (i.e., in this example A = 1 and B = 0). Let the variables C, D, and E represent the first, second, and third digits of m_2 , respectively (in this example C = 0, D = 0, and E = 1). Also let the variables W, X, Y, and Z represent the first, second, third, and fourth digits of the product. (In this example W = 0, X = 0, Y = 1, and Z = 0.) Assume that $m_2 > 101_2$ never occurs as a circuit input.

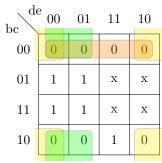
Karnaugh Map

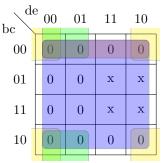
In the tables that follow, a = 1 on the left, a = 0 on the right.

$\frac{\mathrm{d}}{\mathrm{bc}}$	9 00	01	11	10
00	0000	0010	0110	0100
01	1000	1010	xxxx	xxxx
11	1100	1111	xxxx	XXXX
10	0000	0011	1001	0110

bc de	9 00	01	11	10
00	0000	0000	0000	0000
01	0000	0000	xxxx	XXXX
11	0100	0101	xxxx	XXXX
10	0000	0001	0011	0010

We can break this k-map down for each component W, X, Y, Z: W





$$W = A(B+C)(C+D)(C+E).$$

(continued from previous page)

X

bc de	00	01	11	10
00	0	0	1	1
01	0	0	x	х
11	1	1	x	х
10	0	0	0	1

$\frac{\mathrm{d}\epsilon}{\mathrm{d}\epsilon}$	00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	1	1	x	X
10	0	0	0	0
			•	

X = (B+D)(C+D)(B'+C+E')(A+C)

Y

bc de	9 00	01	11	10
00	0	1	1	0
01	0	1	x	x
11	0	1	Х	х
10	0	1	0	1

$\frac{\mathrm{d}\epsilon}{\mathrm{bc}}$	9 00	01	11	10
00	0	0	0	0
01	0	0	х	x
11	0	0	х	х
10	0	0	1	1

Y = (A+B)(A+D)(B+E)(D+E)(A'+B'+D'+E').

Z

bc de	9 00	01	11	10
00	0	0	0	0
01	0	0	x	x
11	0	1	X	Х
10	0	1	1	0

bc de	9 00	01	11	10
00	0	0	0	0
01	0	0	х	x
11	0	1	X	x
10	0	1	1	0

Z = BE

Gate Drawings

