Claire Jeongeun Kim

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Los Angeles, CA, USA

Education

- **University of Southern California** *Aug 2023 - Present*
  Ph.D. in Electrical and Computer Engineering Los Angeles, USA
- **Seoul National University of Science and Technology** *Mar 2021 - Feb 2023*
  M.S. in Electronic Engineering Seoul, South Korea
  - Thesis: Parallel stochastic computing architecture for computationally intensive applications
- **Seoul National University of Science and Technology** *Mar 2013 - Feb 2017*
  B.S. in Electronic Engineering Seoul, South Korea

Research Experience

- **Agile Computer Organization (ACORN) Research Group** *Aug 2023 - Present*
  Graduate Researcher (Advised by Prof. Christopher Torng) Los Angeles, USA
  - **Project: Algorithm-Driven On-Chip Integration for High Density and Low Cost** [P.2]
    - Developed an algorithmic solution to the active chip-site packing problem, eliminating reliance on ad-hoc design heuristics.
    - Designed an architecture and corresponding VLSI implementation that interconnects densely packed chip sites within minimal residual layout area.
  - **Project: A Vertically Integrated Framework for Templatized Chip Design** [P.1]
    - Established a formal verification framework to ensure that hardware behavior conforms to software-level specifications and interface contracts.
    - Evaluated on-chip network architectures for multi-IP integration and explored layout optimization strategies for software-defined chip systems.
- **Computer Architecture Laboratory** *Jan 2021-Feb 2023*
  Graduate Researcher (Advised by Prof. Seung Eun Lee) Seoul, South Korea
  - **Project: Design of a Stochastic Computing Unit for Embedded AI Processors Based on Cortex-M0**
    - Implemented an area-efficient stochastic computing unit for Sobel image edge detection, achieving 92.4% computational accuracy.
  - **Project: Embedded AI Module Based on Neuromorphic Computing** [C.1]
    - Proposed a parallel recognition architecture that achieves a 2.3% accuracy improvement over a standalone AI processor and provides robustness through federated learning with non-IID datasets.
- **Intelligent Control Laboratory** *Jan 2014-Feb 2017*
  Undergraduate Researcher (Advised by Prof. Min-Kee Park) Seoul, South Korea
  - **Project: Development of a Real-Time Sensor Fusion Computing System for Autonomous Vehicles**
    - Participated in the Freescale (NXP) Cup Line Tracer Smart Car Competition.

Skills

- **ASIC Tape-Out Experience** Intel 16nm, Samsung 28nm, TSMC 180nm (Ongoing: TSMC 28nm, 40nm)
- **Programming** Verilog, SystemVerilog, VHDL, Python, C/C++
- **Tools** Synopsys Design Compiler, IC Compiler / IC Compiler II, PrimeTime, Formality, StarRC, VCS, Verdi, Cadence Innovus, Genus, Intel Quartus Prime, ModelSim, PSpice, Altium Designer, MATLAB, LabVIEW

Honors and Awards

- **Scholarship: Ph.D. Fellowship** *Feb 2023*
  University of Southern California
- **The 23rd Semiconductor Design Competition of South Korea** *Corporate (LX Semicon) Special Award*
  Korea Semiconductor Industry Association Oct 2022
  - Topic: AI Processor employing Stochastic Computing for Embedded Systems

SELECTED PUBLICATIONS (FULL LIST ON GOOGLE SCHOLAR) C=CONFERENCE, J=JOURNAL, P=PREPRINT

[P.2] Jeongeun Kim, Sabrina Yarzada, Paul Chen, and Christopher Torng (2025). **"Algorithm-Driven On-Chip Integration for High Density and Low Cost"**, in *arXiv preprint arXiv:2512.10089 (2025)*

[P.1] Jeongeun Kim, and Christopher Torng (2025). **"A Vertically Integrated Framework for Templatized Chip Design"**, in *arXiv preprint arXiv:2512.10155 (2025)*

[C.1] Jeongeun Kim, Youngwoo Jeong, Suyeon Jang, and Seung Eun Lee. **"An Architecture for Resilient Federated Learning through Parallel Recognition"**, in *The 31st International Conference on Parallel Architectures and Compilation Techniques (PACT 2022), Poster Paper*

[J.2] Jeongeun Kim, Won Sik Jeong, Youngwoo Jeong, and Seung Eun Lee. **"Parallel Stochastic Computing Architecture for Computationally Intensive Applications"**. *Electronics*, Vol. 12, no. 7, Apr. 2023.

[J.1] Kwonneung Cho, Jeongeun Kim, Do Young Choi, Young Hyun Yoon, Jung Hwan Oh and Seung Eun Lee. (2022). **"An FPGA-Based ECU for Remote Reconfiguration in Automotive Systems"**. *Micromachines*, Vol. 12, No. 1309, Oct. 2021.

PROFESSIONAL EXPERIENCE

- **Korea Electronics Technology Institute (KETI) [🌐]** *Jan 2023 -Jul 2023*
  Researcher Bundang, South Korea
  ◦ Experience in embedded operating system development and containerization using Docker.
  ◦ Poster presentation at JCCI 2023
  Title: Docker container–based system architecture for interfaces between heterogeneous devices.

- **SEMES Co., Ltd. [🌐]** *Jan 2017 -Jan 2021*
  Department of Next Generation Controller Development, Hardware Design Engineer Hwaseung, South Korea
  ◦ Designed next-generation controller for Overhead Hoist Transport (OHT) systems.
  ◦ Developed power, motor, and I/O control circuits, including PCB layout and design.
  ◦ Implemented firmware for DC and stepper motor control, I/O management, and servo motor operation.

MAJOR COURSEWORK

EE560 Digital System Design: Implemented cache, FIFO, Tomasulo units (FRL, BPB, SAB, ROB, Dispatch), AXI, PCIe, GPGPU modules in VHDL.

EE577A VLSI System Design I: Designed 512-bit SRAM (sense amp, precharge, decoders) in Virtuoso.

EE577B VLSI System Design II: Built and verified a 4×4 mesh NoC with CPU nodes in SystemVerilog.

EE599 Complex Digital ASIC System Design: Integrated top-level ASIC design and on-chip clock generator using Intel 16nm technology.

EE658 Reliable Digital Systems: Developed logic & fault simulator and ATPG (D-algorithm, PODEM) in C++.

CSCI570 Analysis of Algorithms: Implemented memory-efficient sequence alignment algorithms in Python.

TEACHING AND MENTORING EXPERIENCE

- **EE599 Complex Digital ASIC System Design** *Fall 2024*
  Teaching Assistant, University of Southern California
- **Center for Undergraduate Research in Viterbi Engineering (CURVE) Mentoring** *Fall 2024 – Present*
  PhD Mentor, University of Southern California
  ◦ Project: ECG-Based Tachycardia Detection Using Arduino (Student Name: Kyna Rochlani, Andrea Sibrian)
  - Participated in the CURVE & GCSP Research Symposium, presenting a poster.
- **SoC Design Methodology** *Fall 2021*
  Teaching Assistant, Seoul National University of Science and Technology
- **Computer Architecture** *Fall 2021*
  Teaching Assistant, Seoul National University of Science and Technology
- **Digital System Design** *Spring 2021*
  Teaching Assistant, Seoul National University of Science and Technology

PATENTS

[P.2] Seung Eun Lee, Jeongeun Kim, Youngwoo Jeong. (2023). **Federated Learning Method and System Using Shared Learning Data**. Patent No. 10-2795643. Registration Date: Apr 2025, US20250124342

[P.1] Seung Eun Lee, Jeongeun Kim, Youngwoo Jeong. (2023). **Method and System for Determining Final Result Using Federated Learning**. Patent No. 10-2795656. Registration Date: Apr 2025, US20250124343