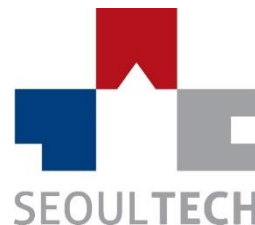


# **Reconfigurable Stochastic Computing Architecture for Computationally Intensive Applications**

**Jeongeun Kim, Yue Ri Jeong, Kwonneung Cho,  
Won Sik Jeong, and Seung Eun Lee**

*Seoul National University of Science and Technology  
Department of Electronic Engineering*

*Seoul, Republic of Korea*

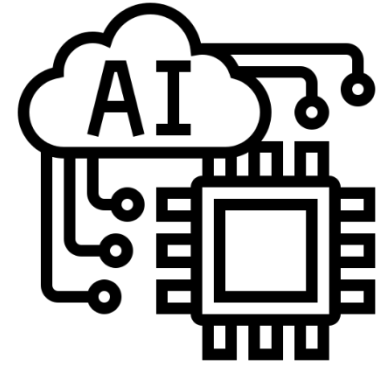
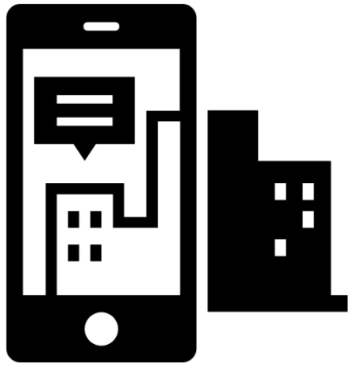


# Outline

- **Introduction**
- **Proposed Architecture**
- **Experimental Results**
- **Conclusion**

# Introduction - Motivation

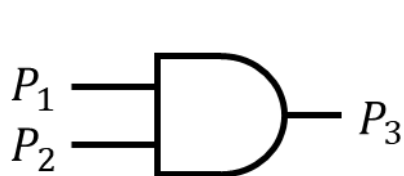
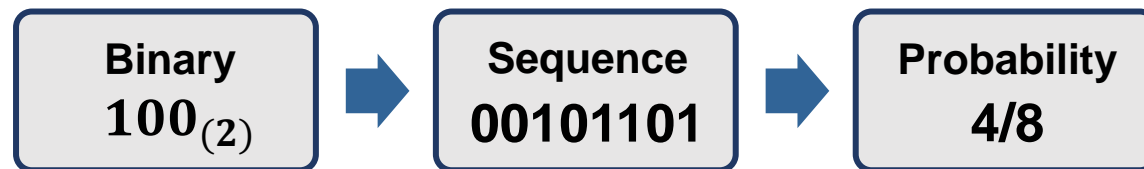
- **Emerging Computationally intensive applications**  
**Image recognition, Autonomous driving, AI Assistant ..**



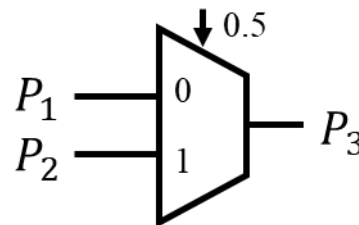
- ✓ **Efficient utilization of circuit area**
- ✓ **Lightweight logics with suitable accuracy**

# Introduction - Preliminaries

- **Stochastic Computing (SC)**
  - The SC adapts **probability value [0,1]**
  - The value is approximated to **ratio of '1's** in random bitstreams



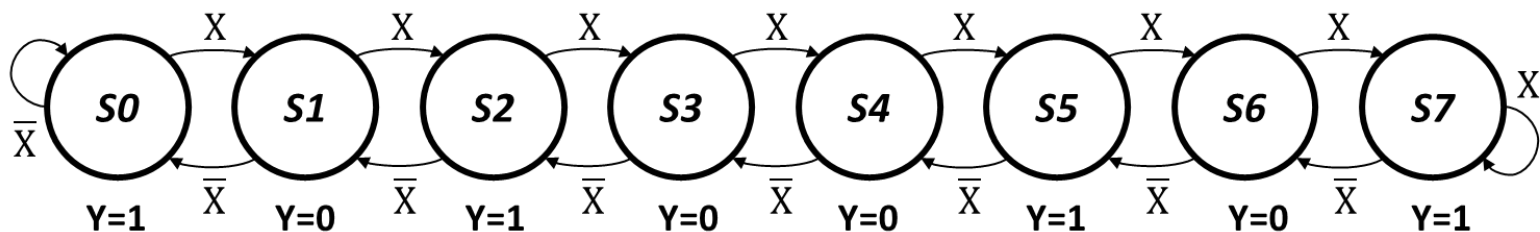
[Unipolar Multiplier]



[Adder]



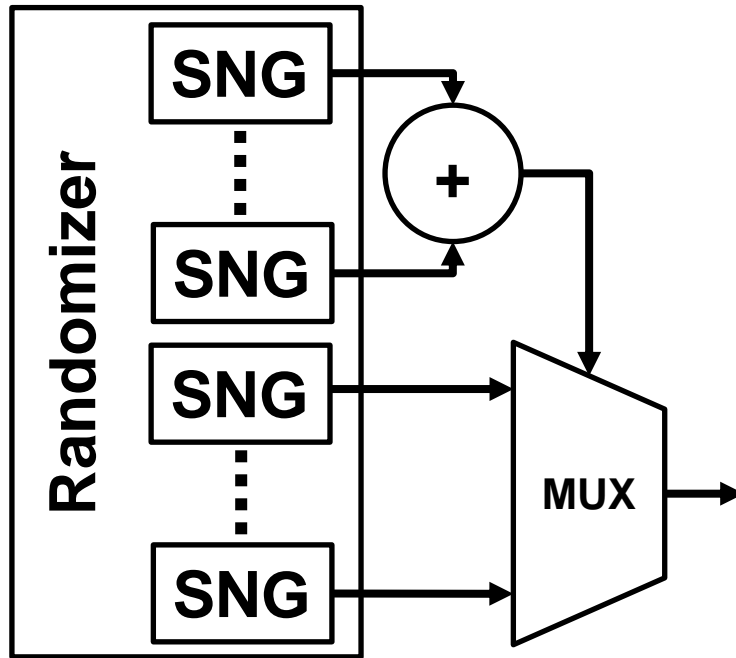
[Bipolar Multiplier]



[Absolute Function]

# Introduction – Related works

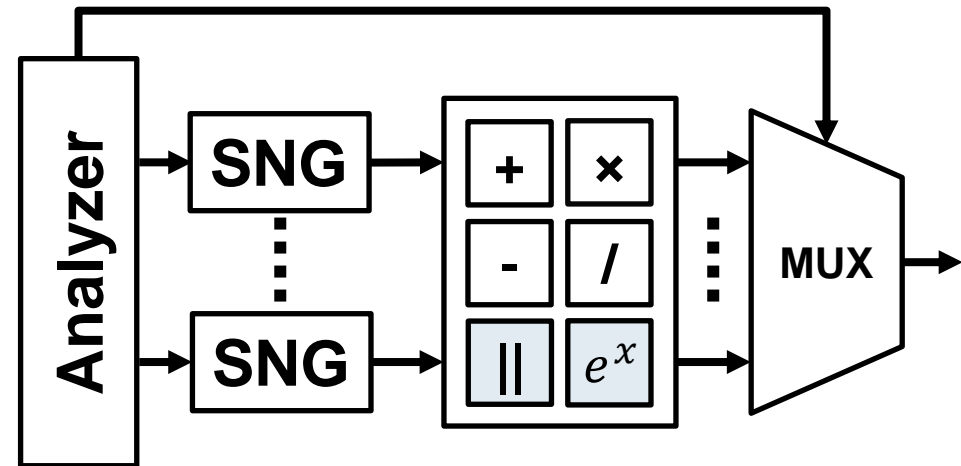
- Reconfigurable SC Unit**



**[Related works]**

**Bernstein polynomial**

$$y = z_0 + z_1x + z_2x^2 + z_3x^3$$



**[Our work]**

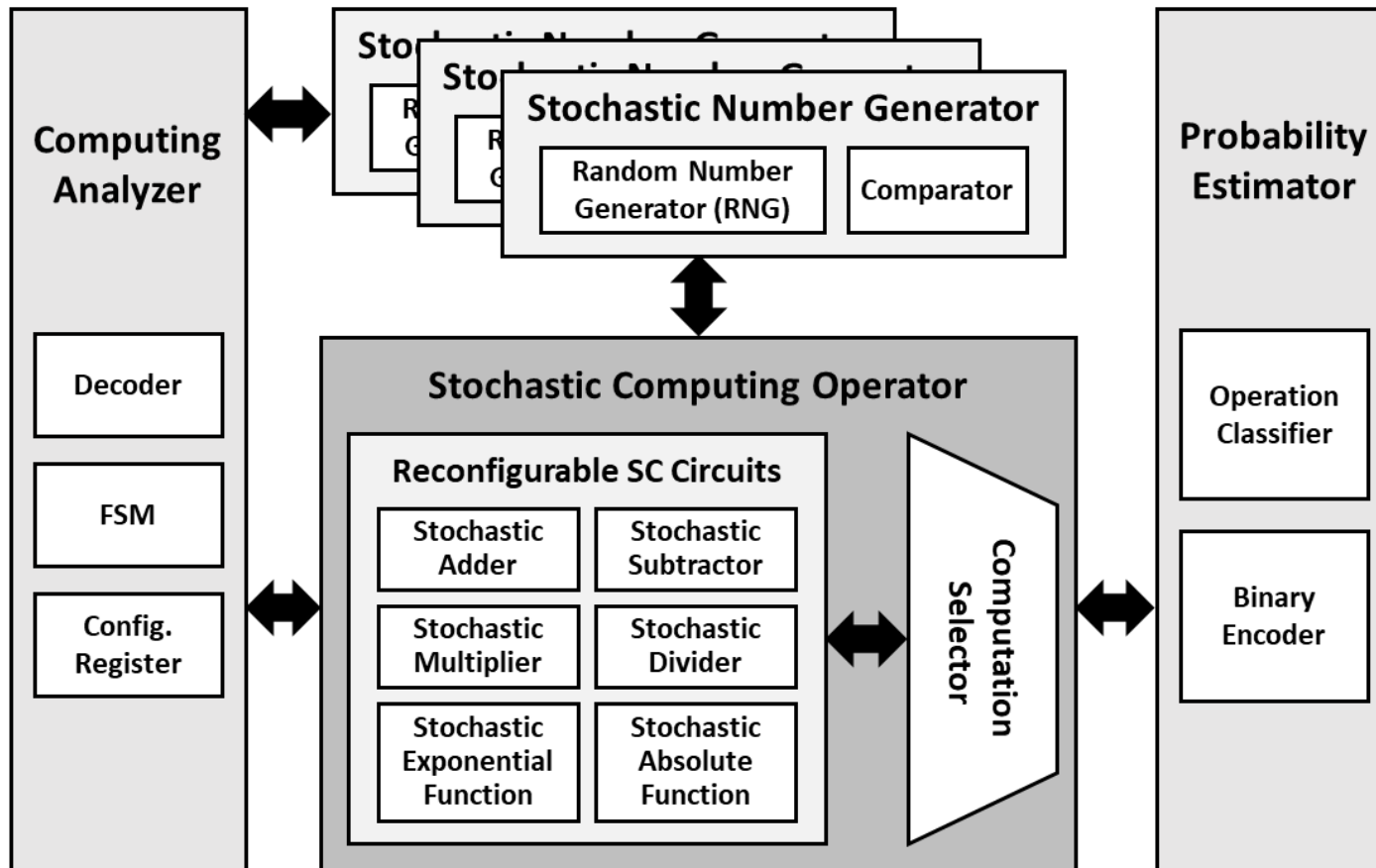
**Arithmetic operation +  
Mathematical functions**

$$y = |z_0 - z_1x| + e^x + \frac{z_2}{z_3}$$

[1] H. El-Derhalli et.al, "OSCAR: An Optical Stochastic Computing Accelerator for Polynomial Functions," DATE, 2020, pp. 1450-1455.

[2] W. Qian et.al, "An Architecture for Fault-Tolerant Computation with Stochastic Logic," in IEEE Transactions on Computers, vol. 60, no. 1, pp. 93-105.

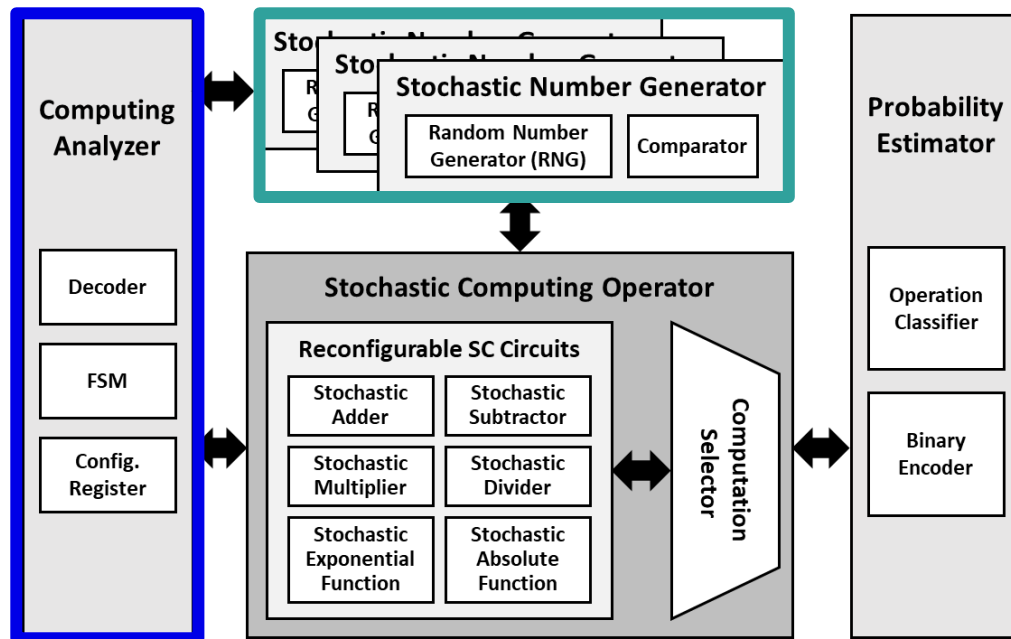
# Proposed Architecture



[The proposed architecture of reconfigurable SC unit]

# Proposed Architecture

## • Reconfigurable Stochastic Computing



### • Computing Analyzer

- Decode the input formula
- Schedule each operation

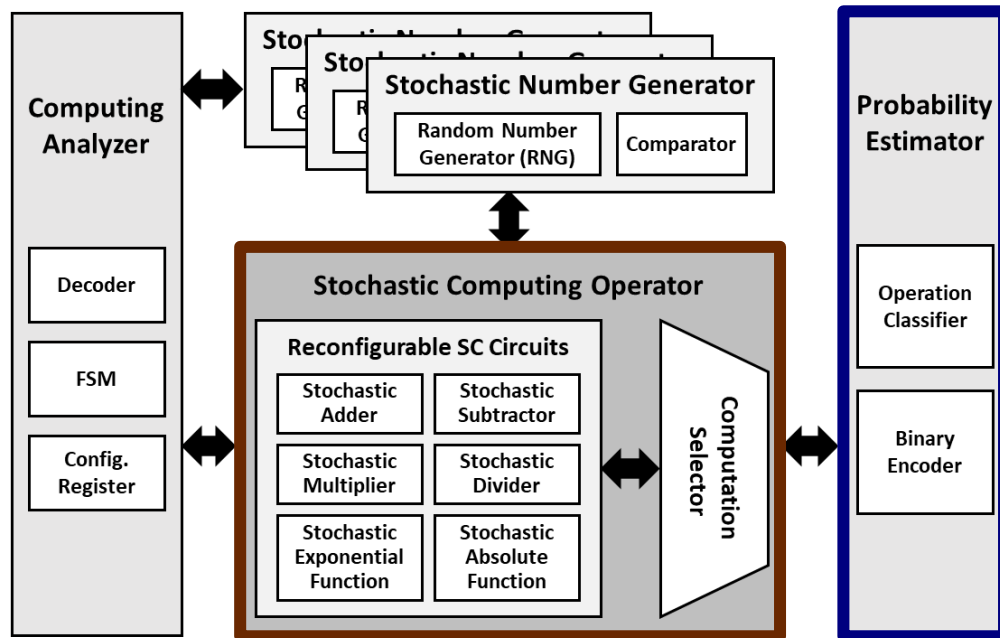
### • Parallelized SNGs

- Include 8-bit linear feedback shift registers (LFSR)
- Generate stochastic sequence

[The proposed architecture of reconfigurable SC unit]

# Proposed Architecture

## • Reconfigurable Stochastic Computing

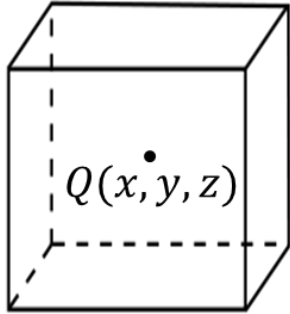


- **Stochastic Computing Operator**
  - Conduct stochastic computations
- **Probability Estimator**
  - Convert the resulting stochastic sequence to binary output

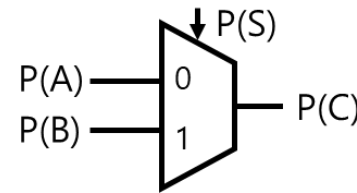
[The proposed architecture of reconfigurable SC unit]



# Experimental Results (1)

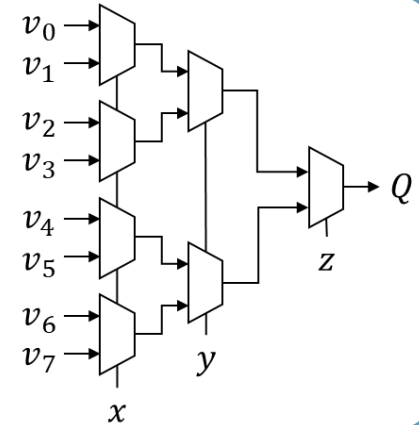


$$\begin{aligned}
 Q = & v_0(1-x)(1-y)(1-z) \\
 & + v_1(1-x)y(1-z) \\
 & + v_2(1-x)(1-y)z \\
 & + v_3(1-x)yz \\
 & + v_4x(1-y)(1-z) \\
 & + v_5xy(1-z) \\
 & + v_6x(1-y)z + v_7xy.
 \end{aligned}$$



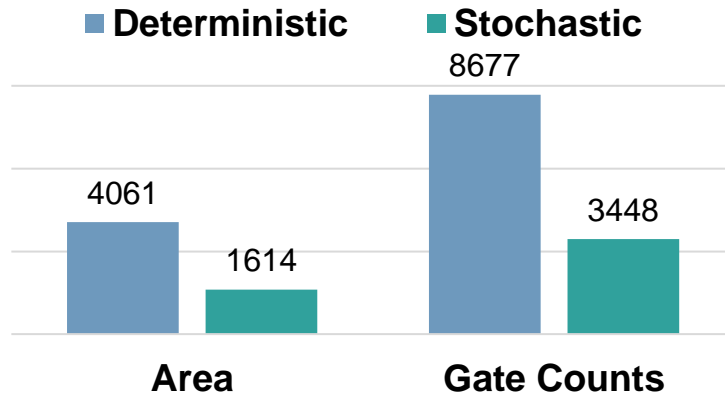
$$P(C) = (P(A) \times (1 - P(S))) + (P(B) \times P(S))$$

In case of  $P(S)=0.5$ ,  
 $P(C)=0.5(P(A)+P(B))$



[Arithmetic expression of Tri-linear interpolation [1]]

[Tri-linear interpolation operator based on SC [2,3]]



	Deterministic	Stochastic
Area	4,061 $\mu m^2$	1,614 $\mu m^2$
Gate counts	8,677	3,448

\* 8bit Operation  
\*Samsung 28nm, Design Compiler

[1] Y. Shicai et.al "An high efficient and speed algorithm of Ray Casting in volume rendering," ICCE, 2011, pp. 1027-1030.

[2] P. Li et.al, "Logical Computation on Stochastic Bit Streams with Linear Finite-State Machines," in IEEE Transactions on Computers, vol. 63, no. 6, pp.1474-1486, June 2014.

[3] Stochastic computing, Technology Trend column from IDEC

# Experimental Results (2)

## • Image Processing



[Original Image]

-1	0	+1	+1	+2	+1
-2	0	+2	0	0	0
-1	0	+1	-1	-2	-1

**Gx Gy**  
[Sobel Convolution Kernels]

$$|G| = |(P_1 + 2P_2 + P_3) - (P_7 + 2P_8 + P_9)| + |(P_3 + 2P_6 + P_9) - (P_1 + 2P_4 + P_7)|$$

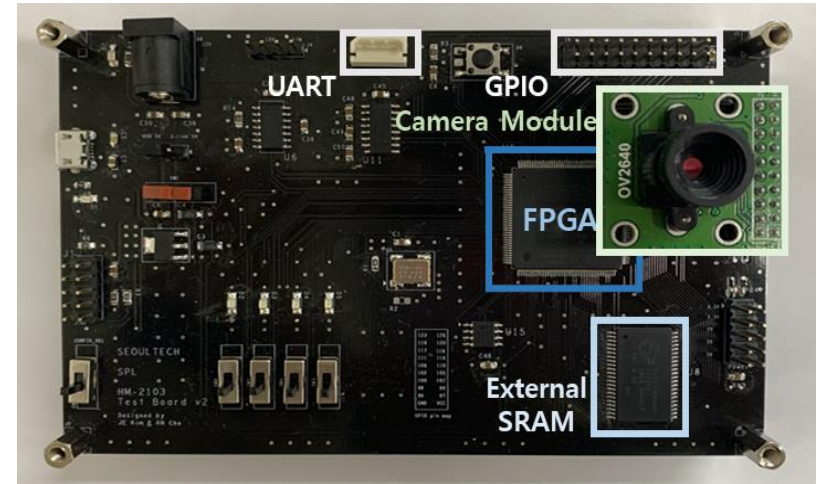
[Approximate Gradient Magnitude]



[Deterministic Implementation]



[Stochastic Implementation,  
Accuracy(avg): 92.4%]



[Verification Prototype]

	Test Board Specifications
<b>FPGA</b>	Altera MAX10 10M50SCE144C8G
<b>Input Voltage</b>	5V / 12V
<b>Operation Freq.</b>	50MHz
<b>Memory</b>	off-chip 512KB SRAM
<b>Camera Module</b>	OV2640 CMOS
<b>Peripheral</b>	Camera I/F, Serial I/F, GPIO

# Conclusion

- **Reconfigurable SC architecture**  
: targeting computationally intensive applications
- **39.7% of area reduction with lightweight circuits**
- **92.4% of accuracy on Image processing**

# Thank You



**Jeongeun Kim**



**Yue Ri Jeong**



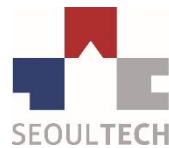
**Kwonneung Cho**



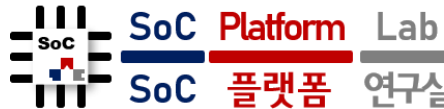
**Won Sik Jeong**



**Seung Eun Lee**



SEOUL NATIONAL UNIVERSITY OF  
SCIENCE & TECHNOLOGY



<https://soc.seoultech.ac.kr>