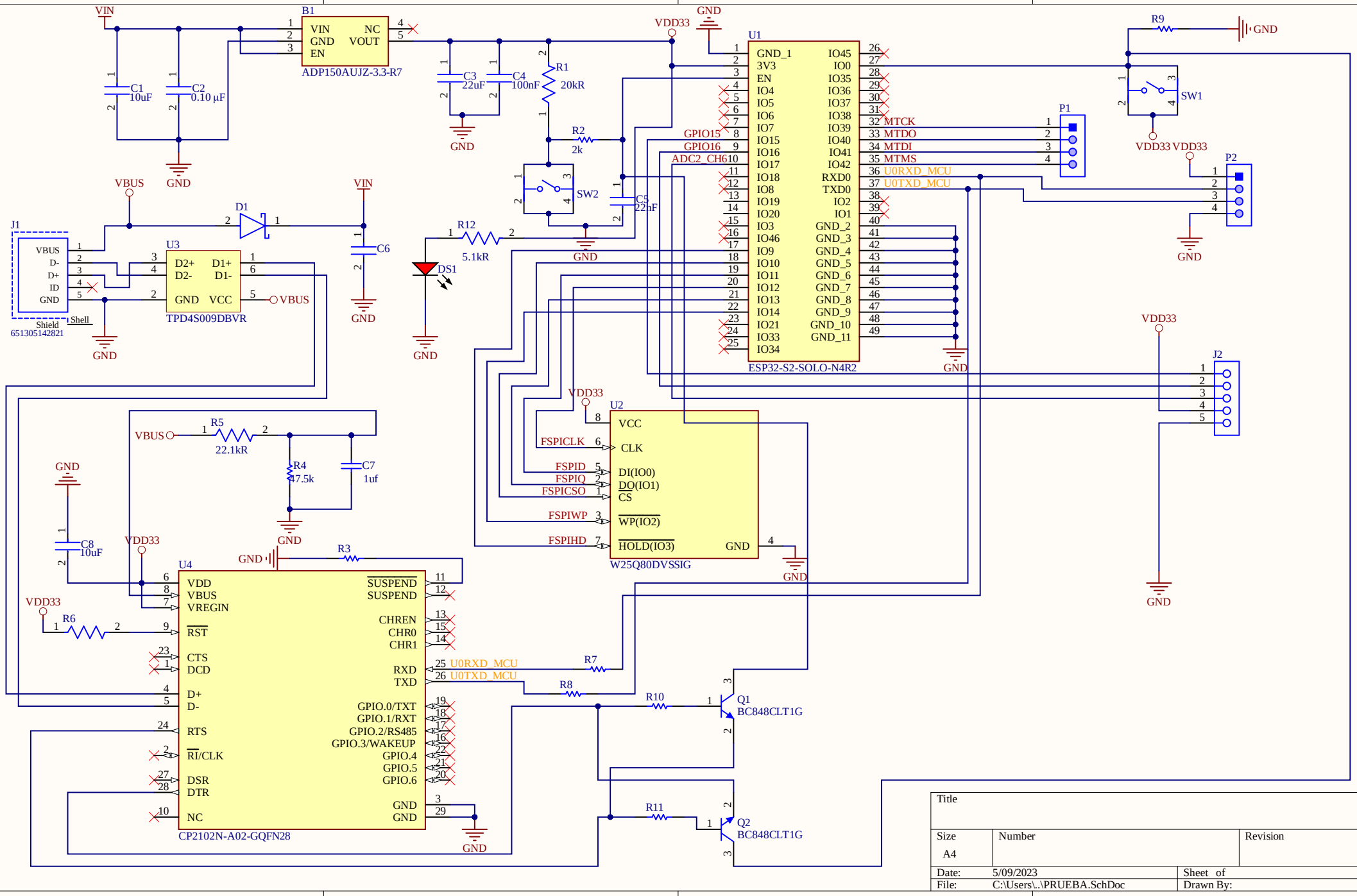

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Date: 5/09/2023		Sheet of
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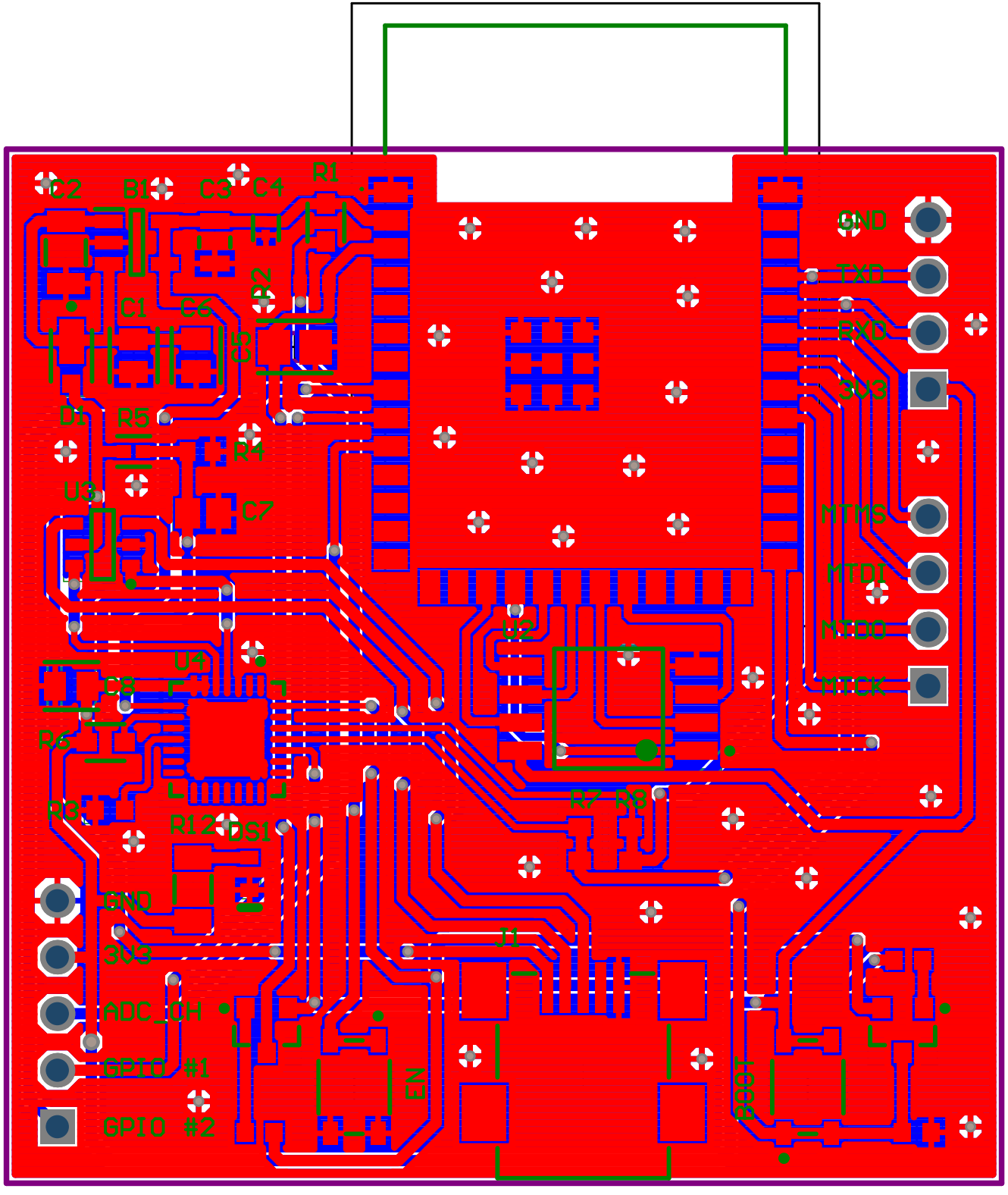
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C4
R1
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C6
C5
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R5
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C7
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R6
R3
R12
DS1
GND
3V3
ADC_CH
GPIO #1
GPIO #2
U2
R7
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RXD
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MTMS
MTDI
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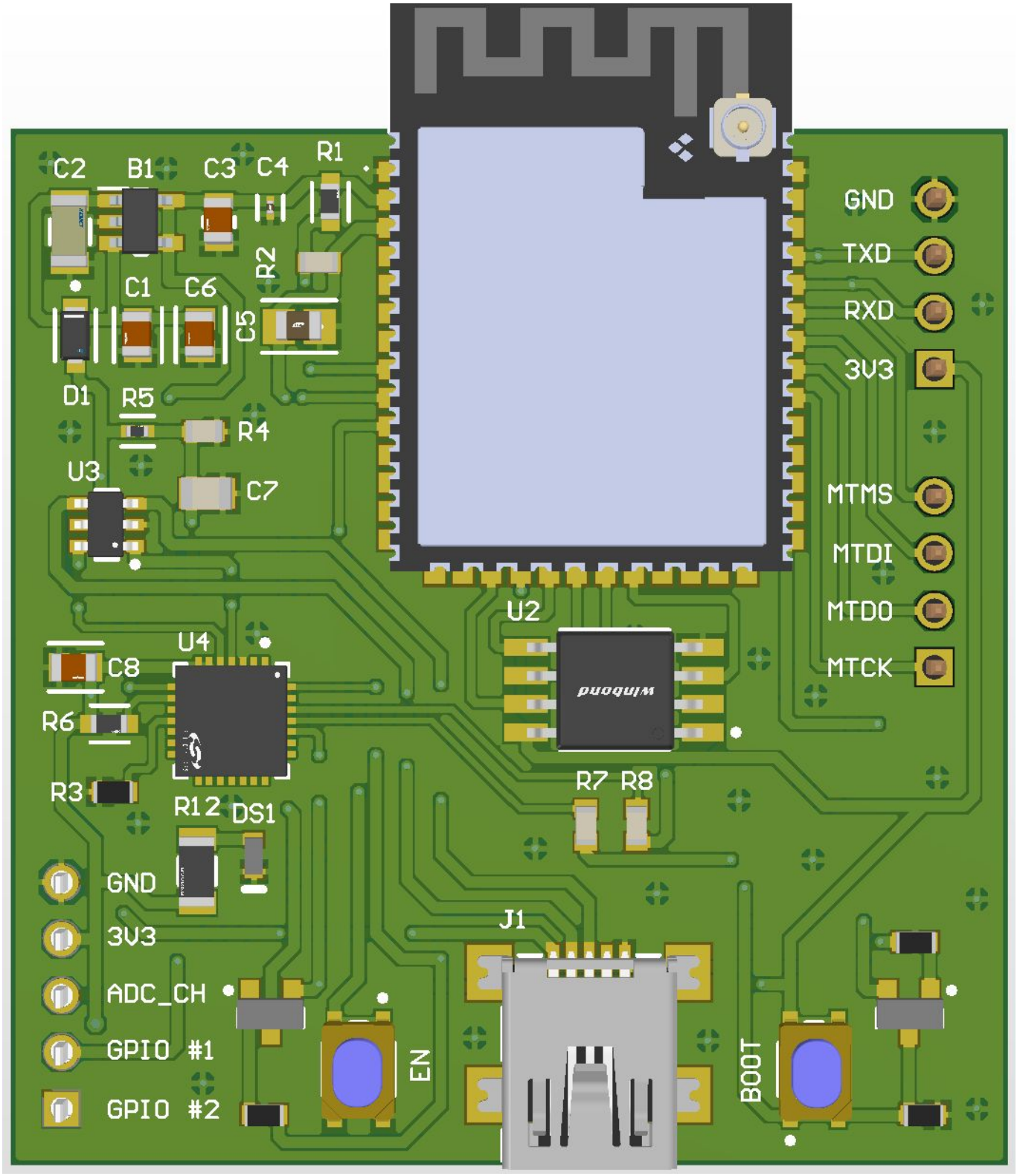
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C8
R6
R3
R12
DS1
R7
R8
J1
EN
BOOT
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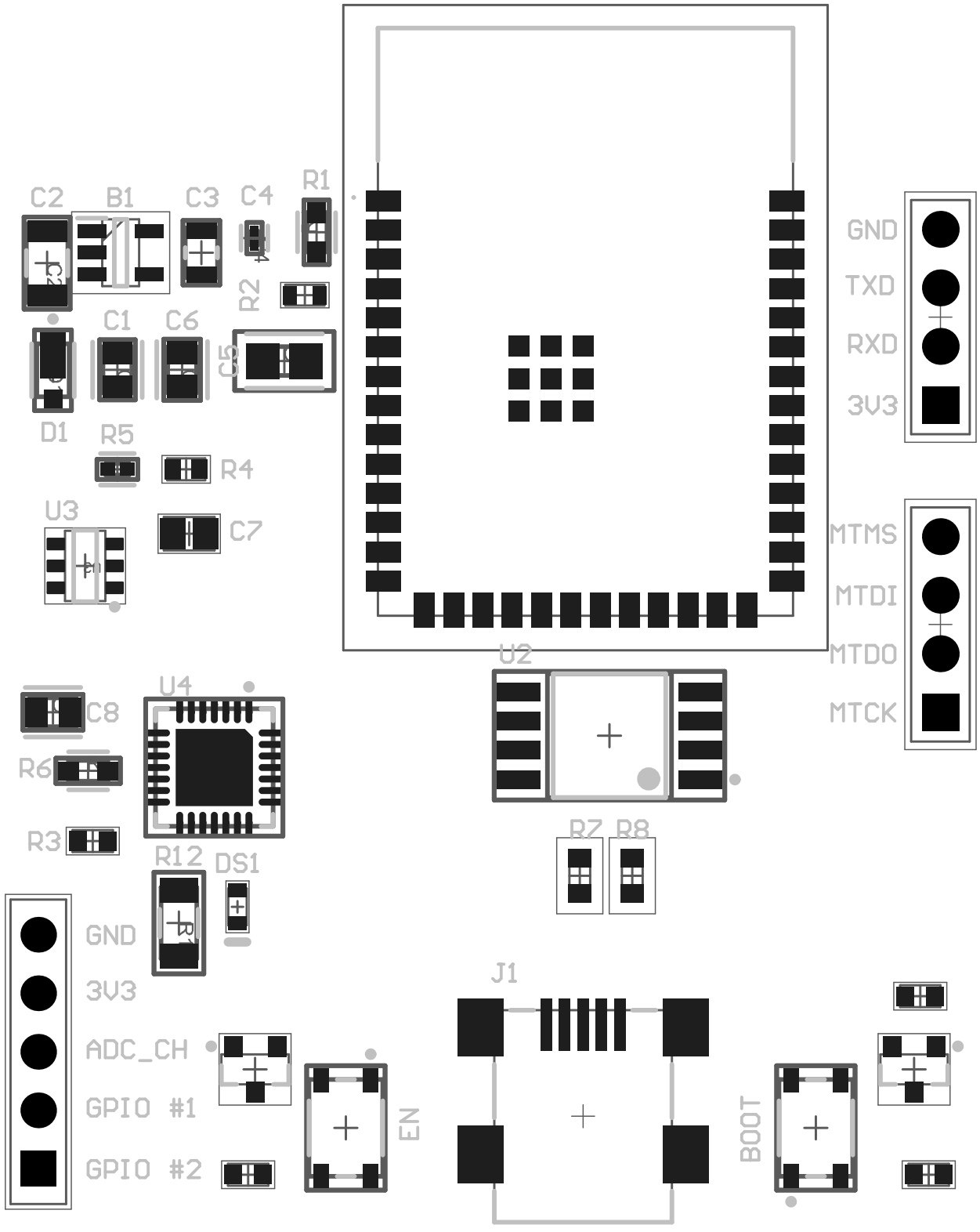
GND
3V3
ADC_CH
GPIO #1
GPIO #2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MTMS
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MTDO
MTCK
U2
U4
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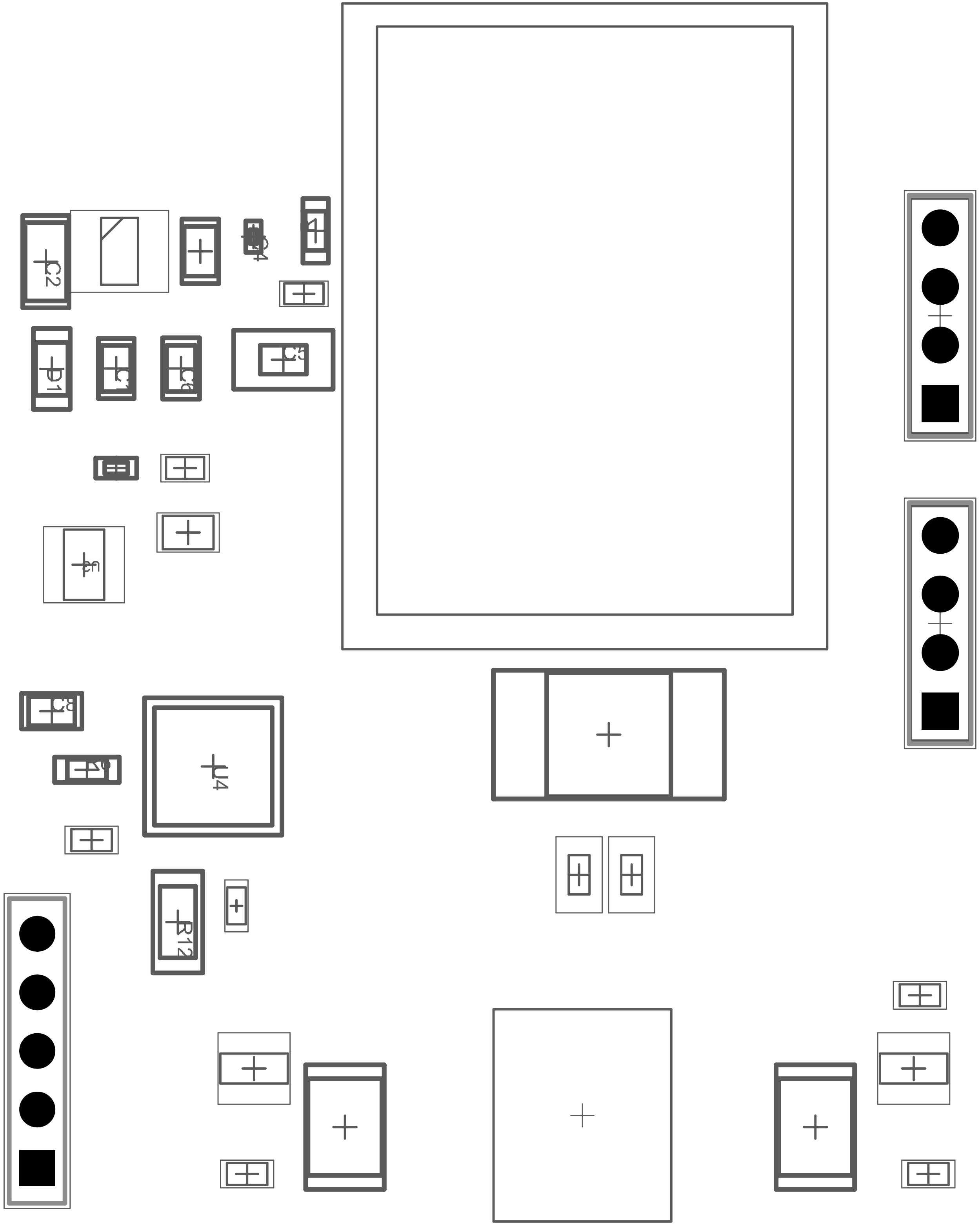
EN
J1
BOOT


C2
C5
U4
R12

Design Rules Verification Report

Filename : C:\Users\57310\Desktop\Altium Designer Proyects\PRUEBA_ESP32-S2_8232\

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=4.5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=30mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air	0
Hole Size Constraint (Min=1mil) (Max=150mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=2.953mil) (All),(All)	0
Silk To Solder Mask (Clearance=2.953mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Room PRUEBA (Bounding Region = (1115mil, 1310mil, 2870mil, 3405mil)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0