

Digital Clock - JEHHEJ



JEHHEJ

Yiqing Huang / Ruyue Hong

Summary:

This may be the best digital clock in the whole universe.

Our GitHub Homepage: <https://github.com/JEHHEJ/Digital-Clock>

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1 INTRODUCTION

The basic task of the project of LED Digital Clock is to use DC power to finally make a clock. And we add two additional functions—alarm and day display—into our circuit. The highlight among all these functions is that we use logic gate to build a unique encoder ourself for 7 LED indicating days from Monday to Sunday.

2 FLOW CHART



3 CIRCUIT PRINCIPLE

What we have learnt from Electric Circuits Lab is the usage of 555 Timer and some simple logic calculation. However, we are not familiar with Flip- Flop and Seven Segment Display and its encoder—74LS48. Through the help of our TA especially his sending a material of the principle of Flip-Flop and some materials on the Internet, we simulate and build our circuit successfully. Here are some principle of the basic components applied into our circuit.

3.1 JK FLIP-FLOP

Figure 7–23 shows the basic internal logic for a positive edge-triggered J-K flip-flop. The Q output is connected back to the input of gate G_2 , and the \bar{Q} output is connected back to the input of gate G_1 . The two control inputs are labeled J and K in honor of Jack Kilby, who invented the integrated circuit. A J-K flip-flop can also be of the negative edge-triggered type, in which case the clock input is inverted.

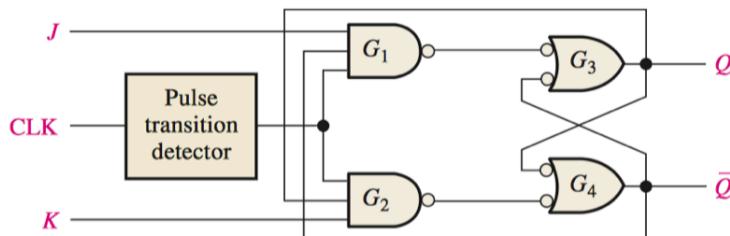


FIGURE 7–23 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

Let's assume that the flip-flop in Figure 7–24 is RESET and that the J input is HIGH and the K input is LOW rather than as shown. When a clock pulse occurs, a leading-edge spike indicated by ① is passed through gate G_1 because \bar{Q} is HIGH and J is HIGH. This will cause the latch portion of the flip-flop to change to the SET state. The flip-flop is now SET.

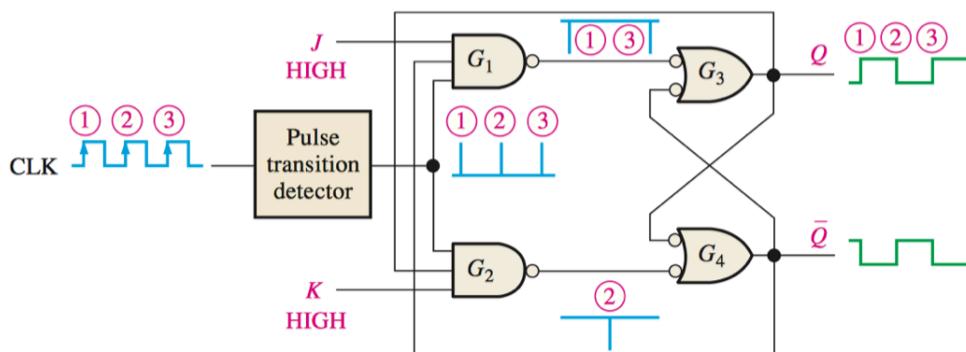


FIGURE 7–24 Transitions illustrating flip-flop operation.

Source: Digital Fundamental Chapter Flip-Flops



3.2 555 TIMER

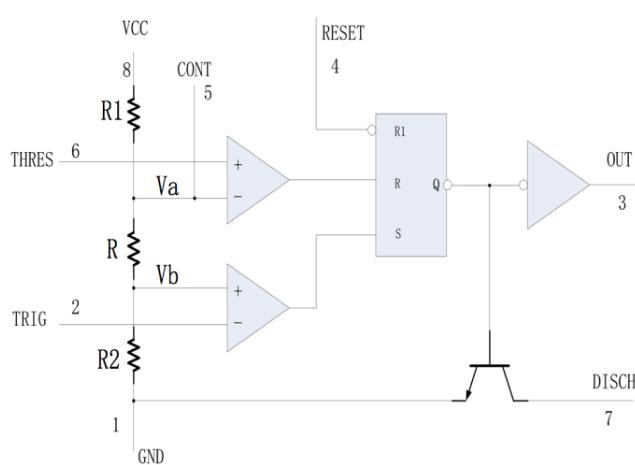


Figure 1

Fig. 1 shows a simplified internal circuit diagram of the 555 timer. Fig. 2 shows its pin diagram.

Source: UC Berkeley, EECS100 Lab, Fall 2009.

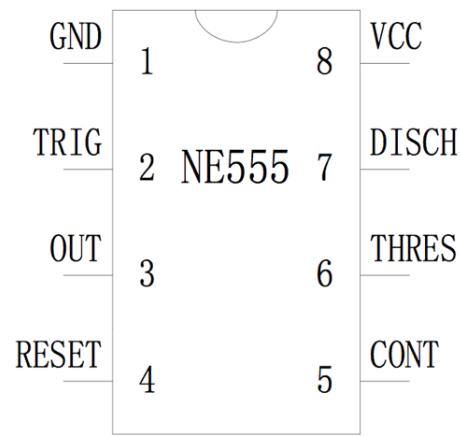


Figure 2

3.3 PMOS

When the voltage of input A is high, the PMOS transistor is in an OFF (high resistance) state so it would limit the current flowing from the positive supply to the output, while the NMOS transistor is in an ON (low resistance) state, allowing the output from drain to ground. Because the resistance between Q and ground is low, the voltage drop due to a current drawn into Q placing Q above ground is small. This low drop results in the output registering a low voltage.

Source: <https://en.wikipedia.org/wiki/CMOS>

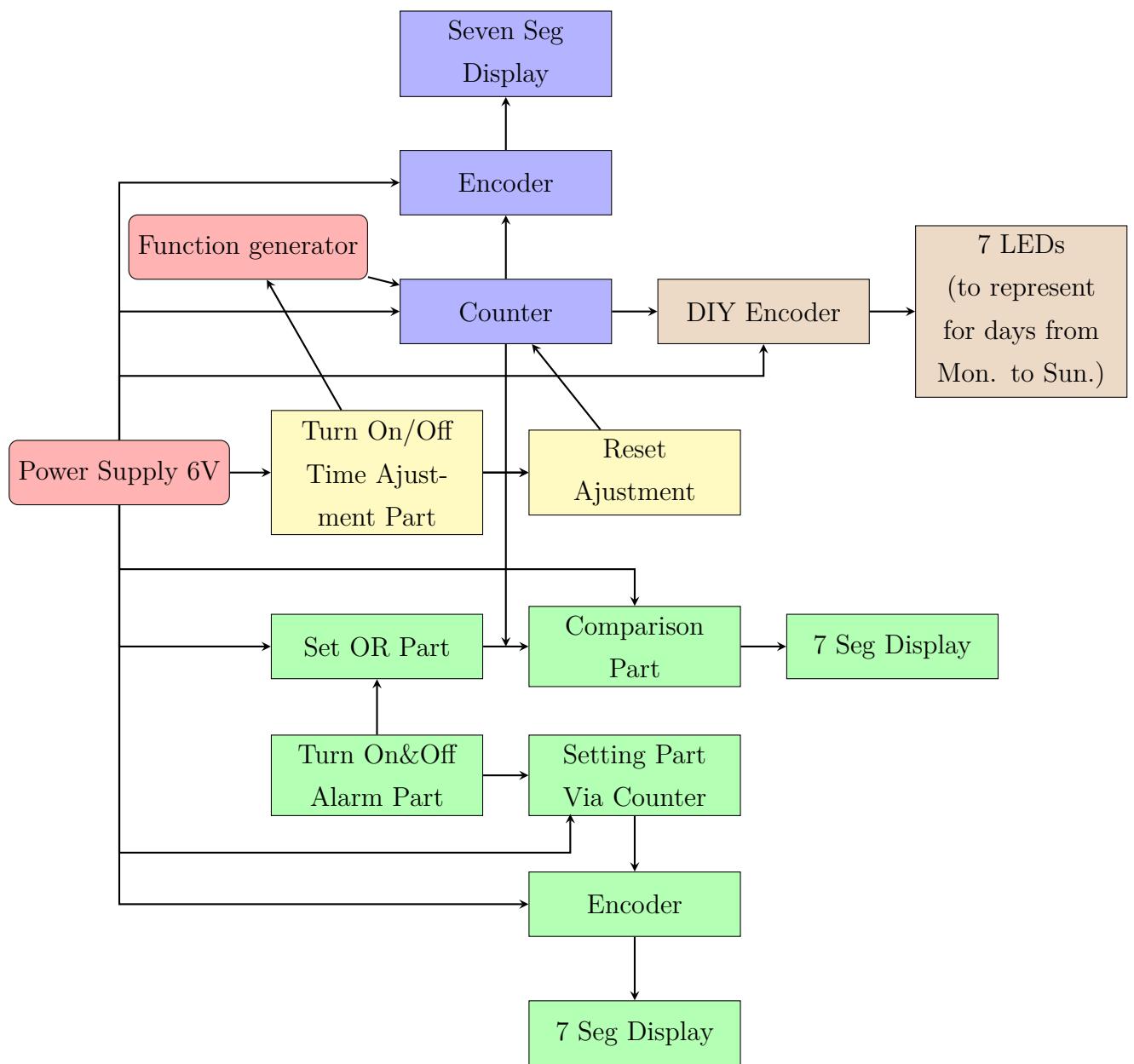
4 COMPONENTS

TABLE 1: COMPONENT LIST.

Name	Type	Quantity
Battery Box		1
Timer555		1
Capactior	$0.01\mu F$	1
	$0.1\mu F$	1
Resistor	$1k\Omega$	1
	$2k\Omega$	1
	100Ω	3
JK Flip Flop	74HC112	27
Seven Seg Display		12
Seven Seg Encoder	74LS48D	12
Switch		10
NOT Gate	74AS04M	20
NAND Gate	7400N	20
XOR Gate	7486N	10
OR Gate	7432N	5
Piezo Buzzer		1
CMOS	IRF510	4
LED	White	10



5 BLOCK SCHEMATIC



FRAME 1: COLOR BLOCK

Red Block: Input

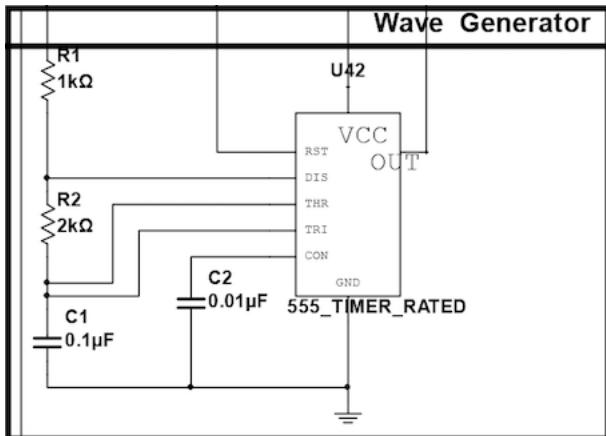
Purple Block: Basic Digital Clock

Yellow Block: Time Adjust Part

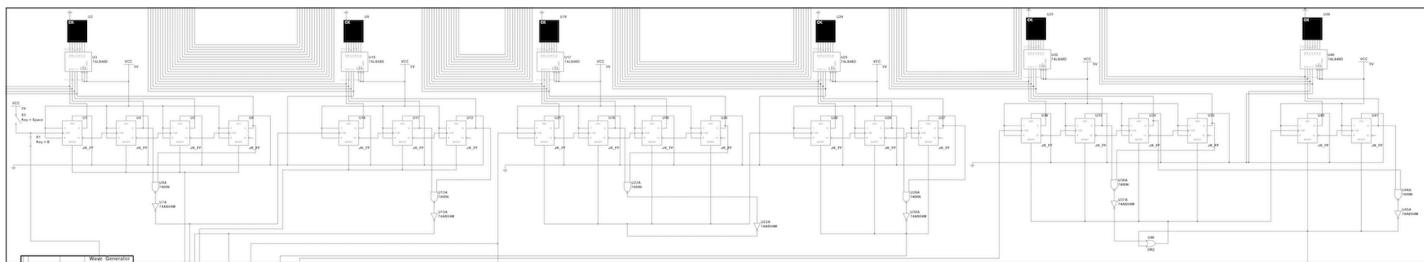
Brown Block: Show-Day Part

Green Block: Alarm Part

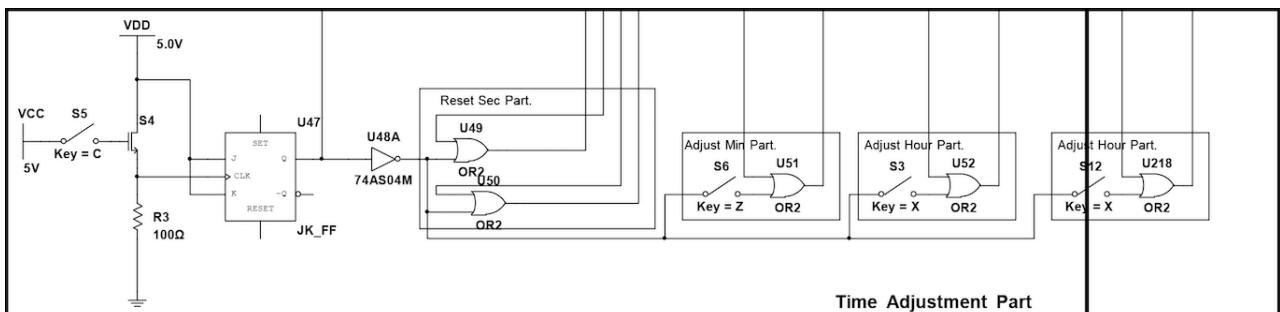
5.1 INPUT



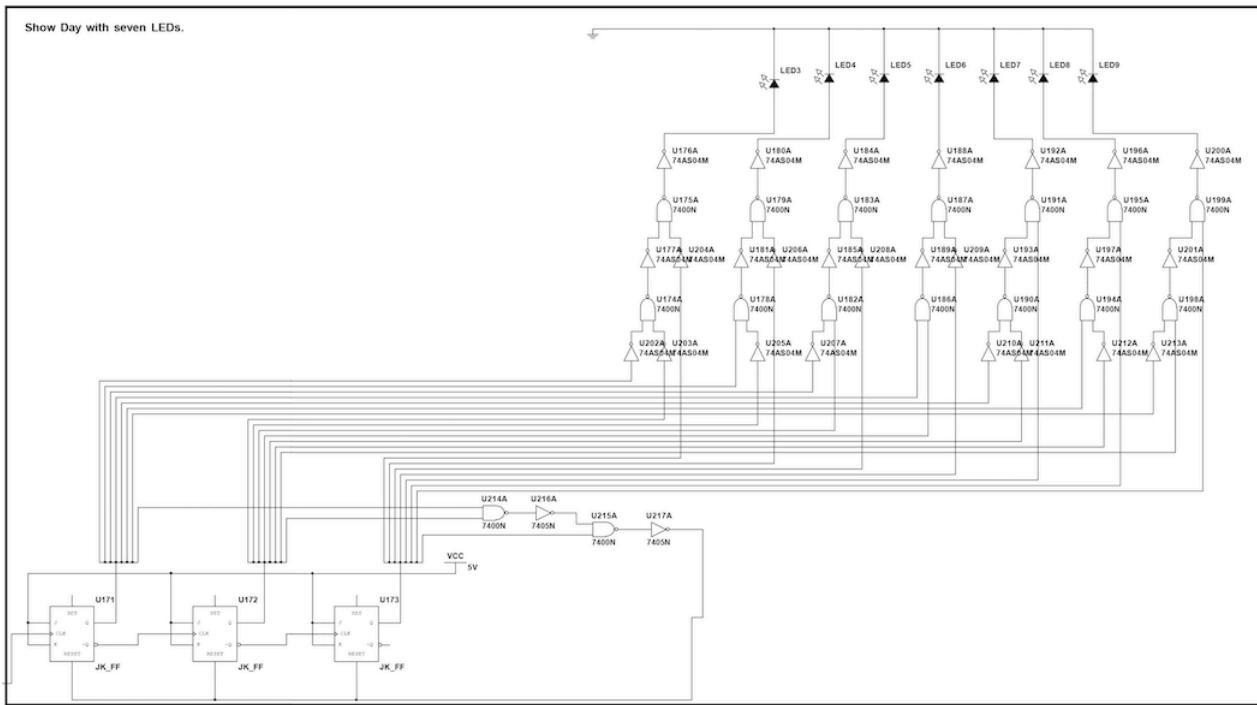
5.2 BASIC DIGITAL CLOCK



5.3 TIME ADJUST PART



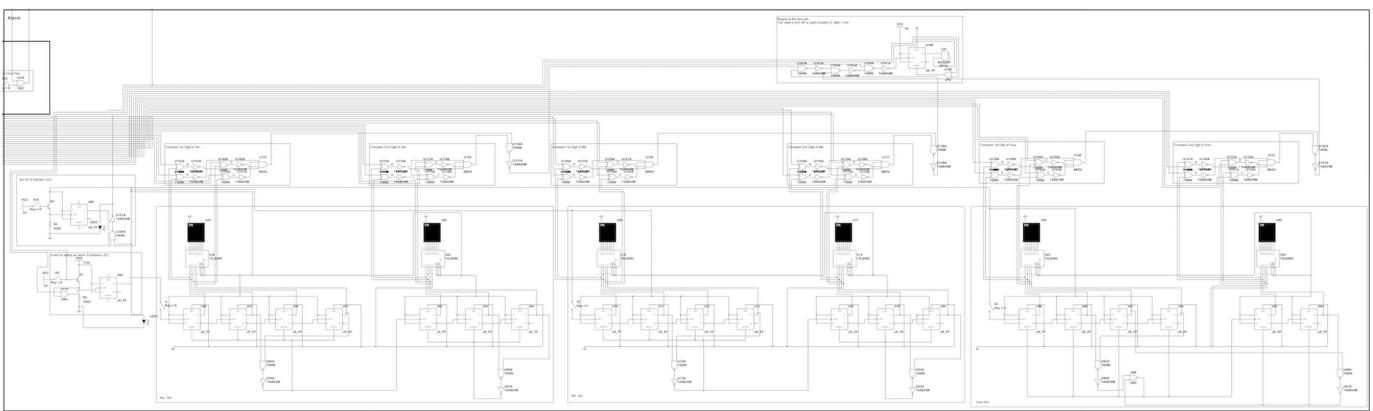
5.4 SHOW-DAY PART



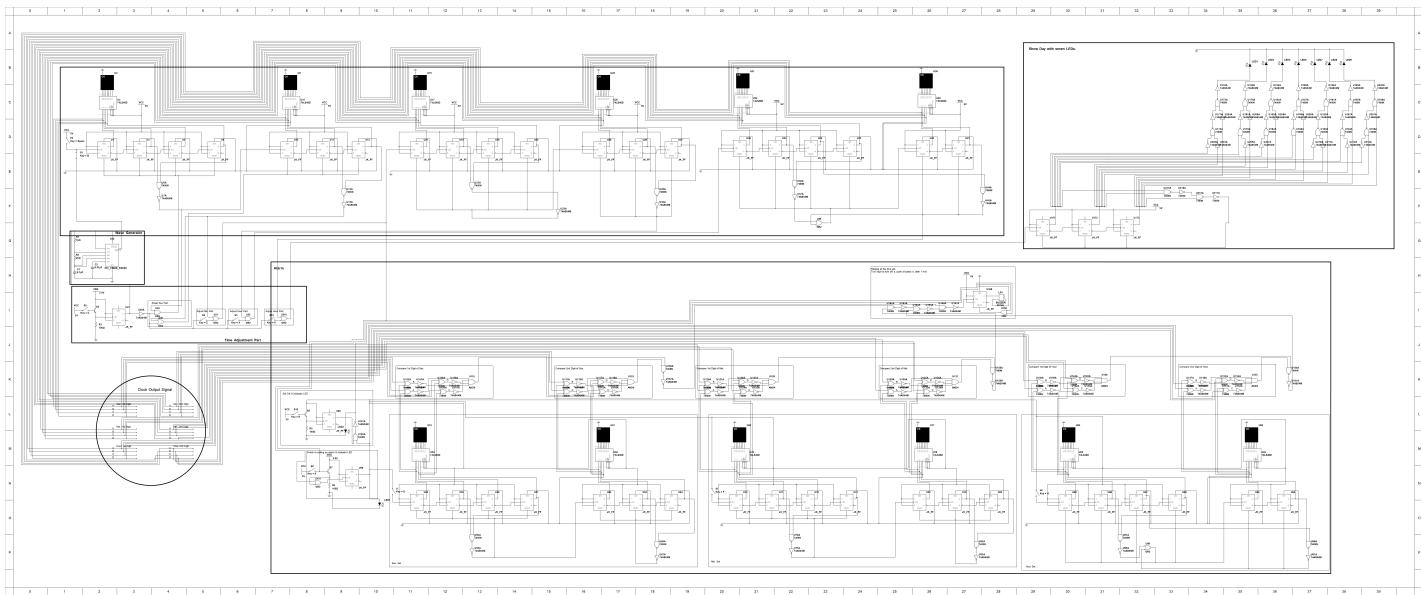
FRAME 2: TIPS

Using 7 Led Lights to indicate From Mon. to Sun.

5.5 ALARM PART

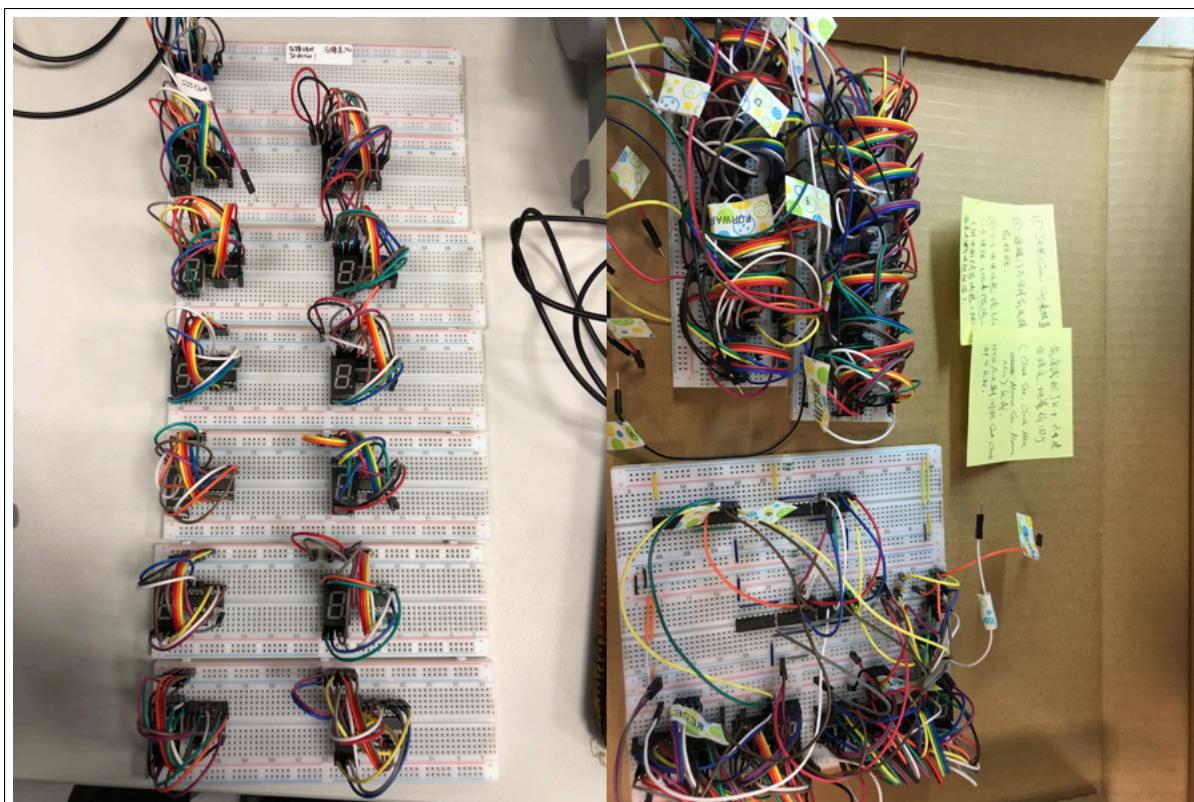


6 SCHEMATIC DIAGRAM



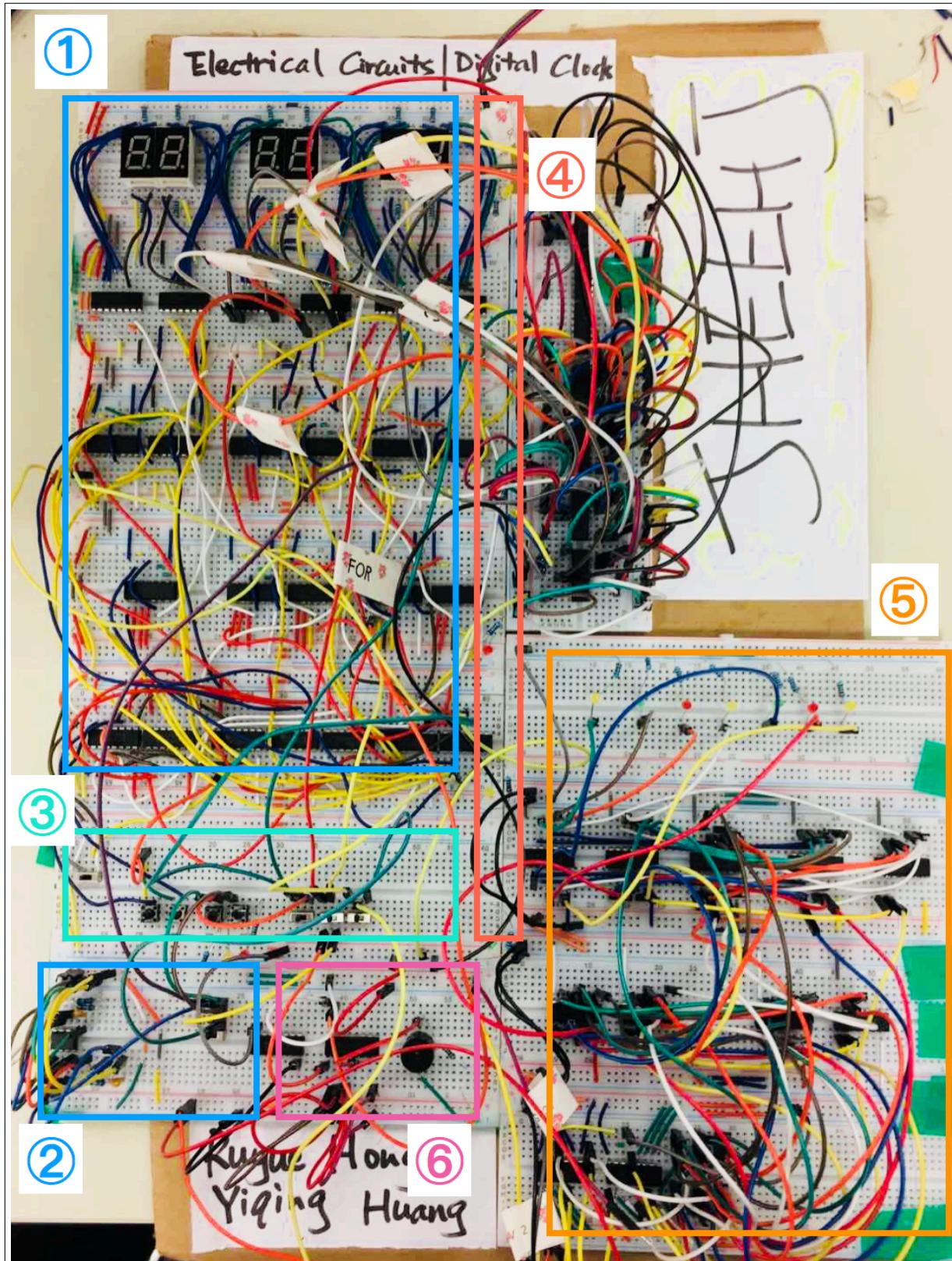
7 ACHIEVEMENT

Lapping circuit was not so successful to be honest. We have achieved most of our functions last Saturday, but because we bound the maximum current inappropriately, the first model was destroyed.



It taught us a lesson that making the circuit readable and using some indicator to suggest us when something goes wrong immediately.

Here is our final achievements.



1. Clock: We use Flip-Flop (74LS112) to count square waves generated from 555 Timer. And some logic gates (NAND—74LS00, NOT—74LS04, OR—74LS32) are applied to carry bit. Seven-Segment Display and its matched encoder (74LS48) are the indicator to show the time (the result).
2. Square Wave: We use 555 timer and some resistors and capacitors to generate square waves.
3. Time Adjustment Part: When turning on the set button, the two numbers which show the second of the clock will be reset to zero. At the beginning, we supposed to use PMOS to generate square waves on our own to adjust time, but failed. So we changed our mind and use the square waves generated from 555 timer part to adjust minute, hour and day part of the clock.
4. Error Indicators: We set a LED on every bread board and they will show us which part goes wrong as soon as an error occurred by turning off or twinkling. It looks very simple, but it is actually convenient and efficient. It do have helped us find a destroyed Flip-flop and several careless mistakes in connecting circuits.
5. Days Indicator: We use 7 LEDs from left to right to represent for Monday to Sunday. To achieve this goal, unlike a Seven-Segment Display which has a matched encoder, we use logic gates which cost 3 bread boards to build an encoder on our own. Of course, Flip-Flops are used to count the number.
6. Hour Alarm: When time goes from an hour to another, the beeper will beep for 10 seconds as we designed. We use a Flip-Flop to receive a signal from hour carry bit, so when it comes to a new hour, the Q of the Flip-Flop will turn from LOW to HIGH and the beeper will keep beeping. Besides, the reset port is connected to the 10-second carry bit so that when 10 seconds after now time, Q will turn from HIGH to LOW, so the beeper will stop to beep.

* 4, 5, 6 are our bonus parts.



8 PRESENTATION AND POSTER

JEHHEJ DIGITAL CLOCK

Ruyue Hong & Yiqing Huang

EE111 Electric Circuits | Final Project

INTRODUCTION

Firstly, we drew up a plan to decide how many functions we would like to achieve. And we use a flow chart to help us to think and make things clear.

```

graph LR
    A[Appearance] --> B[Show days of a week]
    B --> C[Digital Clock]
    C --> D[Show the time]
    C --> E[Reset]
    D --> F[Alarm]
    E --> F
  
```

SIMULATION

BLOCK SCHEMATIC

```

graph TD
    FG[Function generator] --> Counter[Counter]
    PS[Power Supply 6V] --> TOA[Turn On/Off Time Adjustment Part]
    PS --> SetOR[Set OR Part]
    PS --> TurnAO[Turn On/Off Alarm Part]
    TOA --> Counter
    Counter --> DIYEncoder[DIY Encoder]
    DIYEncoder --> LEDs[7 LEDs]
    LEDs --> DayText[7 Seg Display]
    DIYEncoder --> Reset[Reset Adjustment]
    Reset --> Counter
    Counter --> Comparison[Comparison Part]
    Comparison --> SegDisplay[7 Seg Display]
    SetOR --> Comparison
    TurnAO --> Setting[Setting Part Via Counter]
    Setting --> Encoder[Encoder]
    Encoder --> SegDisplay
  
```

FRAME 1: COLOR BLOCK

Red Block: Input
Purple Block: Basic Digital Clock
Yellow Block: Time Adjust Part
Brown Block: Show-Day Part
Green Block: Alarm Part

* We consumed more components than we have expected, and due to our running out of them, we had no choice but to leave the alarm function behind and add an hour alarm to take the place of it.

LAP CIRCUIT EXPERIMENT

Lapping circuit was not so successful to be honest. We have achieved most of our functions last Saturday, but because we bound the maximum current inappropriately, the first model was destroyed. : (

Last things last, here is our final model. :)

Name	Type	Quantity	Name	Type	Quantity
Battery Box		1	Seven Seg Encoder	74LS48D	12
Timer555		1	Switch		10
Capacitor	0.01μF	1	NOT Gate	74AS04M	20
	0.1μF	1	NAND Gate	7400N	20
Resistor	1kΩ	1	XOR Gate	7486N	10
	2kΩ	1	OR Gate	7432N	5
	100Ω	3	Piezo Buzzer		1
JK Flip Flop	74HC112	27	CMOS	IRF510	4
Seven Seg Display		12	LED		10



9 LITTLE THOUGHTS

1. Yiqing Huang

We picked up this project because we truly love it. So we made efforts to it and run out of our comfort zone. We struggle till the last minute to finish as more functions as we can.

To be honest, it is a pity that we lack time to reach our original goal to build a alarm. However, I am so glad that we can find a plan B and bring it into the actual circuit in a short time.

Ruyue is my best partner. We work out our plan smoothly and we exchange our ideas as soon as they came out of our minds. We sometimes argued with each other for our own thoughts or solutions to solve a specific problem and it do result in our remarkably high efficiency. We know when to stop and have a short break and when to insist on. We inspired each other when we were gotten in a dilemma and then fight a way out.

Maybe I will never make a second digital clock in the future but the experience in how to design a circuit, how to learn the usage of components in a fast way and most crucially how to fix unknown bugs in circuits must be rooted in my mind. And this is the essence of this course regardless of the result and the grade, which is extremely helpful.

Last but not least, thanks for my TA Shuo Ni, and thanks for my best partner Ruyue.

2. Ruyue Hong

Looking back on the week that past by, everyday is filled with depression and sudden surprise. Before entering the lab first time, we are occupied with fancy imagination that except accomplishing the required electric circuit we can even build an awesome appearance to cover the circuit which makes it like a real clock in our daily life, thus replacing the old clock with the home-made one. This kind of imagination continued even after the period we build the circuit first time. However, too many seemingly unsolvable bugs destroy our dream. It is easy for us to transfer the simulating one to real electric circuit, however, everyday we spend a large amount of time to figure out the reason why it fails to function even if the Multism runs successfully. I picked up the project simply out of my adoration. We came to the lab everyday with full enthusiasm, but it damped my passion gradually over time.

Those days are like the dark sky I saw every time I walked back to the dormitory with my partner. The little shining stars scattering above are like the final presentation which are shown to others. The darkness around the stars are just our normal days spent in the lab. Our depression , hundreds of time willing to give up combined with little success and sudden surprise are deeply hidden in the darkness which are only shown to us own. Fortunately, our effort are not in vain, we work things out in the end. During the process



to the final point, we are so worried about whether our time and effort will just be a speck of dusk in the galaxy or become the stars lighting up our days. But now, I have to admit that it is not the stars but the darkness that actually form the sky. We have to be thankful to ourselves, it is us who choose to keep on walking even our enthusiasm fading over time. We have to be thankful to my dear partner, who choose to accompany me walking under the dark sky even if he is so tired, even if I am so impatient with him. The final design is different from the initial one. It combined with the fancy ideas of Xiaoqingqing and me, it is also the outcome of our hundreds time of argument... so many words are just on the tip of my tongue but hard to speak them out. Never mind; just let them hidden in the dark sky, hidden in the days we passed by, and buried in our own memory.

10 REFERENCE

- Digital Fundamental Chapter 7 Flip-Flops.
- UC Berkeley, EECS100 Lab, Fall 2009.
- <https://en.wikipedia.org/wiki/CMOS>.

