Soc Design Laboratory

Lab3 Report

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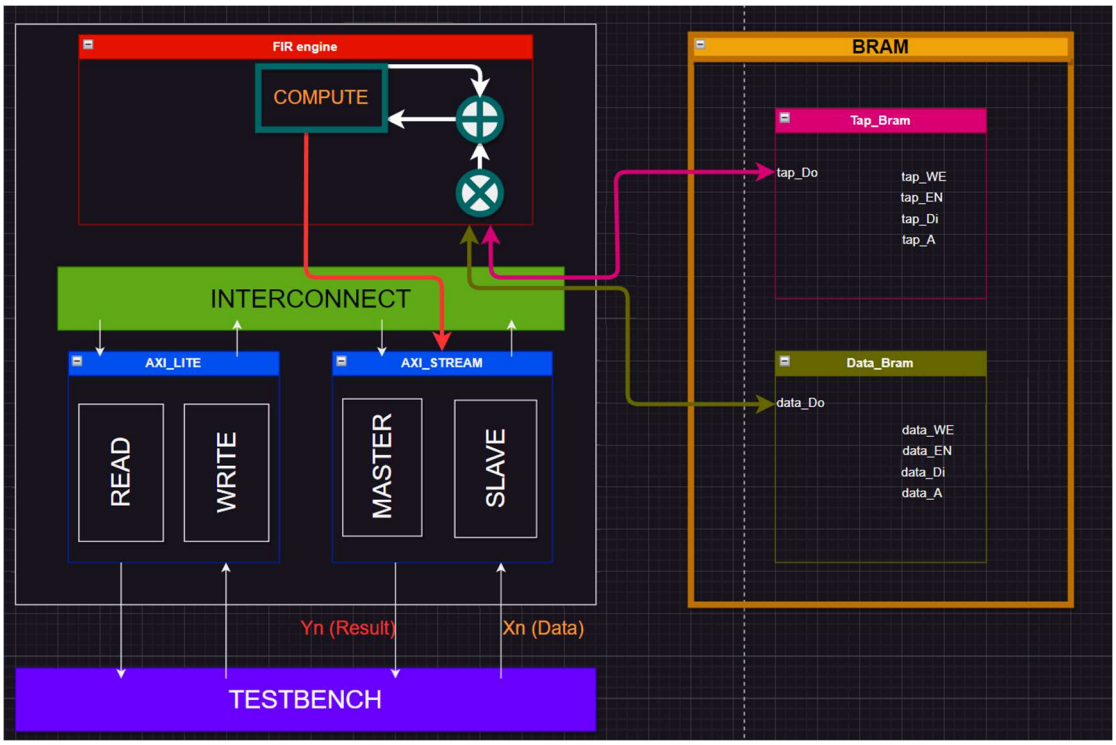
Block diagram:



Overview:

In this Lab3, our main task is to design an 11-tap FIR filter that communicates with the host and testbench through the AXI interface, which includes both AXI-LITE and AXI-Stream. Specifically, the AXI-LITE module is responsible for handling configuration commands such as starting (ap_start) or reading configuration status (ap_done, ap_idle), while the AXI-Stream primarily handles data transmission, including sending input values x[t] to the FIR filter and receiving the output once the FIR calculation is completed.

This design can be broadly divided into two main parts:

Configuration Part: This part utilizes the AXI-LITE interface to manage configuration inputs, allowing the setting of filter parameters.

FIR Dataflow Part: This section is responsible for the AXI-Stream interface and the calculation unit that generates the FIR output.

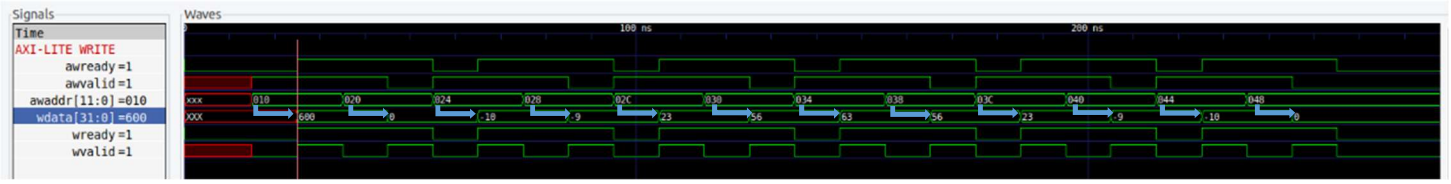
Additionally, the FIR filter has access to two BRAM modules designed at the behavioral level, known as Tap_ram and Data_ram. The Tap_ram stores the filter coefficients, while the Data_ram stores the previous inputs required for the calculation.

Moreover, the execution can be divided into two stages: the configuration stage and the calculation stage. The process begins with the configuration stage, where the host (testbench) sends the FIR coefficients to the FIR filter for storage in Tap_ram. Subsequently, the ap_start signal is set to activate the calculation stage, where the FIR filter receives FIR input from the host and performs the calculation to generate the FIR output.

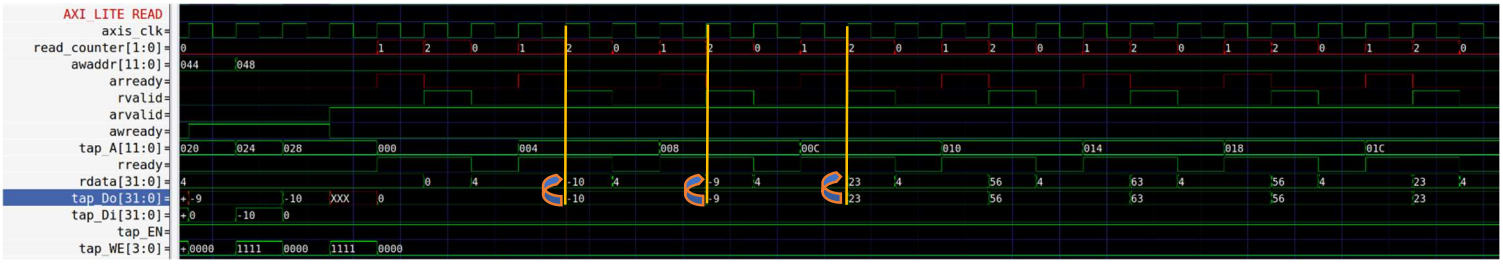
Operation:

AXI Lite Control: -

- ‘write_counter’ and ‘read_counter’ are used to coordinate AXI Lite write and read operations. They ensure that new operations are not provided until the current operation is completed.
- ‘awready’ and ‘wready’ indicate whether AXI Lite write operations can be accepted. They become 0 after completing the control operation to wait for the next operation. ‘wdata’ will be wrote by data from ‘awaddr’(⮡).



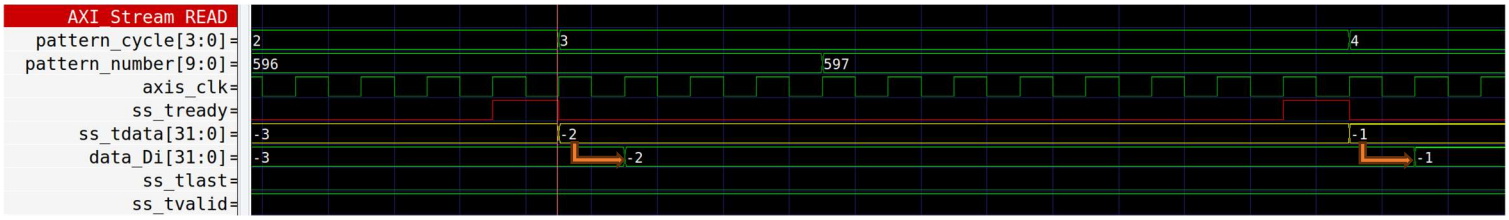
- ‘arready’ is used to indicate whether AXI Lite read operations can be accepted. ( )



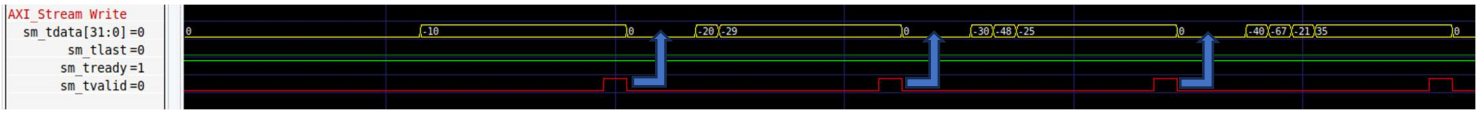
- ‘rvalid’ indicates the success of AXI Lite read operations.

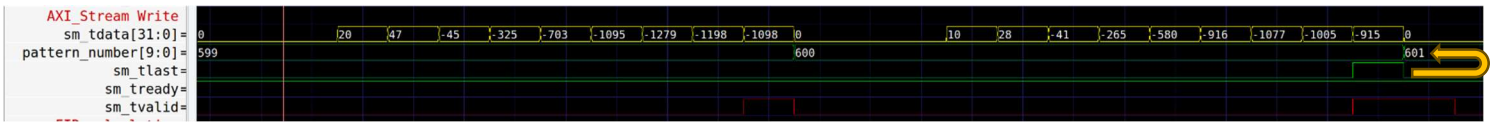
AXI Streaming Control:

- ‘ss_tready’ indicates the readiness of AXI Streaming, signifying whether new AXI Streaming data can be accepted. (⮡)



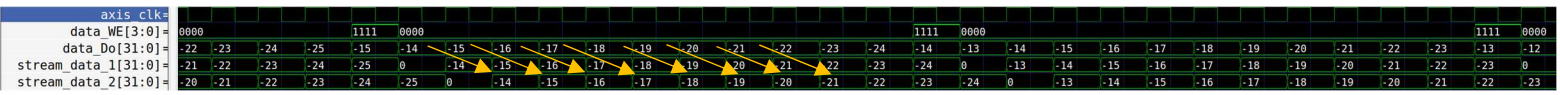
- ‘sm_tvalid’( ) and ‘sm_tlast’ ( )indicate the data validity and end flag of AXI Streaming.





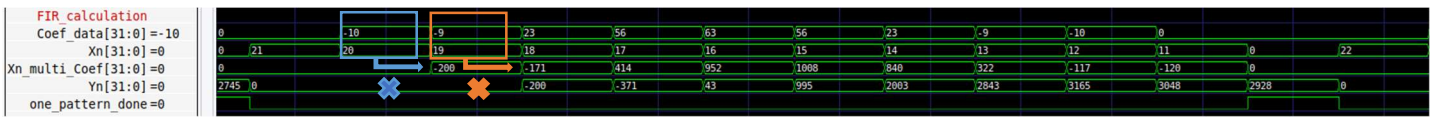
- ‘pattern_cycle’ and ‘pattern_number’ are used to calculate the quantity of AXI Streaming data. ‘pattern_cycle’ tracks the current pattern count(1~11), and ‘pattern_number’ tracks the count of the entire pattern.

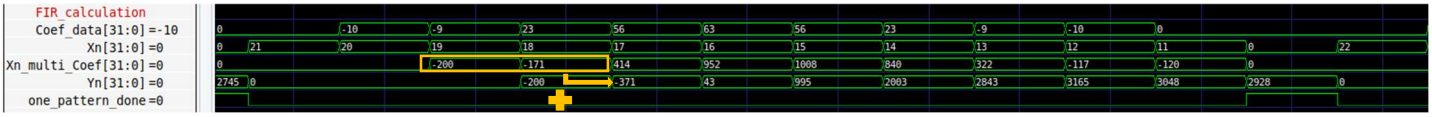
- ‘stream_data_1’ and ‘stream_data_2’ are used to buffer data from BRAM, which will be used for FIR filtering operations.
  (when data_WE = 1111 , data_Do-> stream_data_1-> stream_data_2)



FIR Calculation: -

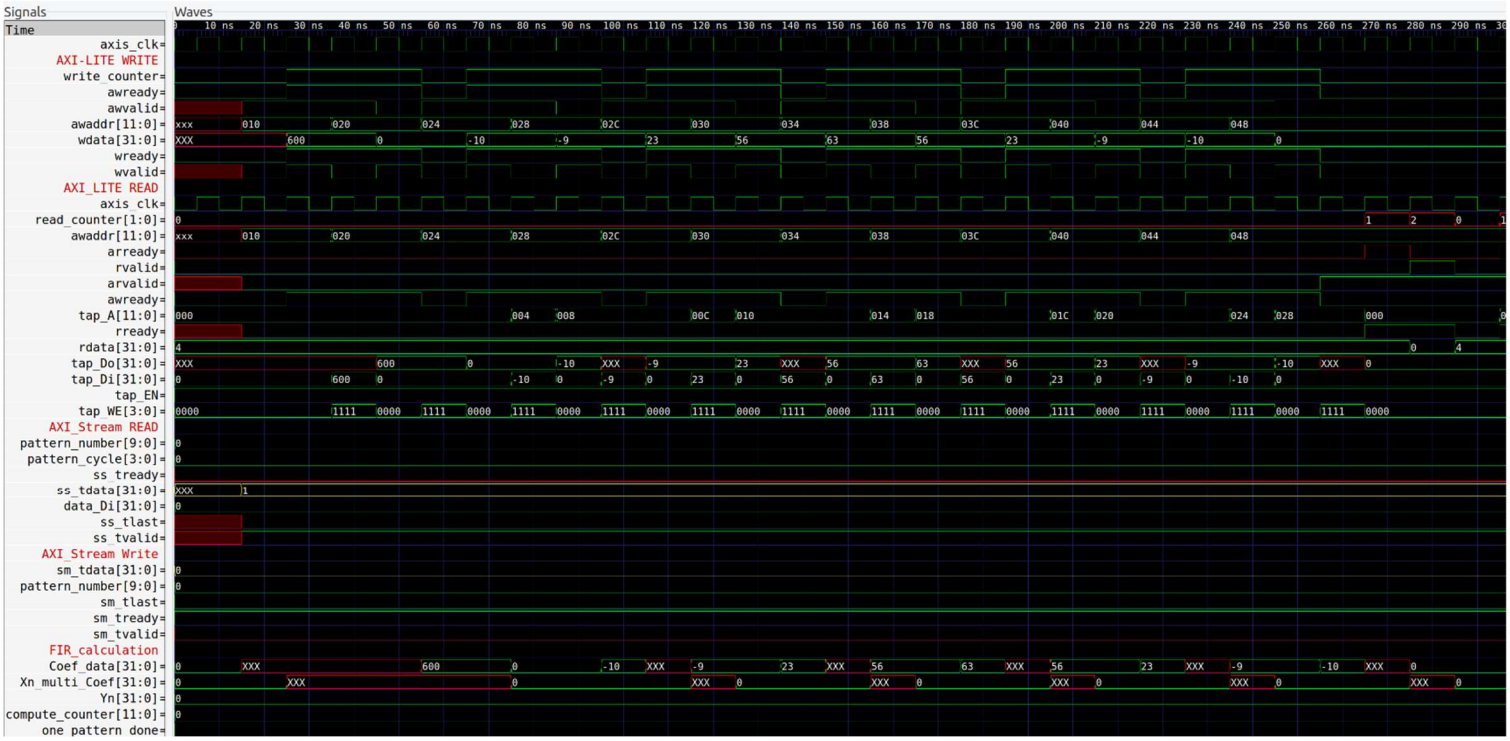
- ‘Coef_data’ is used to store the coefficients of the FIR filter.
- ‘Xn’ is used to store input data. ‘Xn_multi_Coef’ is used to store the result of input data multiplied by the coefficients.
- ‘Yn’ is used to store the output of the FIR filter.
- ‘one_pattern_done’ is used to identify whether a data pattern has been processed. It becomes 1 when ‘tap_A_counter’ is equal to 2 or when the current state is DONE, indicating the completion of processing for the current data pattern.





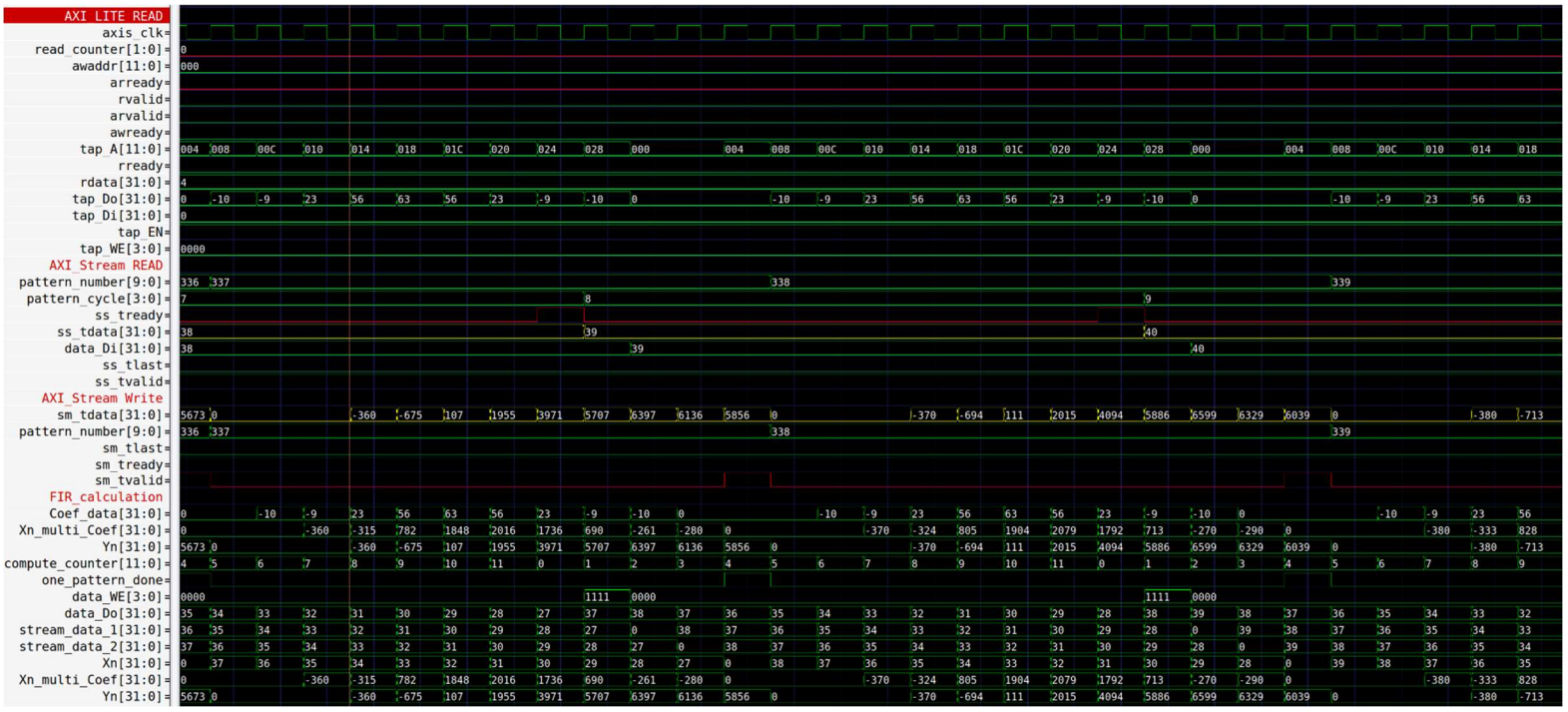
Simulation overall

The beginning



The end

Ram access data and FIR calculation



Resource usage:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	267	0	0	53200	0.50
LUT as Logic	267	0	0	53200	0.50
LUT as Memory	0	0	0	17400	0.00
Slice Registers	299	0	0	106400	0.28
Register as Flip Flop	299	0	0	106400	0.28
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
2	Yes	-	Set
297	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

Memory

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

DSP

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	3	0	0	220	1.36
DSP48E1 only	3				

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	327	0	0	125	261.60
Bonded IPADs	0	0	0	2	0.00
Bonded IOPADs	0	0	0	130	0.00
PHY_CONTROL	0	0	0	4	0.00
PHASER_REF	0	0	0	4	0.00
OUT_FIFO	0	0	0	16	0.00
IN_FIFO	0	0	0	16	0.00
IDELAYCTRL	0	0	0	4	0.00
IBUFDS	0	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	200	0.00
ILOGIC	0	0	0	125	0.00
OLOGIC	0	0	0	125	0.00

Clocking

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	16	0.00
MMCME2_ADV	0	0	0	4	0.00
PLLE2_ADV	0	0	0	4	0.00
BUFMRCE	0	0	0	8	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	16	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

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7. Primitives
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+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| FDCE     |  297 |        Flop & Latch |
| OBUF     |  169 |                  IO |
| IBUF     |  158 |                  IO |
| LUT2     |  127 |                 LUT |
| LUT3     |  126 |                 LUT |
| LUT6     |   70 |                 LUT |
| LUT4     |   32 |                 LUT |
| LUT1     |   25 |                 LUT |
| LUT5     |   21 |                 LUT |
| CARRY4   |   19 |          CarryLogic |
| DSP48E1  |    3 |    Block Arithmetic |
| FDPE     |    2 |        Flop & Latch |
| BUFG     |    1 |               Clock |
+----------+------+---------------------+
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Max Delay Paths

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Max Delay Paths
--------------------------------------------------------------------------------------
Slack:                    inf
  Source:                 tap_A_counter_reg[4]/C
                            (rising edge-triggered cell FDCE)
  Destination:            sm_tvalid
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        6.448ns  (logic 3.647ns (56.566%)  route 2.801ns (43.434%))
  Logic Levels:           5  (FDCE=1 LUT1=1 LUT6=2 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                       FDCE                         0.000     0.000 r  tap_A_counter_reg[4]/C
                       FDCE (Prop_fdce_C_Q)         0.478     0.478 f  tap_A_counter_reg[4]/Q
                       net (fo=8, unplaced)         1.003     1.481    p_0_in0
                                                                       f  sm_tlast_OBUF_inst_i_2/I0
                       LUT6 (Prop_lut6_I0_O)        0.295     1.776 r  sm_tlast_OBUF_inst_i_2/O
                       net (fo=66, unplaced)        0.538     2.314    sm_tlast_OBUF_inst_i_2_n_0
                                                                       r  sm_tvalid_OBUF_inst_i_2/I5
                       LUT6 (Prop_lut6_I5_O)        0.124     2.438 f  sm_tvalid_OBUF_inst_i_2/O
                       net (fo=2, unplaced)         0.460     2.898    sm_tvalid_OBUF_inst_i_2_n_0
                                                                       f  sm_tvalid_OBUF_inst_i_1/I0
                       LUT1 (Prop_lut1_I0_O)        0.116     3.014 r  sm_tvalid_OBUF_inst_i_1/O
                       net (fo=1, unplaced)         0.800     3.814    sm_tvalid_OBUF
                                                                       r  sm_tvalid_OBUF_inst/I
                       OBUF (Prop_obuf_I_O)         2.634     6.448 r  sm_tvalid_OBUF_inst/O
                       net (fo=0)                   0.000     6.448    sm_tvalid
                                                                       r  sm_tvalid (OUT)
  -------------------------------------------------------------------    -------------------
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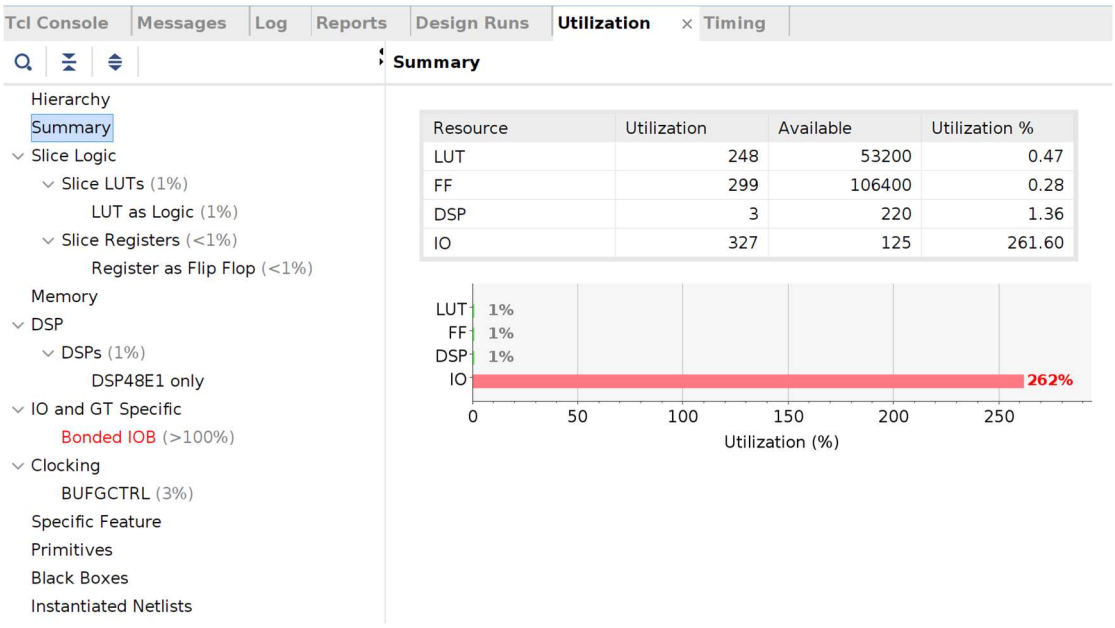
Timing

LUT&FF



Summary

In this experiment, I learned a great deal. It all started with designing circuits, understanding how to use AXI-lite for coefficient retrieval, and progressing to AXI-Stream data transmission. We also had to design a Finite State Machine (FSM) for efficient mode switching. Besides circuit design, we had to create the corresponding testbench and use gtkwave for waveform analysis and debugging. As someone with limited prior experience in Verilog programming, this entire process proved to be quite a substantial challenge.

Fortunately, I had many classmates taking the same course, which allowed for discussions and mutual support. However, the experiment did present its share of challenges, including power outages and program issues that caused delays in our progress. Nevertheless, we ultimately succeeded in completing the experiment, which brought a great sense of accomplishment and joy.

I look forward to successfully completing future labs and continuing to learn and grow.