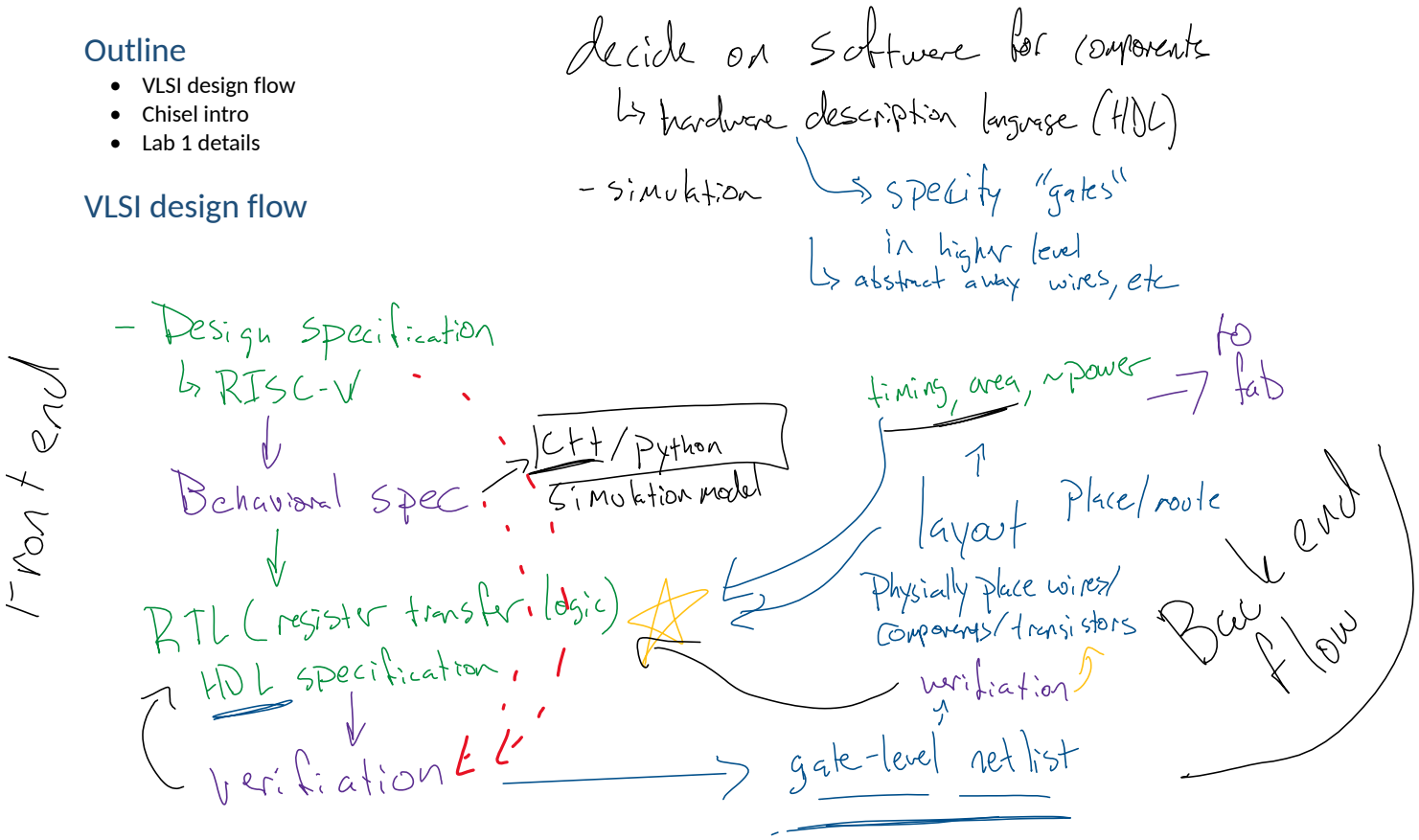
Discussion 1: Chisel + VLSI

Thursday, January 10, 2019 12:24 PM

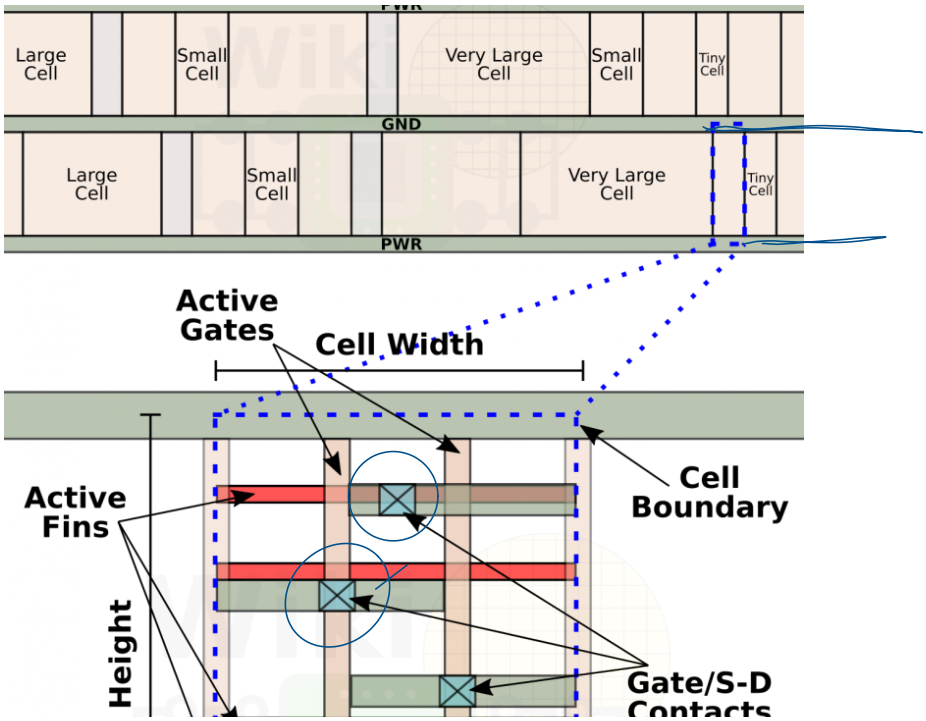
Outline

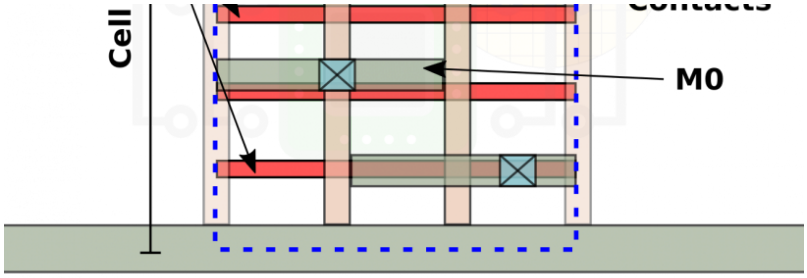
- VLSI design flow
- Chisel intro
- Lab 1 details

VLSI design flow



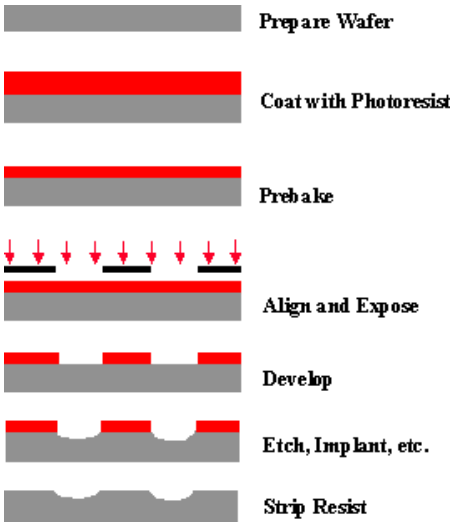
Standard Cells





https://fuse.wikichip.org/news/2004/iedm-2018-intels-10nm-standard-cell-library-and-power-delivery

Photolithography



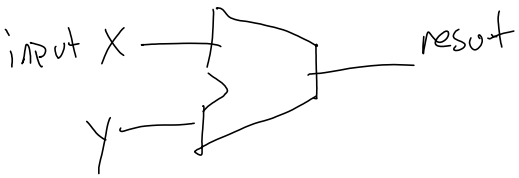
Chisel

https://chisel.eecs.berkeley.edu/

Scala functional
+ pure object oriented

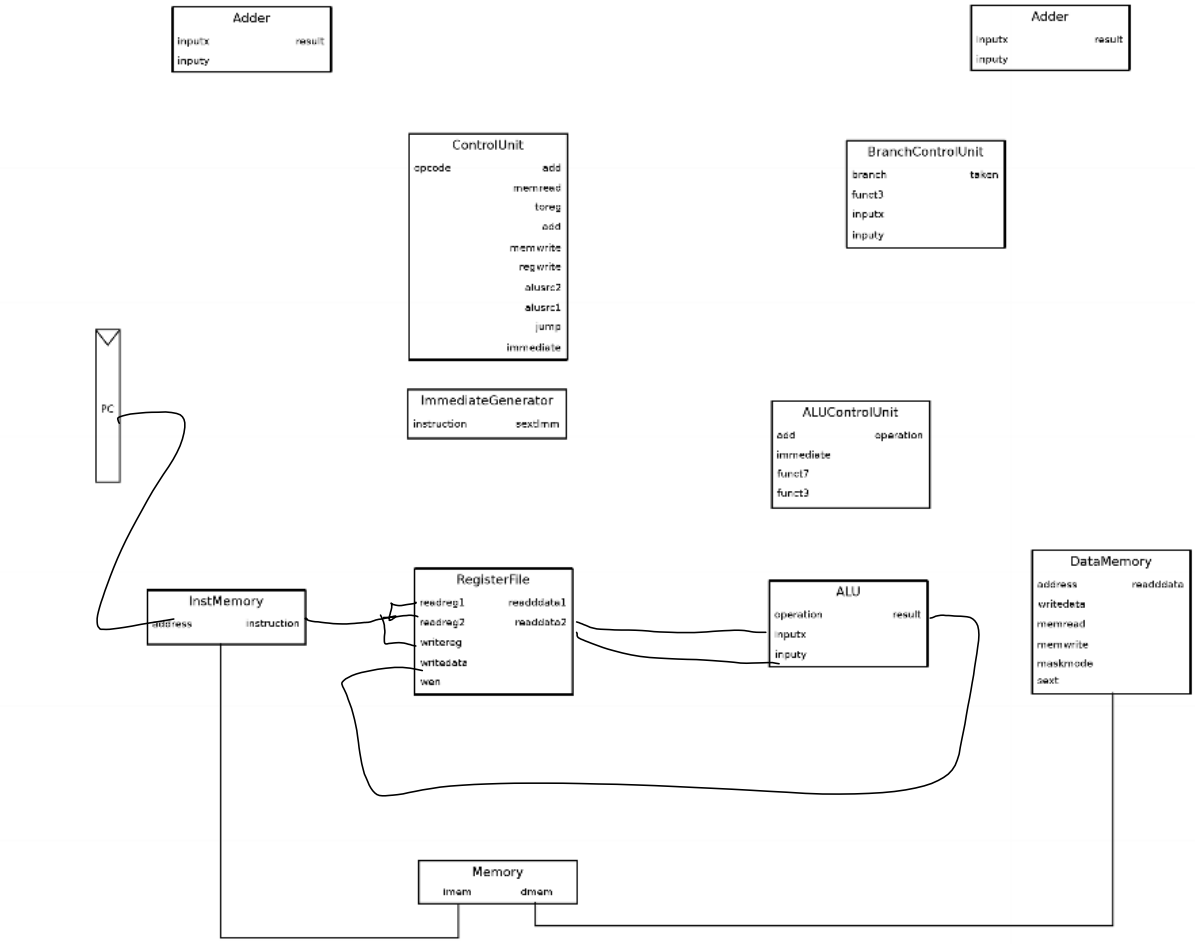
Domain-specific language in scala

use singularity container specified in lab



Lab 1

Filling in the diagram (part 2)


Adder
inputx
inputy
result
Adder
inputx
inputy
result
ControlUnit
opcode
add
memread
toreg
add
memwrite
regwrite
alusrc2
alusrc1
jump
immediate
BranchControlUnit
branch
funct3
inputx
inputy
taken
PC
ImmediateGenerator
instruction
sextimm
ALUControlUnit
add
immediate
funct7
funct3
operation
InstMemory
address
instruction
RegisterFile
readreg1
readreg2
writereg
writedata
wen
readdata1
readdata2
ALU
operation
inputx
inputy
result
DataMemory
address
writedata
memread
memwrite
maskmode
sext
readdata
Memory
imem
dmem

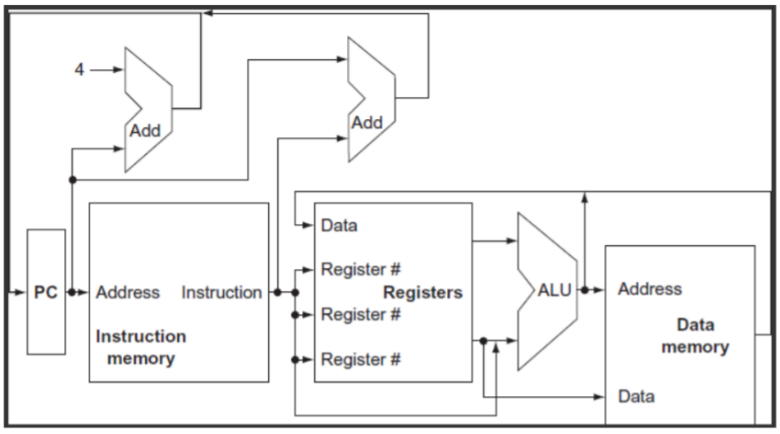

4
Add
Add
PC
Address
Instruction
Instruction memory
Data
Register #
Registers
Register #
Register #
ALU
Address
Data memory
Data

Figure 04-01