Lecture 3: More technology

Wednesday, January 9, 2019 6:40 PM

Outline

- Energy and power of CMOS devices
- Trends in technology
- Start on ISA/instructions, if time

IF A RESEARCHER SAYS A COOL NEW TECHNOLOGY SHOULD BE AVAILABLE TO CONSUMERS IN...

	WHAT THEY MEAN IS...
THE FOURTH QUARTER OF NEXT YEAR	THE PROJECT WILL BE CANCELED IN SIX MONTHS.
FIVE YEARS	I'VE SOLVED THE INTERESTING RESEARCH PROBLEMS. THE REST IS JUST BUSINESS, WHICH IS EASY, RIGHT?
TEN YEARS	WE HAVEN'T FINISHED INVENTING IT YET, BUT WHEN WE DO, IT'LL BE AWESOME.
25+ YEARS	IT HAS NOT BEEN CONCLUSIVELY PROVEN IMPOSSIBLE.
WE'RE NOT REALLY LOOKING AT MARKET APPLICATIONS RIGHT NOW.	I LIKE BEING THE ONLY ONE WITH A HOVERCAR.

Energy and Power of CMOS devices

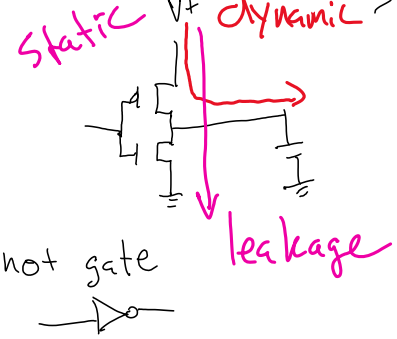
How do energy and power relate?

$P = E/time$

Constraints
Energy + power

Energy costs money → Battery for mobile
↳ Wh

Power → heat dissipation → mobile limited by human hand
↳ Wh
↳ tech to cool
fan vs fanless vs water cooling
↳ energy to cool



Energy =

Static energy: constant output

Dynamic energy: Depends on switching

Static energy increases w/ smaller transistors

Dynamic energy of a system = $\alpha C \cdot V^2$

α: activation, # transistors switching
C: capacitance

Power:

Dynamic Power of chip $= \alpha C V^2 \cdot f$ (f → frequency)

If we are power/energy constrained: How do we reduce power/energy?

$E = \alpha C V^2$

$P = \alpha C V^2 f$

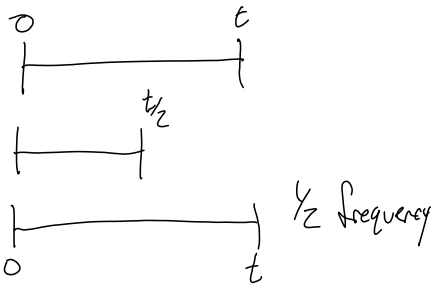
$E = P \cdot t$

reduce power by reducing freq → longer to run program

reduce voltage → errors
↳ threshold voltage ~ 0.7 V
→ lower voltage slower transitors

fewer transistors
↳ C goes down
→ fewer "features" on chip

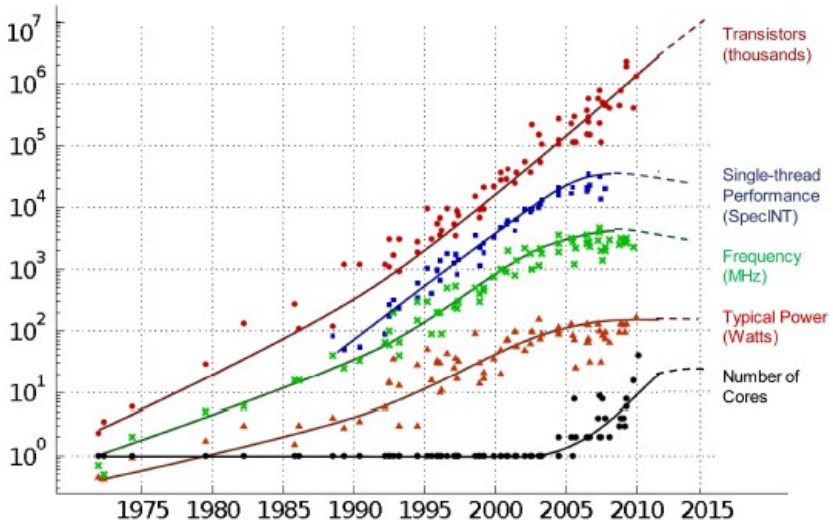
★ turn off early



Better instruction sets
↳ multiple things per cycle
→ parallelism
reduce freq

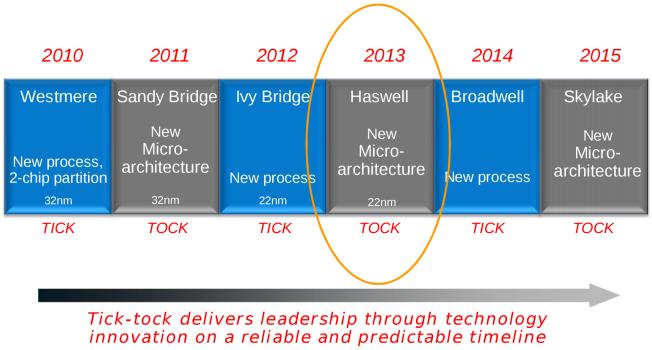
Trends

35 Years of Microprocessor Trend Data

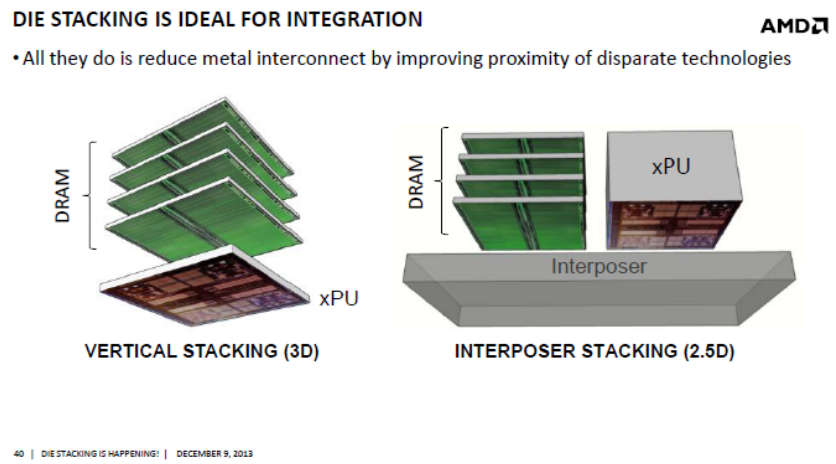


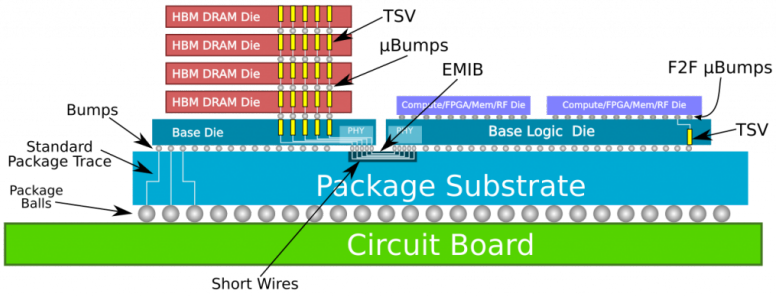
Slides from Intel

Intel Tick-Tock Model



Other trends





[John Hennessy and David Patterson 2017 ACM A.M. Turing Award Lecture]