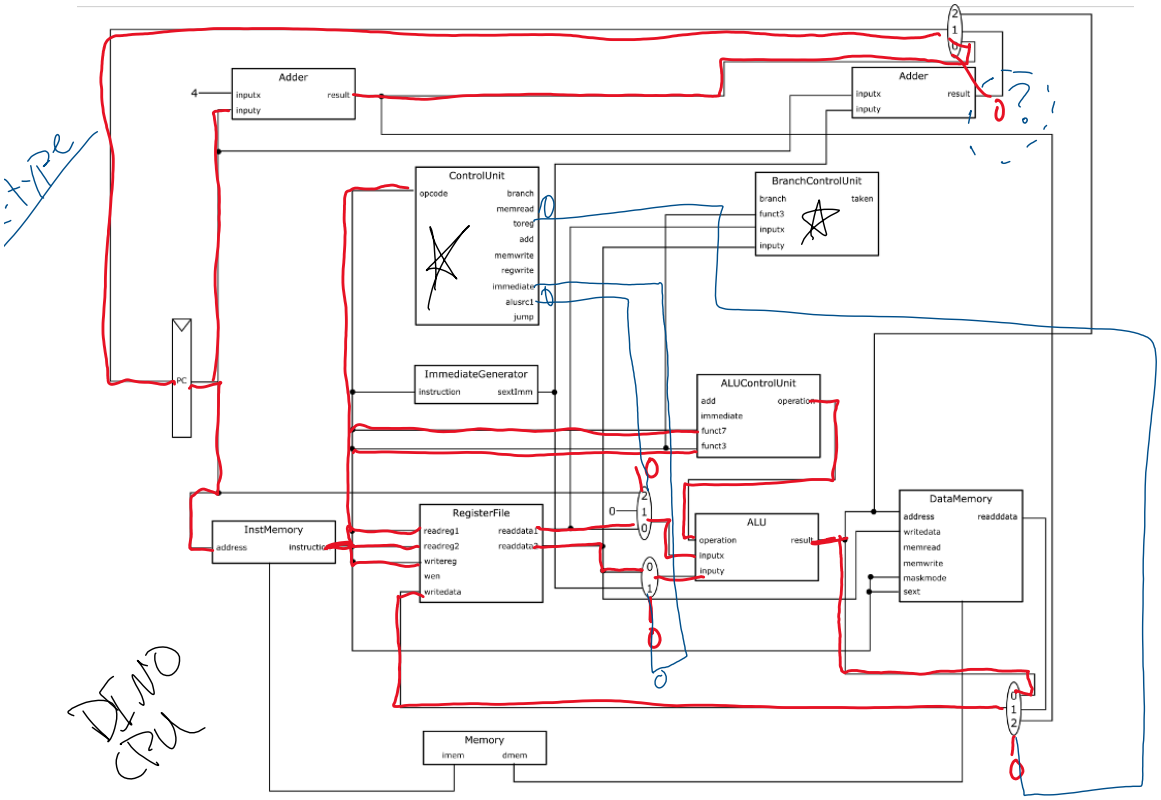
Discussion 3: Single cycle + Performance

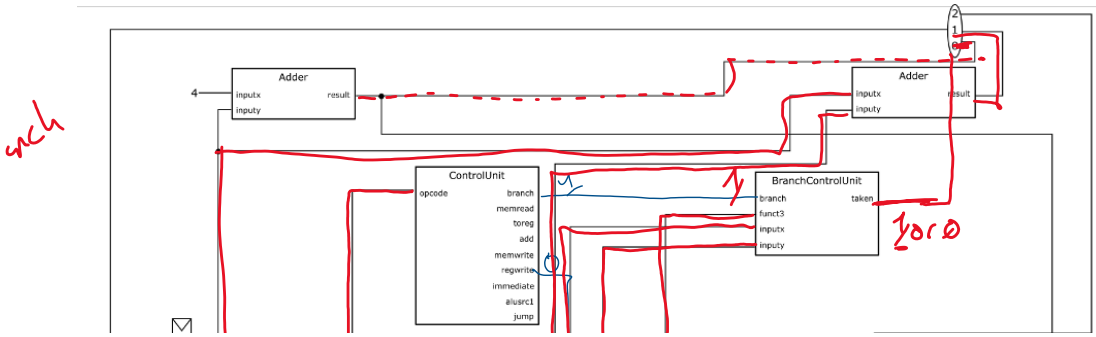
Thursday, January 24, 2019 1:54 PM

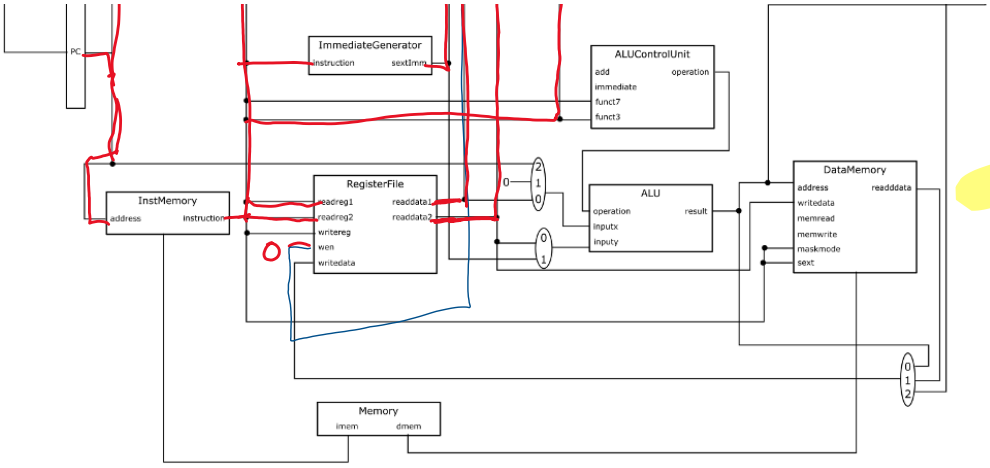
Outline

- Lab 2 overview
- More on single cycle CPU control
- Revisit the Iron Law
- Single cycle CPU performance

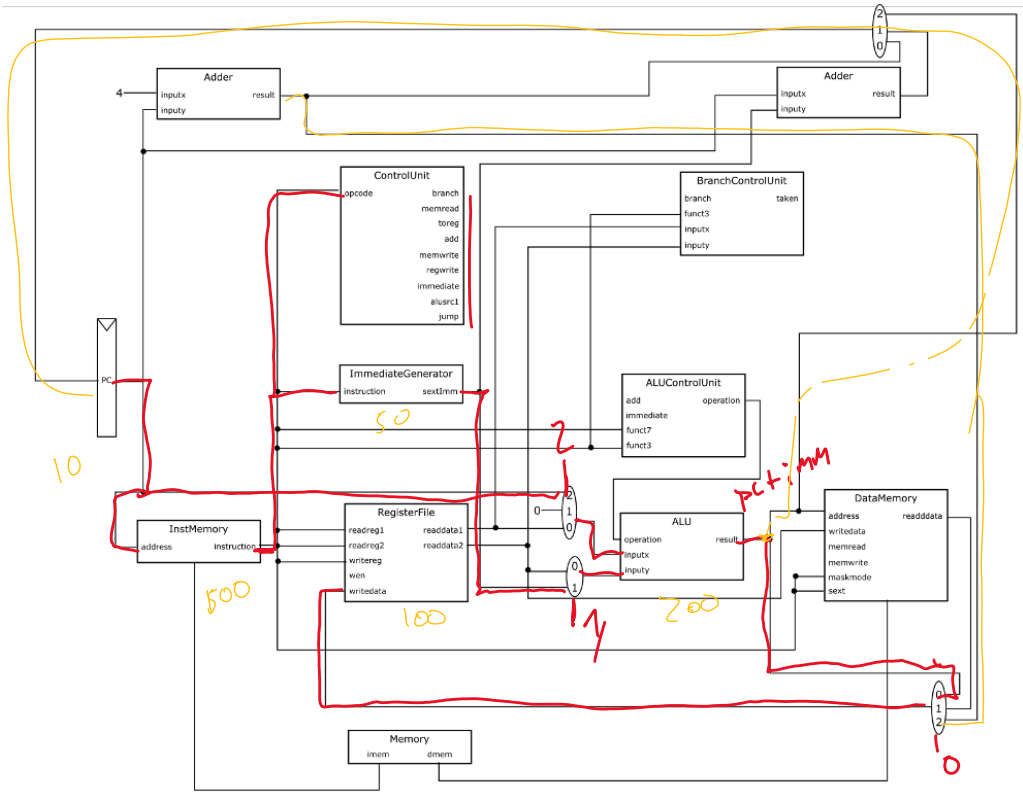
lab 2 posted
-> github.com/UPteaching/dino-cpu
↳ master has been updated
-> full application
↳ if problems -> post on piazza
-> Don't change I/O
->I'll be adding docs from last lecture soon







slow through data path



auipc
add upper imm to pc

R[rd] = pc + imm

jalr

pc = R[rs1] + imm
R[rd] = pc+4

Iron Law

$$\frac{\text{seconds}}{\text{cycle}} \times \frac{\text{cycles}}{\text{inst}} \times \frac{\text{inst}}{\text{program}} = \frac{\text{seconds}}{\text{program}}$$

technology impl. | micro arch impl. | program/compiler/ISA

Single cycle CPU performance

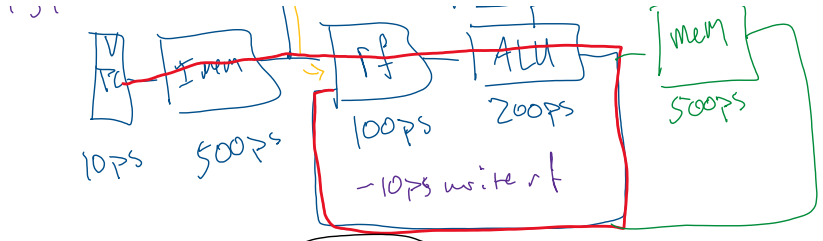
? $\times$ 1 $\times$ 10,000 r-type inst = ~~8.1 ms~~ ?

~~810 ps~~ 1210

50ps (control) + 10ps (ALU ctrl)

13.1 ms

load inst

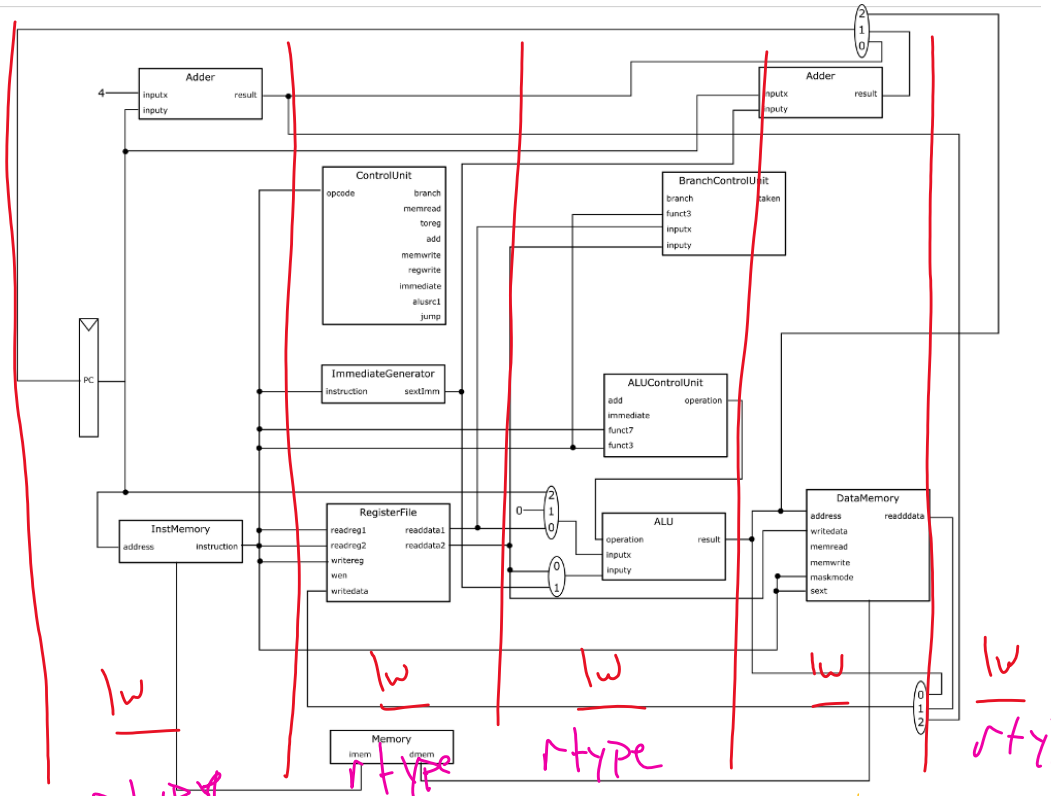


R type → 810 ps 870ps → 1.23 GHz

looking for worst case

lw → 1310 ps → 760 MHz ? worst case

jalr → ~810ps



lw lw lw lw lw

rtype rtype rtype

500ps 500ps

2GHz

50% rtype → 4 cycles

50% lw → 5 cycles

Perf = 500ps X CPI X 10,000 insts

5/cycle 4.5

= 22.50 μs