

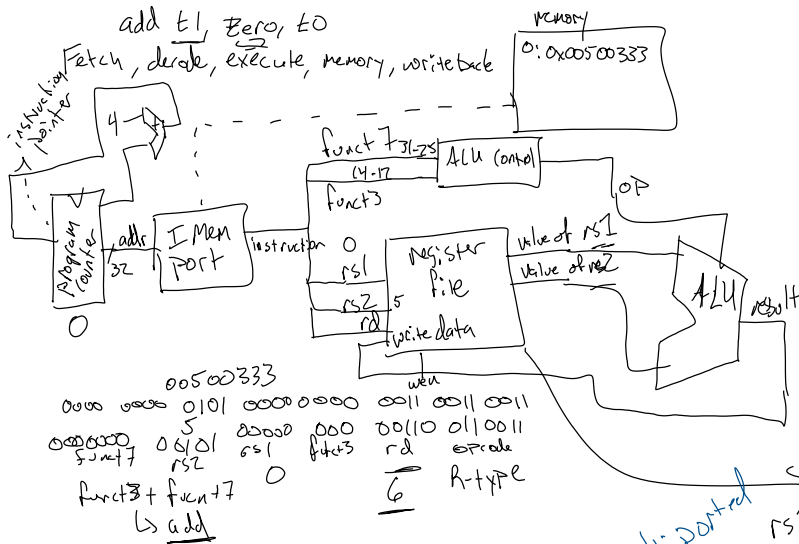
Thursday, January 17, 2019 10:10 AM

- Lab announcements
- Examples of executing RISC-V instructions
- Other lab questions

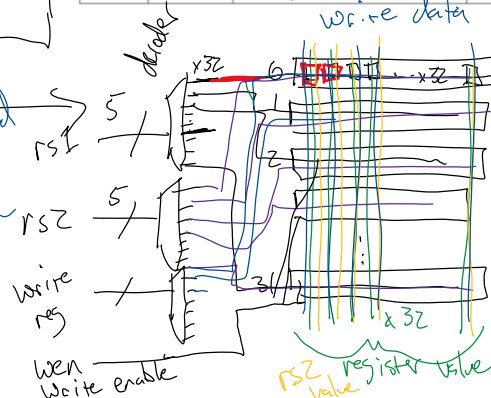
-bug \rightarrow fixed instruction (12, 7) $\neq 0.4$
 $1 \neq 1$ use this

↳ Control unit has all 0 output

31	27	26	25	24	20	19	15	14	12	11	7	6	0	
funct7				rs2		rs1		funct3		rd		opcode		R-type
imm[11:0]						rs1		funct3		rd		opcode		I-type
imm[11:5]				rs2		rs1		funct3		imm[4:0]		opcode		S-type
imm[12:0:5]						rs1		funct3		imm[4:1][11]		opcode		B-type
				imm[31:12]						rd		opcode		U-type
				imm[20:10][11:19:12]								opcode		J-type



Register	ABI Name	Description	Saver
x0	ra	Hard-wired zero	
x1	ro	Return address	Caller
x2	sp	Stack pointer	Callee
x3	gp	Global pointer	—
x4	tp	Thread pointer	—
x5	t0	Temporary/alternate link register	Caller
x6	t1	Temporaries	Caller
x7	s0/fp	Saved register/frame pointer	Callee
x9	s1	Saved register	Callee
x10-11	a0-1	Function arguments/return values	Caller
x12-17	a2-7	Function arguments	Caller
x18-27	a2-11	Saved registers	Callee
x28-31	t3-6	Temporaries	Caller
f0-7	f0-7	FP temporaries	Caller
f8-9	fo-1	FP saved registers	Callee
f10-11	fo-1	FP arguments/return values	Caller
f12-17	fa2-7	FP arguments	Caller
f18-27	fa2-11	FP saved registers	Callee
f28-31	ft8-11	FP temporaries	Caller



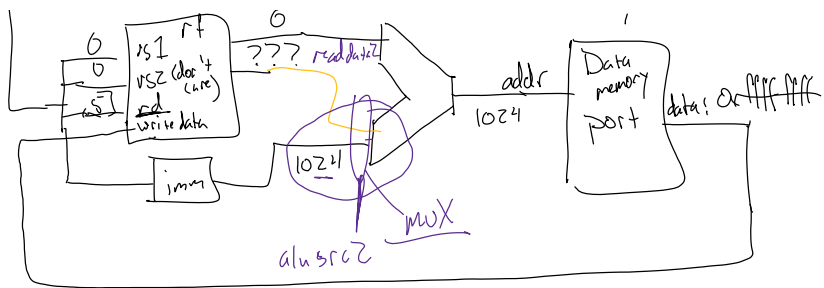
Example 2:

Diagram illustrating the instruction format and its components:

- Instruction: 0: 40002283, 4: 00000000, 1024: 0xffffffff
- I Mem Port
- V PC: 0
- 4000 22 83
- 0100 0000 0000 0010 0010 1000 0011 0100 0000 0000 0101 0010 0000 0011
- rs1 funct3 rd opcode
- immediate

	imm	11:0		rs1	000	rd	0000011	LE
	imm	11:0		rs1	001	rd	0000011	LF
	imm	11:0		rs1	010	rd	0000011	LW
	imm	11:0		rs1	100	rd	0000011	LE
	imm	11:0		rs1	101	rd	0000011	LF
	imm	11:5	rs2	rs1	000	imm 4:0	0100011	SB
	imm	11:5	rs2	rs1	001	imm 4:0	0100011	SH
	imm	11:5	rs2	rs1	010	imm 4:0	0100011	SW

$$lw \rightarrow Mem[R[rs] + imm] \rightarrow R[rd]$$



address