XLINIX REPORT

Device utilization summary:

Selected Device : 5vlx50tff1136-2

Slice Logic Utilization:

Number of Slice Registers: 30 out of 28800 0%

Number of Slice LUTs: 30 out of 28800 0%

Number used as Logic: 30 out of 28800 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 30

Number with an unused Flip Flop: 0 out of 30 0%

Number with an unused LUT: 0 out of 30 0%

Number of fully used LUT-FF pairs: 30 out of 30 100%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 34

Number of bonded IOBs: 34 out of 480 7%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

Partition Resource Summary:

No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	30

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
reset	IBUF	30

Timing Summary:

Speed Grade: -2

Minimum period: 2.140ns (Maximum Frequency: 467.322MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 2.830ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.140ns (frequency: 467.322MHz)

Total number of paths / destination ports: 465 / 30

Delay: 2.140ns (Levels of Logic = 31)

Source: core/pc_2 (FF)

Destination: core/pc_31 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: core/pc_2 to core/pc_31

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 30 / 30

Offset: 2.830ns (Levels of Logic = 1)

Source: core/pc_31 (FF)

Destination: pc_out<31> (PAD)

Source Clock: clk rising

Data Path: core/pc_31 to pc_out<31>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDC:C->Q	2	0.396	0.290	core/pc_31 (core/pc_31)
OBUF:I->O		2.144		pc_out_31_OBUF (pc_out<31>)
Total		2.830ns (2.540ns logic, 0.290ns route)		
		(89.8% logic, 10.2% route)		

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Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 5.70 secs

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Total memory usage is 4563536 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 19 (0 filtered)

Number of infos : 2 (0 filtered)

top_riscv Project Status (10/31/2025 - 11:15:26)			
Project File:	jeyawin.xise	**Parser Errors:**	No Errors
Module Name:	top_riscv	**Implementation State:**	Placed and Routed
Target Device:	xc5vlx50t-2ff1136	• **Errors:**	No Errors
Product Version:	ISE 14.6	• **Warnings:**	19 Warnings (8 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

DEVICE UTILIZATION SUMMARY

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	30	28,800	1%	
Number used as Flip Flops	30			
Number of Slice LUTs	30	28,800	1%	
Number used as logic	29	28,800	1%	
Number using O5 output only	28			
Number using O5 and O6	1			
Number used as exclusive route-thru	1			
Number of route-thrus	29			
Number using O6 output only	29			
Number of occupied Slices	8	7,200	1%	
Number of LUT Flip Flop pairs used	30			
Number with an unused Flip Flop	0	30	0%	
Number with an unused LUT	0	30	0%	
Number of fully used LUT-FF pairs	30	30	100%	
Number of unique control sets	1			
Number of slice register sites lost to control set restrictions	2	28,800	1%	
Number of bonded IOBs	34	480	7%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Average Fanout of Non-Clock Nets	2.51			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri 31. Oct 11:14:05 2025	0	19 Warnings (8 new)	2 Infos (0 new)
Translation Report	Current	Fri 31. Oct	0	0	0

		11:14:52 2025			
Map Report	Current	Fri 31. Oct 11:15:04 2025	0	0	6 Infos (6 new)
Place and Route Report	Current	Fri 31. Oct 11:15:17 2025	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri 31. Oct 11:15:25 2025	0	0	4 Infos (4 new)
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

Date Generated: 10/31/2025 - 11:15:26