EE800/820 Weekly Status Report

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Project Advisor: Bernard Yett
Week of: February 9, 2026
Project: An Educational Framework for AI-Driven RF Signal Processing on FPGA

Accomplishments This Week

- Met with Dr. Yett to discuss project direction and proposal scope
- Completed the research proposal by the February 10 deadline, pending review and approval.
- Ordered STM32 Nucleo-L476RG microcontrollers for use as beacon targets
- Set up Vivado development environment for the Nexys A7-100T
- Began preliminary literature review on FPGA-based signal processing and integrated curriculum design

Goals for Next Week

- Collect and review research papers from the last five years on FPGA-based RF signal processing, embedded system integration, and applied ML for signal classification
- Evaluate and select a radio module for the beacon subsystem (LoRa, sub-GHz ISM, or alternative)
- Begin outlining the curriculum module sequence based on literature findings
- Confirm STM32 delivery timeline and verify board functionality upon arrival

Potential Blockers

- Limited published work combining FPGA and ML in an educational or signal processing context may narrow the literature base
- STM32 delivery timeline is uncertain and could delay initial hardware integration testing
- Radio module selection remains open, which blocks detailed system architecture and interface design decisions