

Research Proposal

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I pledge to adhere to the Stevens Graduate Student Code of Academic Integrity, and I have discussed the proposal with my Project Advisor.

Signature Date

FPGA-Based Signal Processing System

Student: Jude Eschete

Project Advisor: Dr. Bernard Yett

1 Introduction

2 Problem Description

3 Expected Contributions

4 Project Timeline

Date Range	Milestone
Feb 10 - Feb 28	Literature review and requirements finalization
Mar 1 - Mar 21	Algorithm design and simulation in MATLAB/Python
Mar 22 - Apr 11	FPGA implementation (RTL design, synthesis)
Apr 12 - Apr 25	Testing, verification, and performance benchmarking
Apr 26 - May 9	Final report writing and presentation preparation
May 10 - May 16	Final submission and defense