Research Proposal

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Signature Date

An Educational Framework for AI-Driven Signal Processing

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1 Introduction

Field-Programmable Gate Arrays (FPGAs), Radio-Frequency (RF) communication systems, microcontroller-based embedded platforms, and Machine Learning (ML) each represent core pillars of modern electrical engineering education. However, university curricula frequently treat these disciplines in isolation. Students may complete a digital design course that introduces Hardware Description Language (HDL) synthesis on an FPGA, a separate communications course covering modulation and RF signal theory, an embedded systems course focused on microcontroller peripherals and firmware development, and a machine learning course built around static datasets, yet rarely encounter a structured experience that requires them to integrate these domains into a cohesive working system. This gap leaves graduates underprepared for the multidisciplinary demands of industries such as defense, telecommunications, and aerospace, where systems routinely require real-time RF data acquisition, hardware-accelerated processing, and intelligent decision-making within a single pipeline.

This project addresses that gap by developing a structured, progressive educational guide built around the design and implementation of an Artificial Intelligence (AI)-driven RF signal processing system on FPGA. The target audience is senior undergraduate and master's-level electrical engineering students who have foundational exposure to digital design, signals and systems, embedded programming, and introductory machine learning but lack experience synthesizing these skills into an integrated system. Rather than presenting these topics as independent modules, the guide sequences them so that each stage builds on the previous one, culminating in a complete pipeline where students collect RF data from real hardware, process it on reconfigurable logic, and apply machine learning models to classify or characterize the received signals.

2 Problem Description

The system under development is a benchtop signal processing platform composed of three subsystems. Multiple STM32 Nucleo-L476RG microcontrollers, each paired with a low-power radio module such as a Long Range (LoRa) transceiver, serve as cooperative beacon targets that transmit known signals at configurable intervals and parameters. A separate receiver station captures these transmissions and feeds the incoming RF data to a Digilent Nexys A7-100T FPGA, which performs detection, identification, and prioritization of the received signals in real time. Processed signal data is then collected and used to train and evaluate machine learning models for tasks such as signal classification, emitter identification, or anomaly detection. As students progress through the guide, they scale the system from a single beacon and basic signal detection to multiple simultaneous targets, increasing the processing demands placed on the FPGA and the complexity of the classification task at each stage.

This architecture presents several concrete engineering challenges that the guide must address. The FPGA must ingest data from multiple asynchronous RF sources, each transmitting independently, requiring careful clock domain management and buffering strategies. As the number of active beacons grows, the processing pipeline must classify and prioritize incoming signals under real-time throughput and latency constraints while remaining within the logic, memory, and timing resources available on the Artix-7 fabric. Bridging the microcontroller and FPGA domains introduces additional complexity in interface design, protocol selection such as Serial Peripheral Interface (SPI) or Universal Asynchronous Receiver-Transmitter (UART), and synchronization between heterogeneous hardware. On the AI side, students must design a data collection pipeline that captures labeled signal features from the FPGA, select and train appropriate models, and evaluate classification performance against real-world RF data rather than curated academic datasets.

3 Expected Contributions

The principal contribution of this project is a unified pedagogical framework that treats FPGA design, RF communications, embedded systems, and applied machine learning not as four independent subjects but as a single integrated discipline with its own design principles, interface patterns, and system-level reasoning. Existing educational resources address each domain thoroughly in isolation, and individual capstone projects may combine two of the four, but no published curriculum presents a structured methodology for teaching students how the entire pipeline connects: how digital hardware design decisions propagate into RF system behavior, how embedded firmware must adapt to the timing and resource realities of reconfigurable logic, how RF link characteristics constrain the architecture of the processing back end, and how the resulting data informs and challenges the machine learning models that operate on it. This project fills that gap by identifying and articulating the theoretical connections across all four domains and organizing them into a progressive learning sequence where each integration point becomes an explicit teaching objective rather than an incidental implementation detail.

The resulting curriculum is designed around weekly assignments using commercially available hardware, specifically the Digilent Nexys A7-100T, STM32 Nucleo-L476RG microcontrollers, and LoRa transceiver modules, with all development tools either free or available through standard academic licenses. This choice ensures that the curriculum is reproducible at other institutions without requiring custom hardware or proprietary infrastructure. However, the core contribution is not the hardware platform or the individual assignments but the synthesis itself: a documented, teachable model of how these four disciplines interact at the system level, from RF data collection through hardware-accelerated processing to intelligent classification, supported by a concrete implementation that students can build, test, and reason about as a unified whole.

4 Project Timeline

Date Range	**Milestone**
Feb 10 - Feb 28	Literature review; finalize RF radio module selection and hardware requirements
Mar 1 - Mar 14	Design RF beacon and receiver subsystem; define curriculum module sequence
Mar 15 - Mar 28	FPGA Register-Transfer Level (RTL) design and signal processing simulation
Mar 29 - Apr 11	Integrate STM32 beacons with FPGA receiver; develop initial curriculum labs
Apr 12 - Apr 25	Implement ML classification pipeline on collected RF data; draft remaining labs
Apr 26 - May 9	System testing and benchmarking; finalize curriculum documentation
May 10 - May 16	Final report writing, presentation preparation, and defense