Week 4 Application Assignment: Mission 007

Overview

The goal of this assignment is to extend your knowledge of schematic design using Quartus Prime by using pipelining and IP blocks to improve design performance. The student should be following the video instructions and creating the example as they go along. Their progress is checked at milestones by presenting screenshots which are matched to the solution screenshots to verify their work. Milestones checked are design schematic creation, timing improvement with pipelining, pin assignment, timing analysis and simulation.

This assignment is required. Peers must review 3 submissions to pass the assignment.

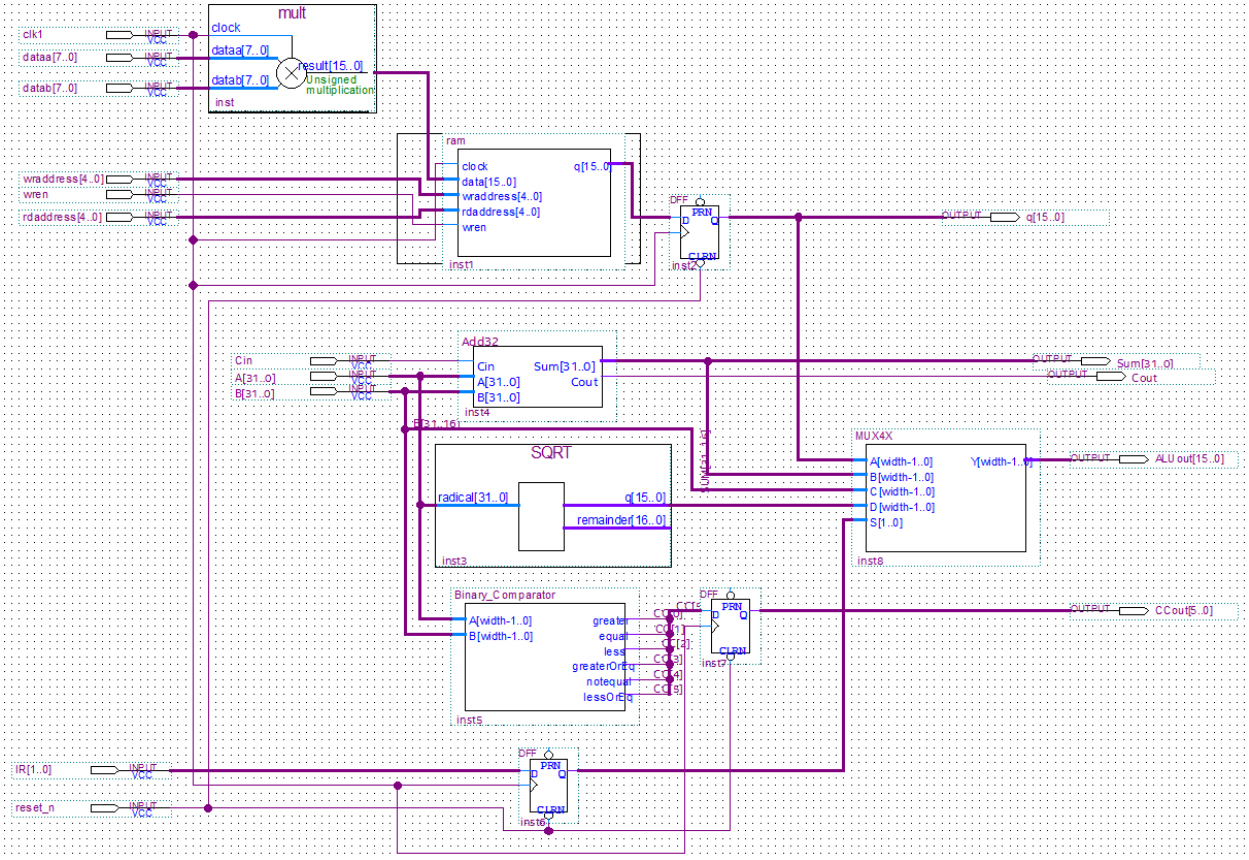
Submit screenshots (Format: .jpg) of:

1) The completed pipemult2 schematic after Video #3
2) The Compilation Report after Video #4 showing Fmax and % utilization
3) The Assignment editor showing signal wren after Video #6
4) The Compilation Report at the end of Video #9 showing Fmax and % utilization

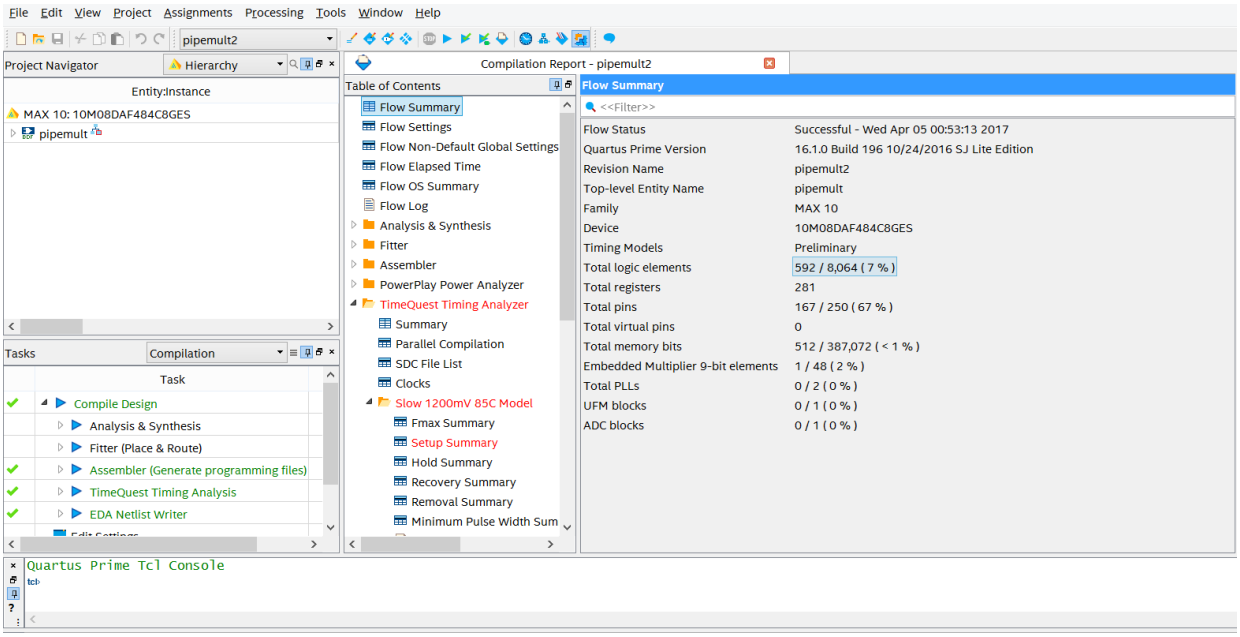
Solutions

Screenshots:

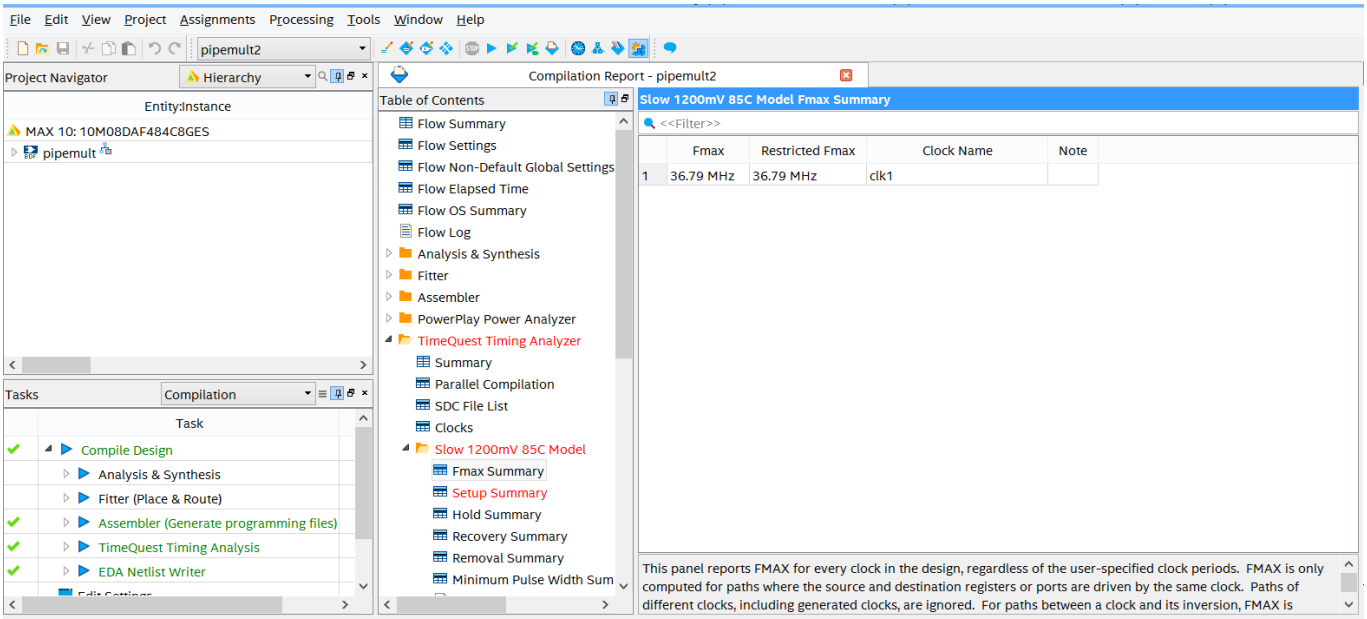
1)



2)

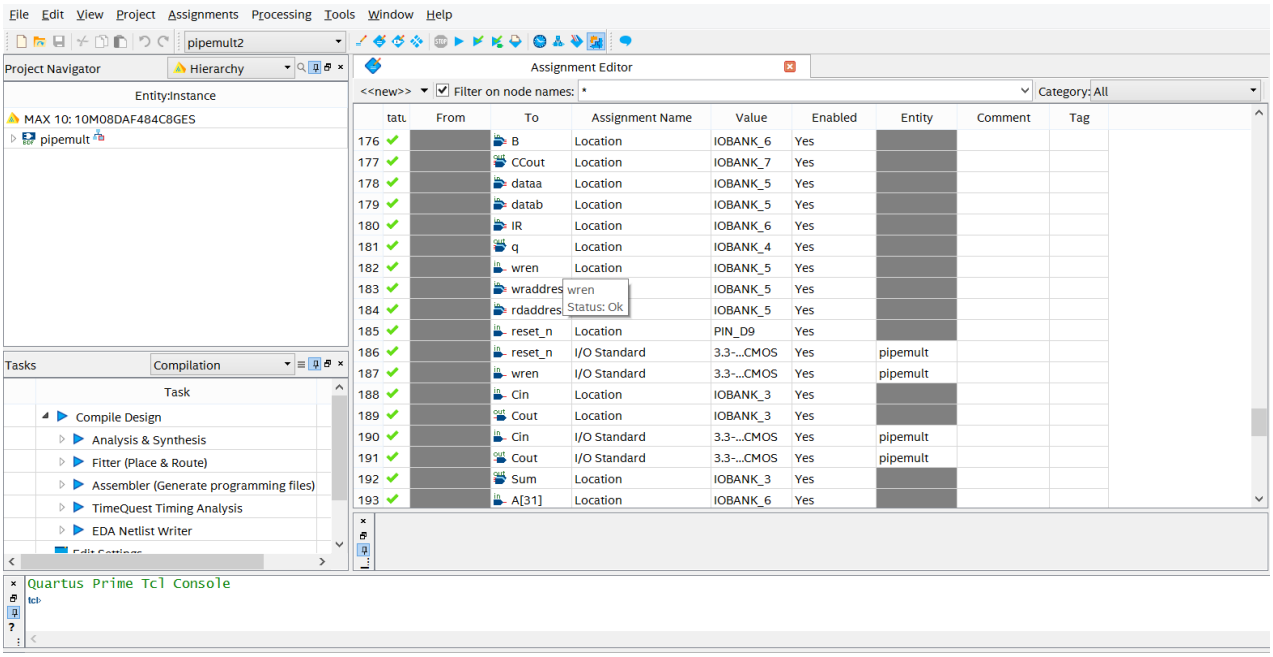


Utilization of logic elements is 7%. 5.5% to 8.5% is acceptable

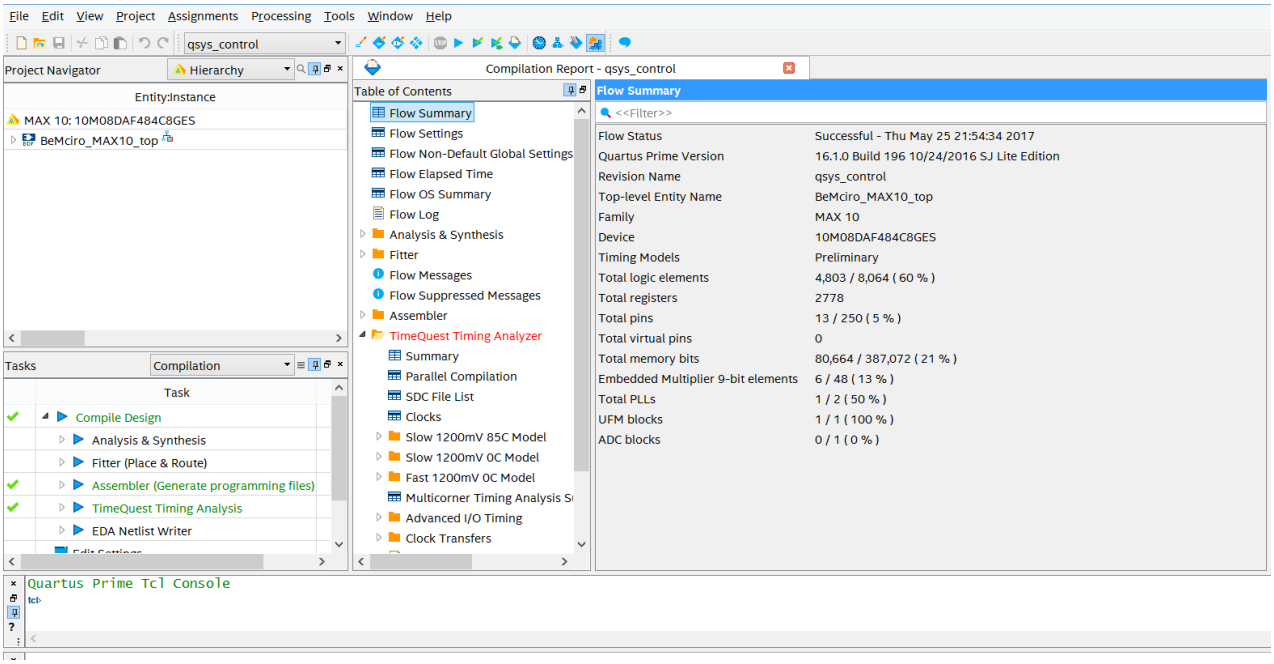


Fmax is 36.79 MHz, 29.43 to 44.15 MHz is acceptable

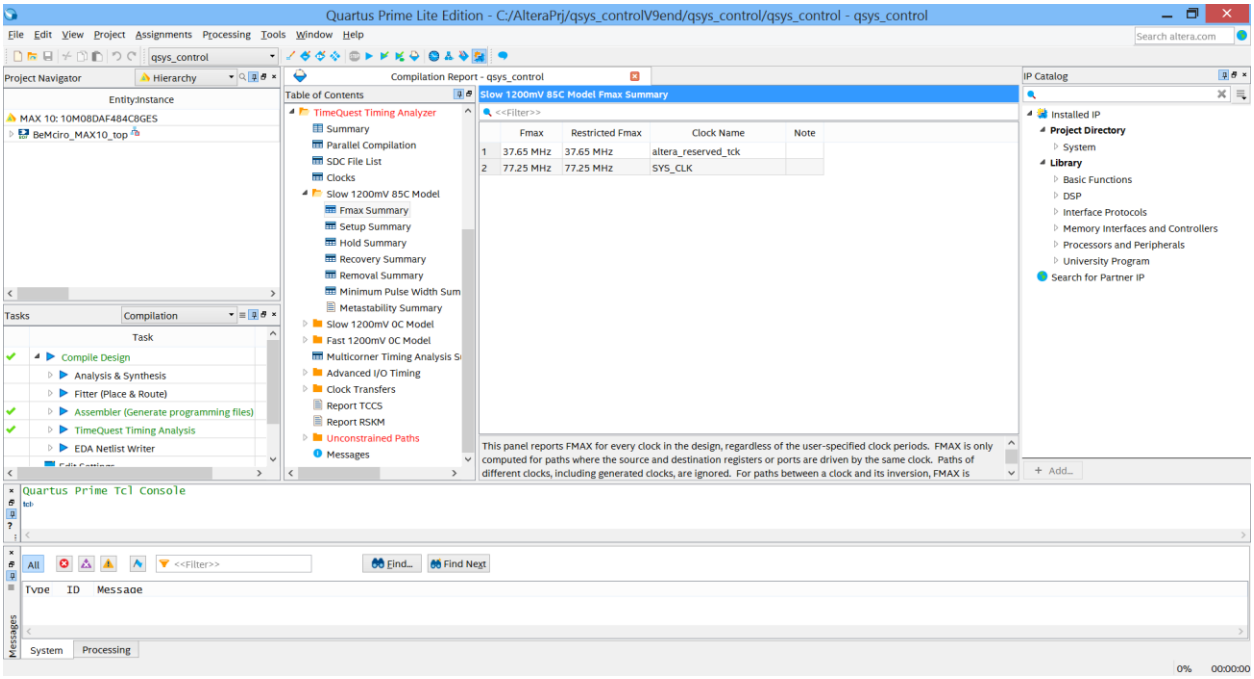
3)



4)



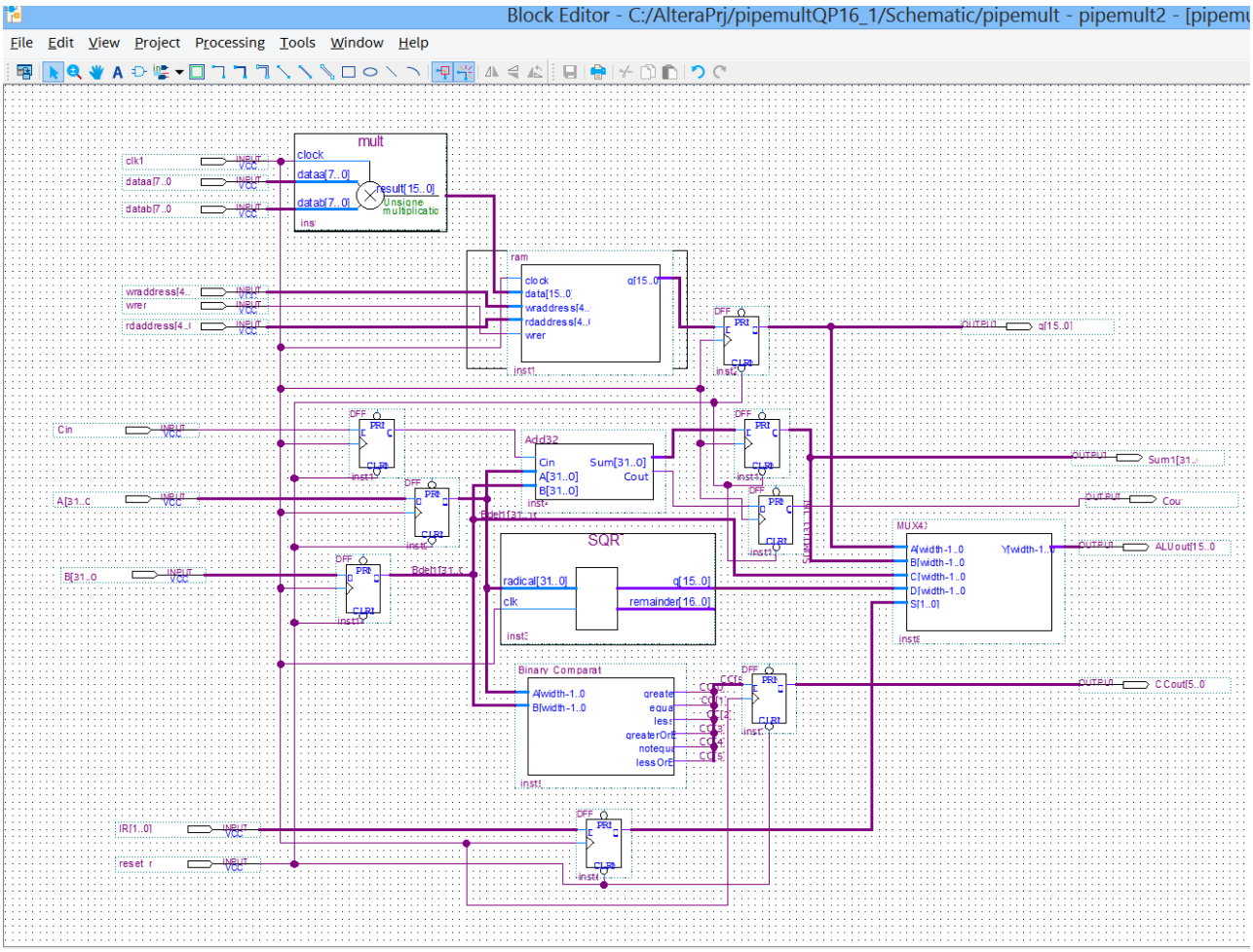
Utilization of logic elements is 60%. 48% to 72% acceptable.

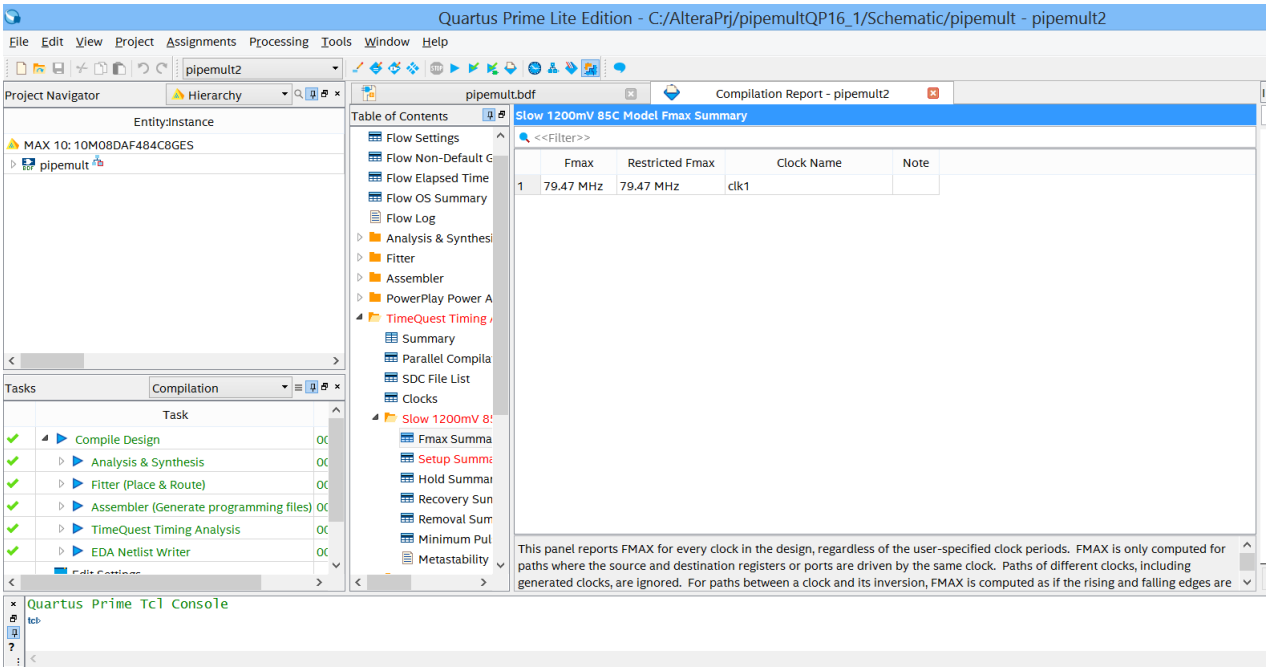


SYS_CLK Fmax is 77.25 MHz. 61.8 to 92.7 MHz is acceptable. This is before timing constraints are added (note the unconstrained paths in red). After constraining the design Fmax would likely be higher.

Design Question

1) **Add D-type registers to the input and output signals of the 32-bit adder in the pipemult2 circuit and compile the design. Submit a screenshot of your new schematic and the Compilation Report. Did your Fmax improve?**





Fmax is 79.47 MHz, 63 to 95 MHz is acceptable.

Yes, the Fmax improved, more than doubling, from 36.79 MHz to 79.47 MHz.