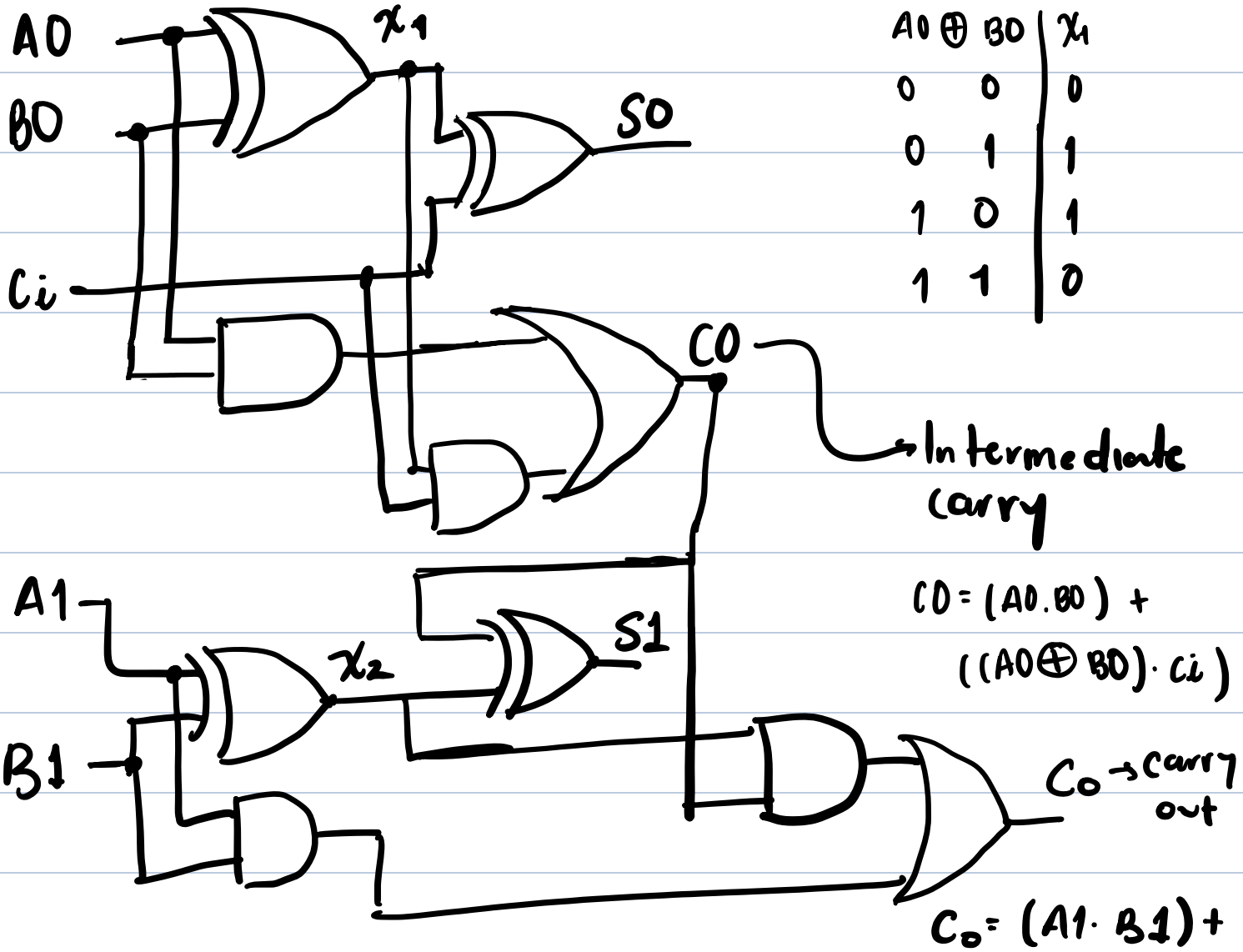
Week 1: Application Assignment

1 Design a 2-bit full Adder with carry

INPUTS					OUTPUTS		
A0	A1	B0	B1	Ci	S0	S1	Co
0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0
1	0	1	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	0	0	1	1	1	0
1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1



Xor

A0 ⊕ B0	X1
0 0	0
0 1	1
1 0	1
1 1	0

$C0 = (A0.B0) + ((A0 \oplus B0) \cdot Ci)$

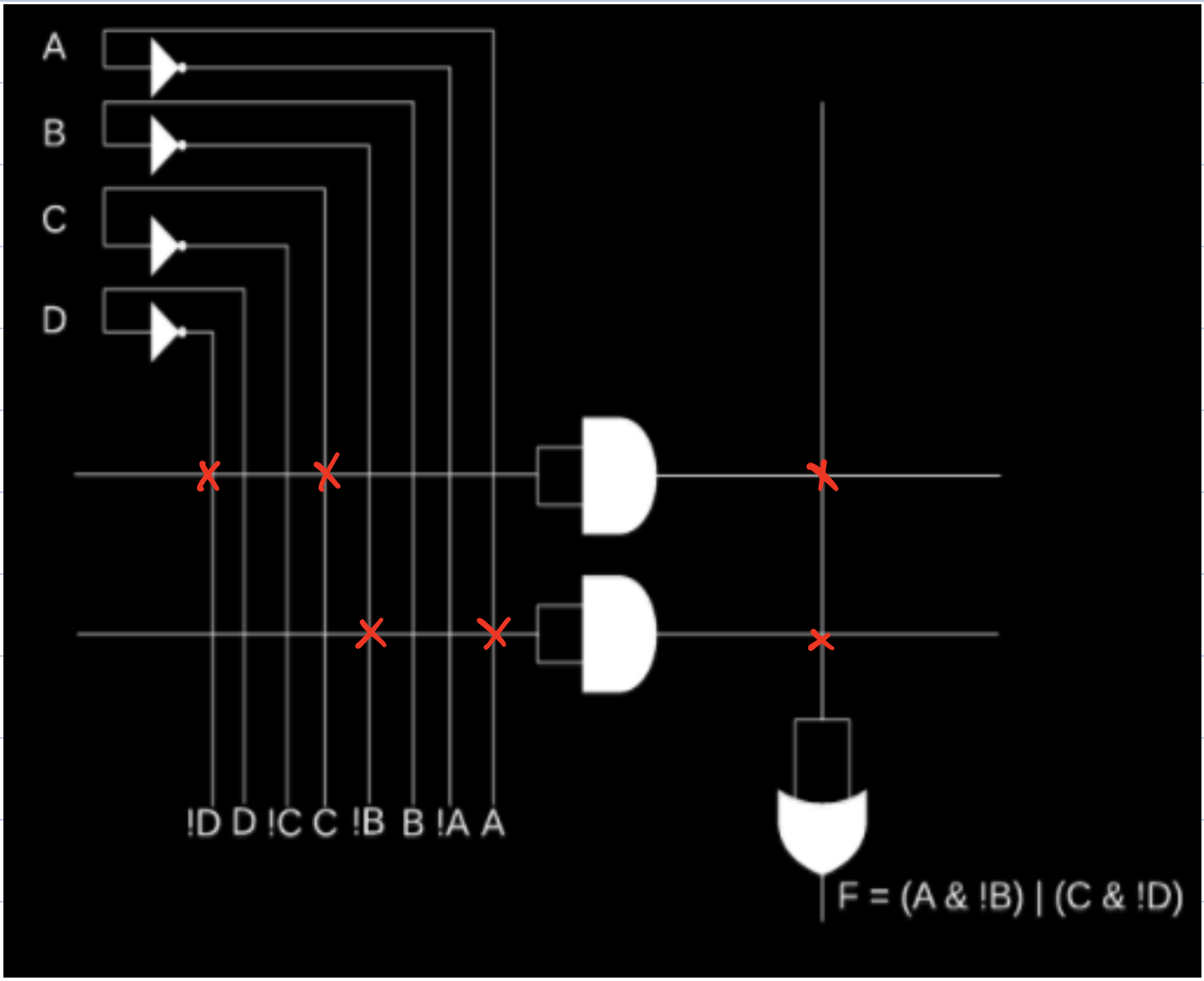
$C_o = (A1 \cdot B1) + (C0 \cdot (A1 \oplus B1))$

$S1 = A1 \oplus B1 \oplus C0$

$S0 = A0 \oplus B0 \oplus Ci$

2 $F = (A \& !B) | (C \& !D)$

①



(B) LUT

RAM CONTENTS				
Address				Output Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Explanation:

We have two options when the output is 1. First when the output (A & !B) is 1 OR when the output (C & !D). In case 1 is True when A is 1 and B is 0. In case 2 is true when C is 1 and D is 0.