

Week 4 Application Assignment:

Mission 007

Overview

The goal of this assignment is to extend your knowledge of schematic design using Quartus Prime by using pipelining and IP blocks to improve design performance. The student should be following the video instructions and creating the example as they go along. Their progress is checked at milestones by presenting screenshots which are matched to the solution screenshots to verify their work. Milestones checked are design schematic creation, timing improvement with pipelining, pin assignment, timing analysis and simulation.

This assignment is required. Peers must review 3 submissions to pass the assignment.

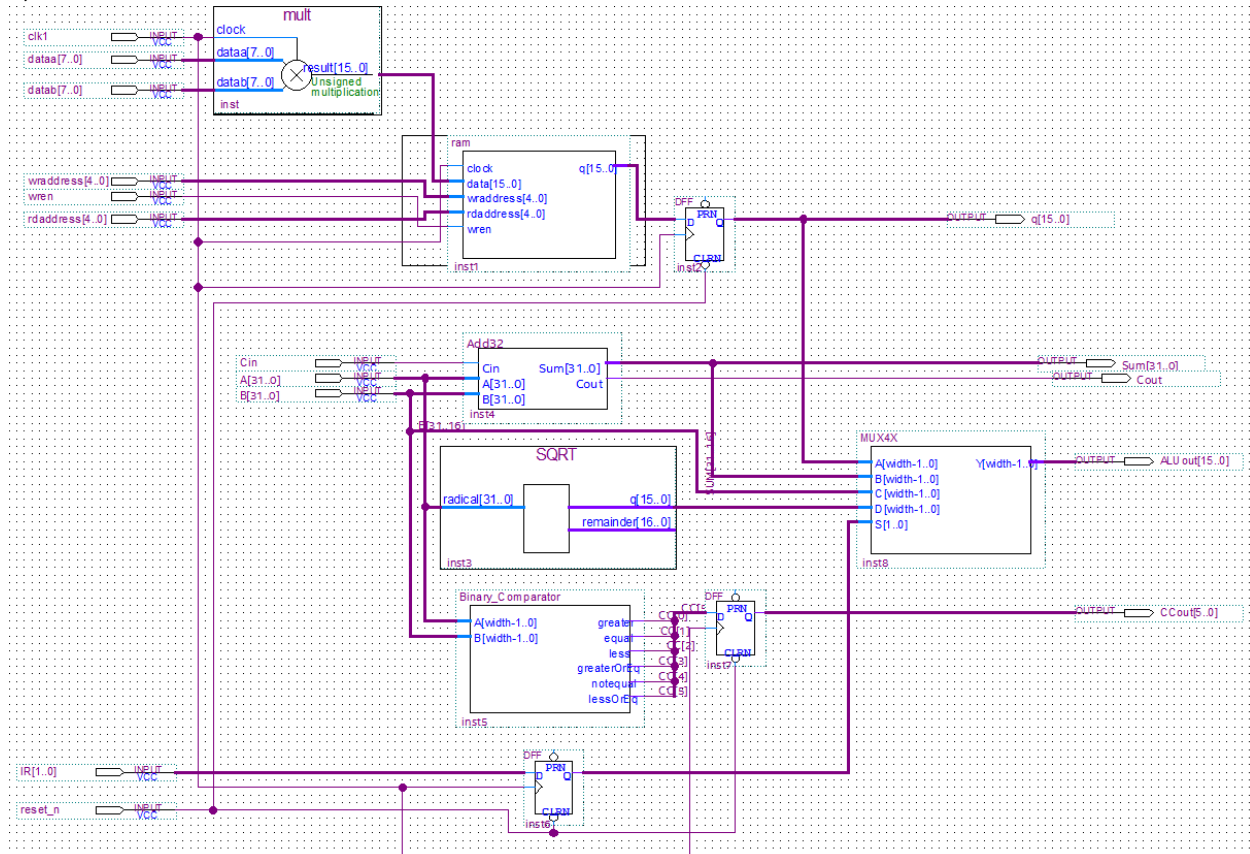
Submit screenshots (Format: .jpg) of:

- 1) The completed pipemult2 schematic after Video #3
- 2) The Compilation Report after Video #4 showing Fmax and % utilization
- 3) The Assignment editor showing signal wren after Video #6
- 4) The Compilation Report at the end of Video #9 showing Fmax and % utilization

Solutions

Screenshots:

1)



2)

Entity:Instance

MAX 10: 10M08DAF484C8GES

pipemult

Tasks

Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Quartus Prime Tcl Console

tcl

Compilation Report - pipemult2

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TimeQuest Timing Analyzer

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Slow 1200mV 85C Model

Fmax Summary

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Sum

Flow Summary

Flow Status

Successful - Wed Apr 05 00:53:13 2017

Quartus Prime Version

16.1.0 Build 196 10/24/2016 SJ Lite Edition

Revision Name

pipemult2

Top-level Entity Name

pipemult

Family

MAX 10

Device

10M08DAF484C8GES

Timing Models

Preliminary

Total logic elements

592 / 8,064 (7 %)

Total registers

281

Total pins

167 / 250 (67 %)

Total virtual pins

0

Total memory bits

512 / 387,072 (< 1 %)

Embedded Multiplier 9-bit elements

1 / 48 (2 %)

Total PLLs

0 / 2 (0 %)

UFM blocks

0 / 1 (0 %)

ADC blocks

0 / 1 (0 %)

Utilization of logic elements is 7%. 5.5% to 8.5% is acceptable

Entity:Instance

MAX 10: 10M08DAF484C8GES

pipemult

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Minimum Pulse Width Sum

Slow 1200mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	36.79 MHz	36.79 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is

Fmax is 36.79 MHz, 29.43 to 44.15 MHz is acceptable

3)

File Edit View Project Assignments Processing Tools Window Help

pipemult2

Project Navigator

EntityInstance

MAX 10: 10M08DAF484C8GES

pipemult

Tasks

Compilation

Task

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EDA Netlist Writer

Edit Settings

Assignment Editor

Filter on node names: *

Category: All

	tati	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
176	✓		B	Location	IOBANK_6	Yes			
177	✓		CCout	Location	IOBANK_7	Yes			
178	✓		dataa	Location	IOBANK_5	Yes			
179	✓		datab	Location	IOBANK_5	Yes			
180	✓		IR	Location	IOBANK_6	Yes			
181	✓		q	Location	IOBANK_4	Yes			
182	✓		wren	Location	IOBANK_5	Yes			
183	✓		wrddres	wren	IOBANK_5	Yes			
184	✓		rdaddress	Status: Ok	IOBANK_5	Yes			
185	✓		reset_n	Location	PIN_D9	Yes			
186	✓		reset_n	I/O Standard	3.3-...CMOS	Yes	pipemult		
187	✓		wren	I/O Standard	3.3-...CMOS	Yes	pipemult		
188	✓		Cin	Location	IOBANK_3	Yes			
189	✓		Cout	Location	IOBANK_3	Yes			
190	✓		Cin	I/O Standard	3.3-...CMOS	Yes	pipemult		
191	✓		Cout	I/O Standard	3.3-...CMOS	Yes	pipemult		
192	✓		Sum	Location	IOBANK_3	Yes			
193	✓		A[31]	Location	IOBANK_6	Yes			

Quartus Prime Tcl Console

4)

File Edit View Project Assignments Processing Tools Window Help

qsys_control

Project Navigator

EntityInstance

MAX 10: 10M08DAF484C8GES

BeMciro_MAX10_top

Tasks

Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Edit Settings

Compilation Report - qsys_control

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Flow Summary

Flow Status

Successful - Thu May 25 21:54:34 2017

Quartus Prime Version

16.1.0 Build 196 10/24/2016 SJ Lite Edition

Revision Name

qsys_control

Top-level Entity Name

BeMciro_MAX10_top

Family

MAX 10

Device

10M08DAF484C8GES

Timing Models

Preliminary

Total logic elements

4,803 / 8,064 (60 %)

Total registers

2778

Total pins

13 / 250 (5 %)

Total virtual pins

0

Total memory bits

80,664 / 387,072 (21 %)

Embedded Multiplier 9-bit elements

6 / 48 (13 %)

Total PLLs

1 / 2 (50 %)

UFM blocks

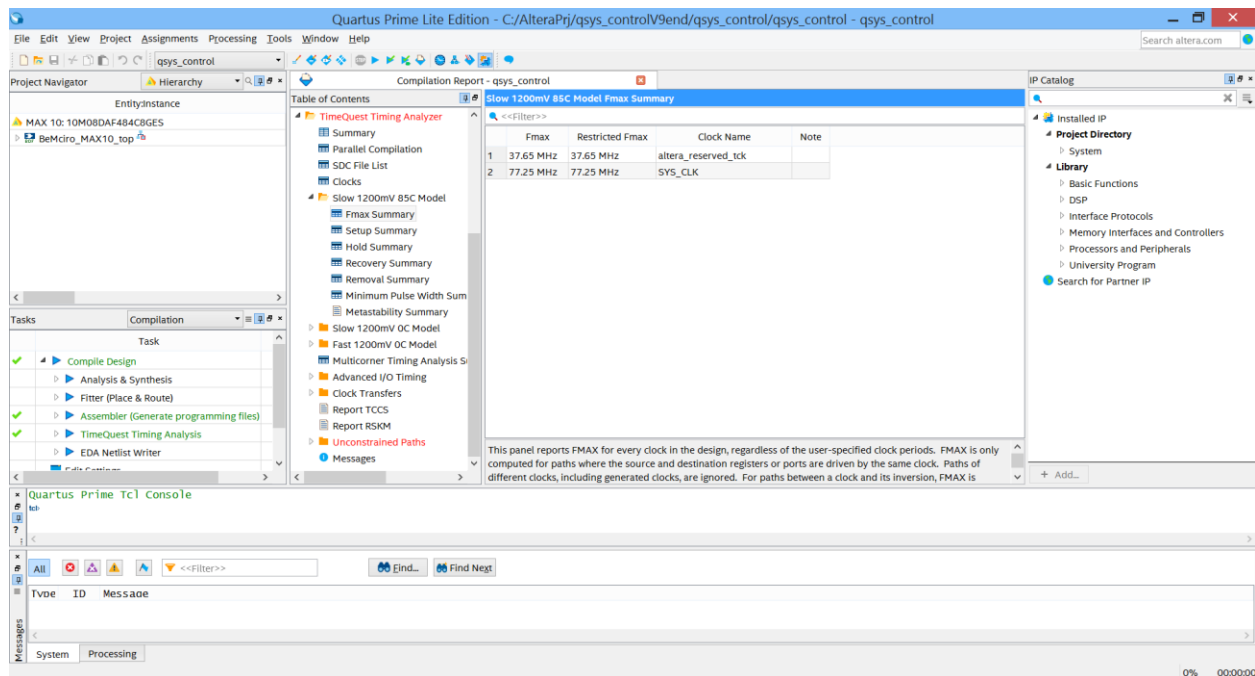
1 / 1 (100 %)

ADC blocks

0 / 1 (0 %)

Quartus Prime Tcl Console

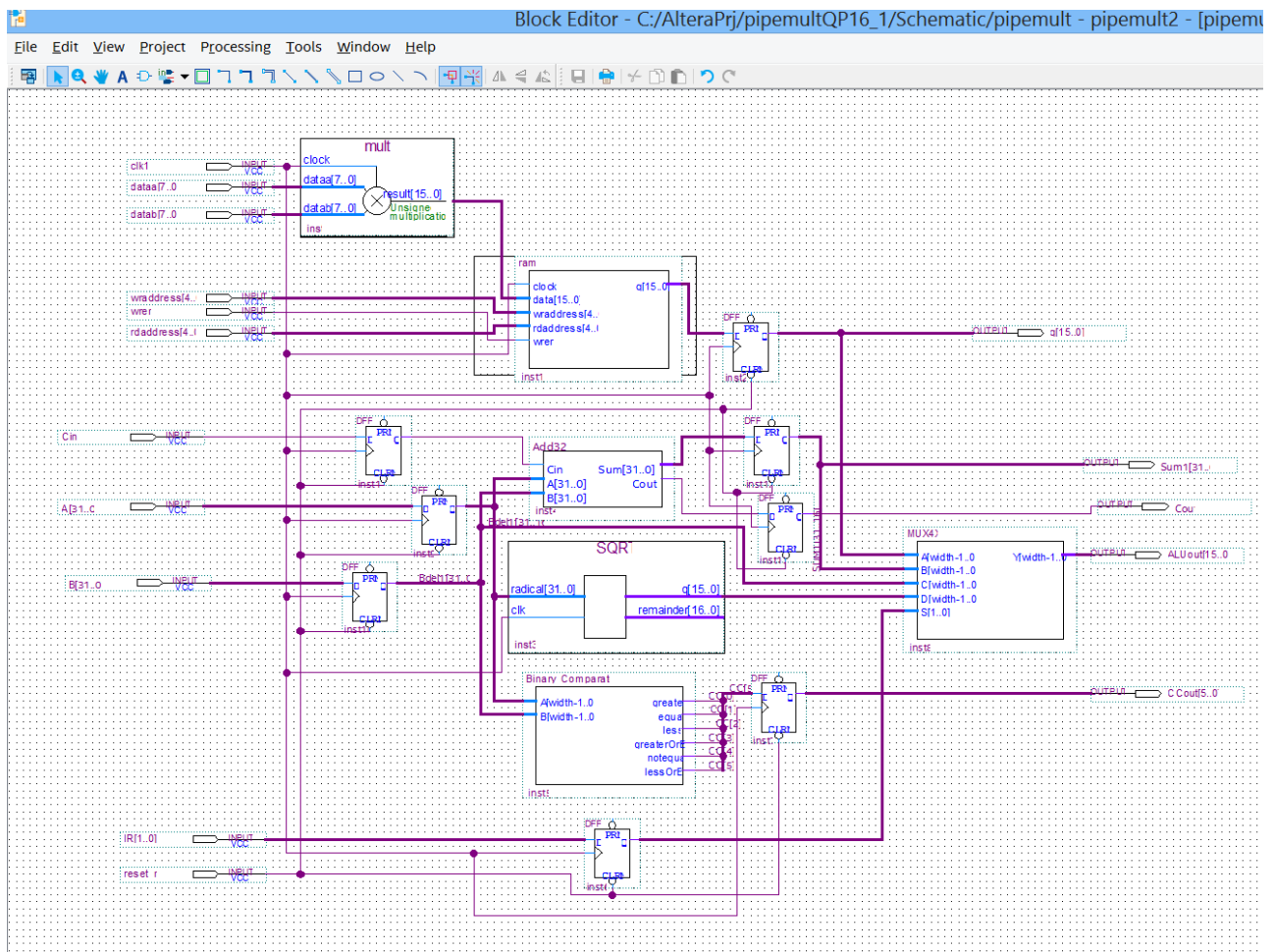
Utilization of logic elements is 60%. 48% to 72% acceptable.



SYS_CLK Fmax is 77.25 MHz. 61.8 to 92.7 MHz is acceptable. This is before timing constraints are added (note the unconstrained paths in red). After constraining the design Fmax would likely be higher.

Design Question

- 1) Add D-type registers to the input and output signals of the 32-bit adder in the pipemult2 circuit and compile the design. Submit a screenshot of your new schematic and the Compilation Report. Did your Fmax improve?



Quartus Prime Lite Edition - C:/AlteraPrj/pipemultQP16_1/Schematic/pipemult - pipemult2

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity/Instance

- MAX 10: 10M08DAF484C8GES
 - pipemult

Tasks

Compilation

Task	Status
Compile Design	OK
Analysis & Synthesis	OK
Fitter (Place & Route)	OK
Assembler (Generate programming files)	OK
TimeQuest Timing Analysis	OK
EDA Netlist Writer	OK

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- Fmax Summa
- Setup Summe
- Hold Summar
- Recovery Sun
- Removal Sum
- Minimum Pul
- Metastability

Slow 1200mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	79.47 MHz	79.47 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are

Quartus Prime Tcl Console

```
tcl>
```

Fmax is 79.47 MHz, 63 to 95 MHz is acceptable.

Yes, the Fmax improved, more than doubling, from 36.79 MHz to 79.47 MHz.