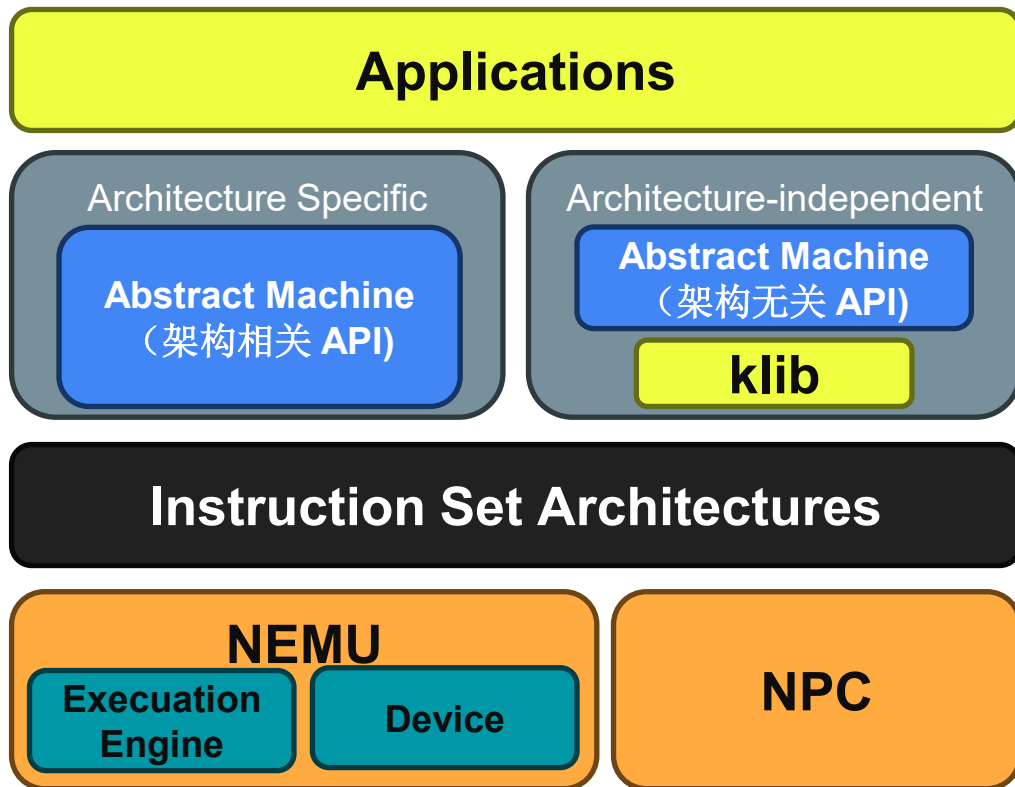# **Golden Apple Corelet**: a compact, in-order RISC-V microarchitecture optimized for embedded systems.

Shuao Jia

Beijing University of Posts and Telecommunications

Project Architecture Overview

Functional Simulator (NEMU)

- **The "Differential Testing" Mechanism.**
  - Instead of writing test cases, we compare processor's architectural state every cycle.
  - **DUT (Design Under Test):** My RISC-V Core (Verilator simulation).
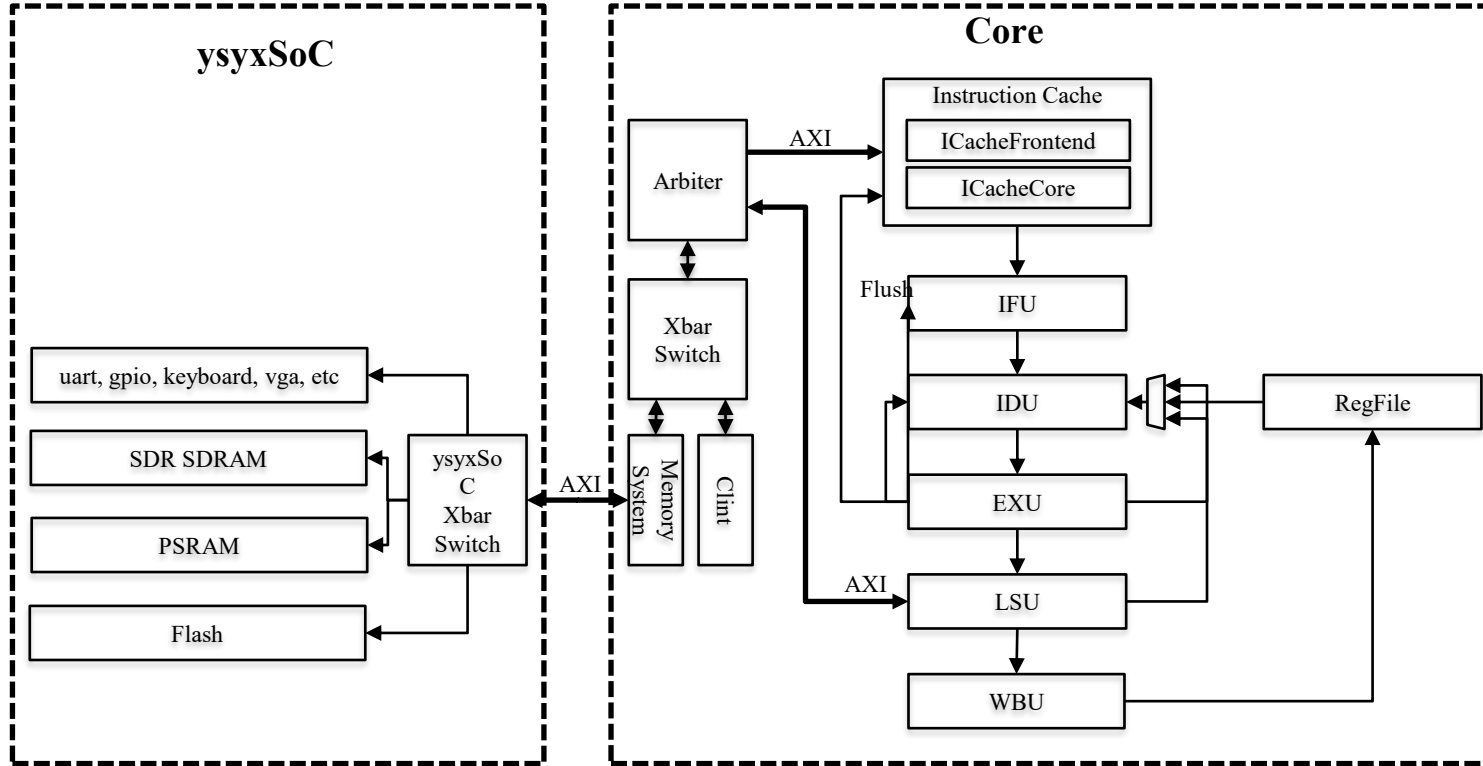 - **REF (Reference):** NEMU (C++ functional simulator).
- **Workflow:**
  1. Execute one instruction on both DUT and REF.
  2. Check for consistency in GPRs and PC.
  3. Abort immediately upon mismatch.
- **Result:**
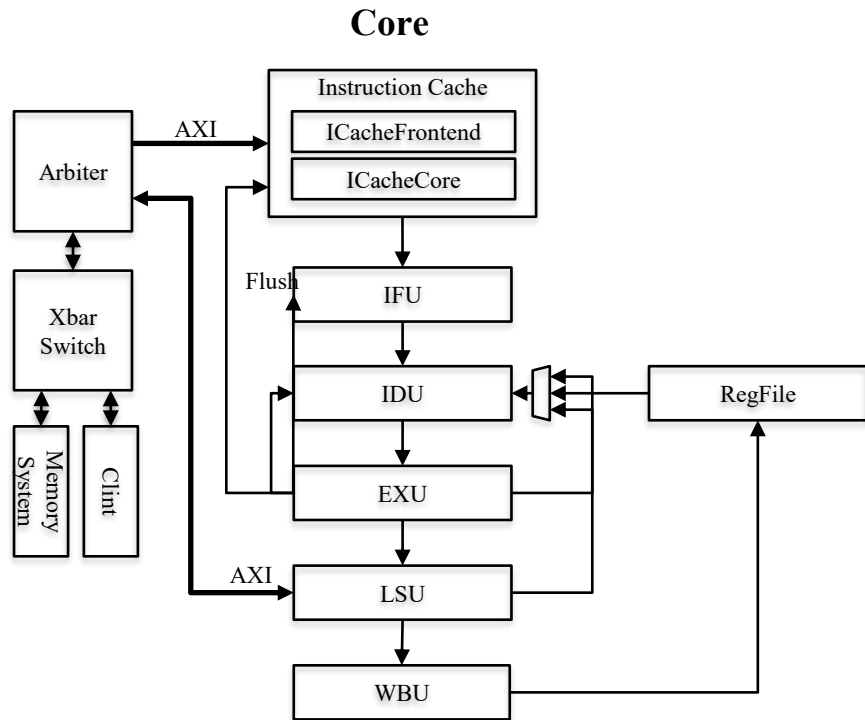 - Successfully identified logic errors.

Microarchitecture & System Integration

Core Microarchitecture: RV32E

2+5 Stage Pipeline Design

- **Instruction Fetch (2 Stages):** Decoupled fetch unit with dual-stage ICache for high throughput.
- **Execution (5 Stages):** Classic RISC pipeline with full bypassing and hazard detection.
- **Prediction:** Static branch prediction to reduce control hazards.

Core

Agile Development

Chisel3

Constructed hardware using Scala-based generator language for parameterized and reusable modules.

Verilator

High-speed cycle-accurate simulation for rapid iteration and regression testing.

Yosys + iSTA

Utilized open-source synthesis and timing analysis flows to ensure physical realizability.

System Bring-up: RT-Thread

- **Booting a real-time operating system is the ultimate stress test for architectural correctness.**
    - Implemented CSR (Control and Status Registers) for exception handling.
    - Handled timer interrupts and context switching.
    - Successfully entered the interactive shell of RT-Thread.
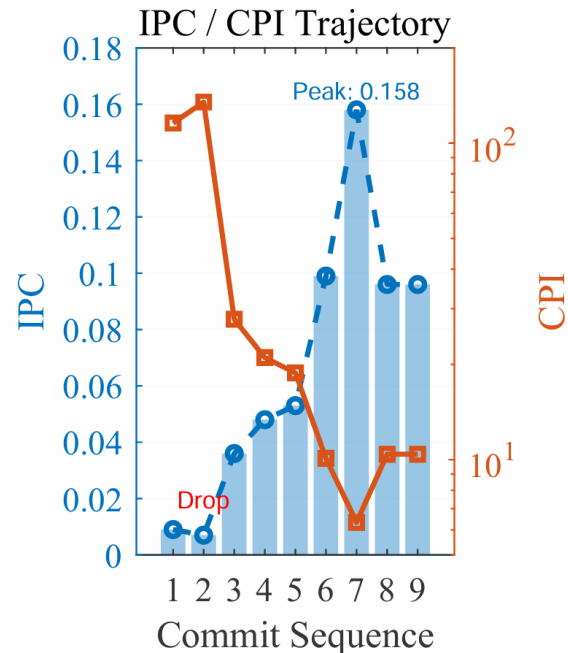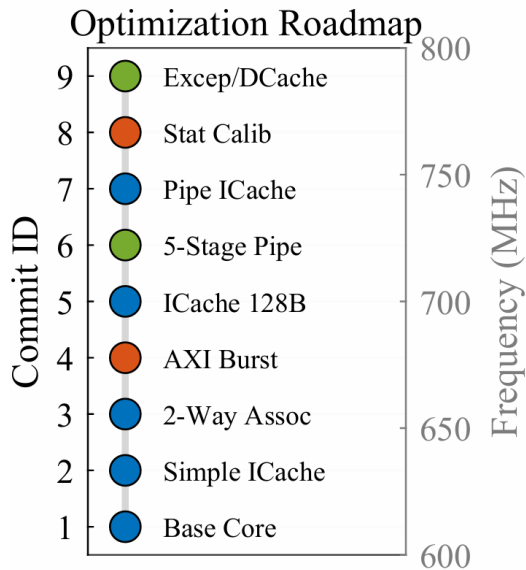

Boot

Performance Evaluation: Microarchitectural Evolution

- **IPC Trajectory:**
  - Significant improvement from Base Core (0.02) to Peak (0.158).
- **Bottleneck Shift:**
  - *Phase 1:* Memory Bound (84.6%)
  - *Phase 2:* Fetch Bound (64.8%)
  - *Final:* IDU Stall Bound

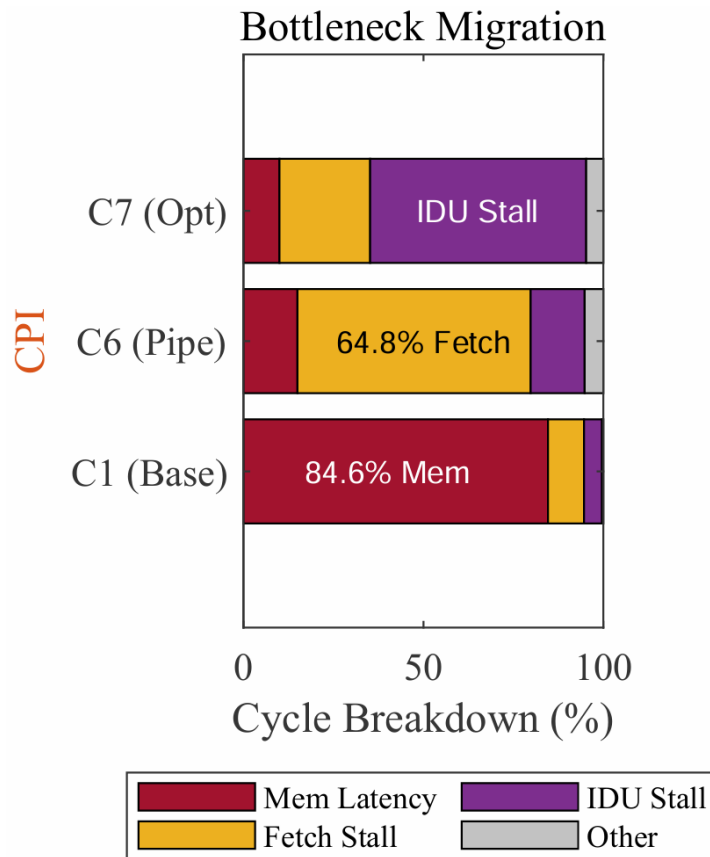# Performance Evaluation: Microarchitectural Evolution

Iterative optimization process tracking IPC growth and bottleneck migration.

- **IPC Trajectory:**
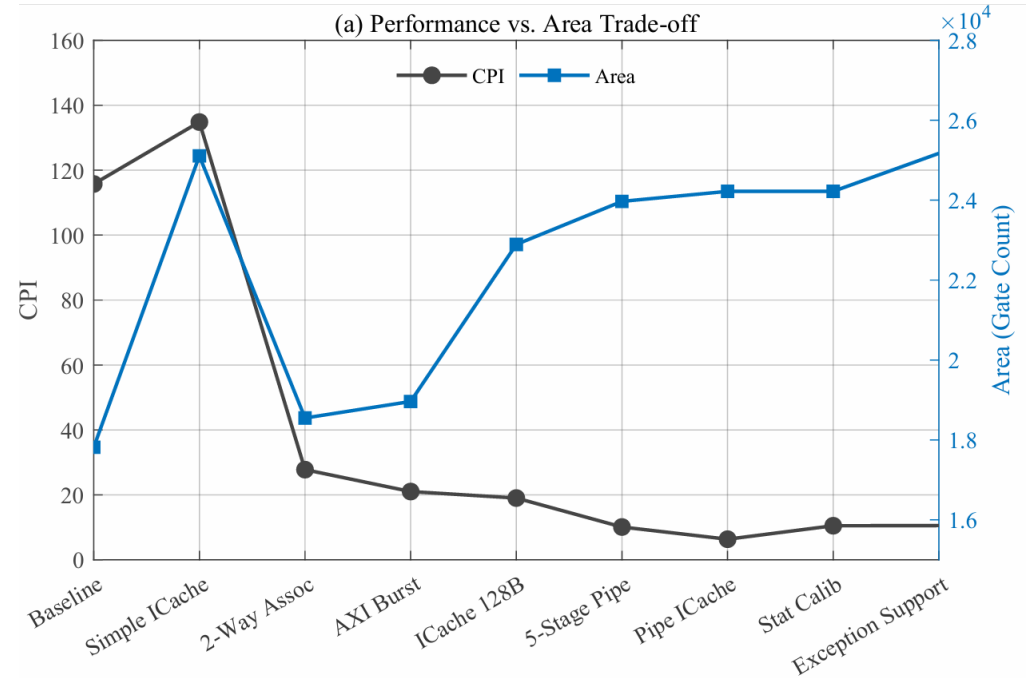 - Significant improvement from Base Core (0.02) to Peak (0.158).
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  - *Phase 1:* Memory Bound (84.6%)
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  - *Final:* IDU Stall Bound

Bottleneck Migration

Performance Evaluation: Optimization Results

- **Performance vs. Area:** Gate count increased linearly while CPI dropped exponentially, validating the efficiency of complex structures.
- **Final Speedup:** Achieved an 11.0x total speedup over the baseline implementation.
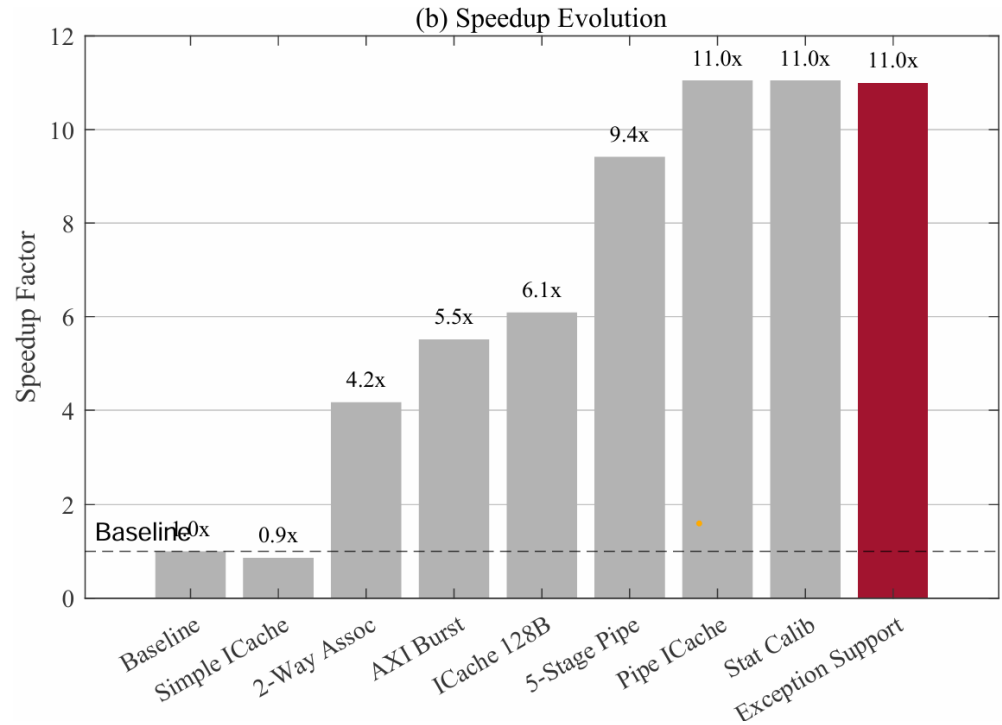

(a) Performance vs. Area Trade-off

Performance Evaluation: Optimization Results

- **Performance vs. Area:**
  Gate count increased linearly while CPI dropped exponentially, validating the efficiency of complex structures.
- **Final Speedup:** Achieved an 11.0x total speedup over the baseline implementation.

(b) Speedup Evolution

Summary & Future Work

Achievements

- ✓ Designed 2+5-stage RISC-V Core
- ✓ Integrated SoC & Booted OS
- ✓ Passed Stage C Review

Tape-out Target

Advance from Stage C to Stage B to complete full chip tape-out verification and silicon validation.

Advanced Architecture

Participate in the NSCSCC (全国计算机系统能力大赛) to explore Out-of-Order (OoO) execution and dynamic scheduling.