Assignment – Caches

due date: June 11st 9:00am

1. [30 points]

A small 16-bit address space special-purpose processor may be equipped with one of two tiny direct-mapped caches, C1 or C2, each of which has a total capacity of 64 bytes. C1 has a blocksize of 4 bytes (which corresponds to the size of an integer on this system) while C2 has a blocksize of 16 bytes.

(a) What are the cache parameters (m, C, B, E, S, t, s, b) for C1 and C2?

(b) Consider that the following sequence of addresses are read, (where the size of the data path equals the blocksize): BA00, BA04, AA08, BA05, AA14, AA11, AA13, AA38, AA09, AA0B, BA04, AA2B, BA05, BA06, AA09, AA11.

For each cache option, specify which references are hits and which are misses, and show the final data content of the cache.

2. [25 points]

Given a cache with parameters little m = 32, little b = 8, little s = 8 and E = 4.

Assume that:

sizeof(element)	= 8 bytes
@x[256]	= AAAA0000
@y[256]	= AABB0000
@a[512]	= AAAA8000
@b[512]	= AABB8000
value1 and value2 are in registers	

Use the code segment:

```
for i = 0 to 255
    value1 = x[ i ] × y[ i ]
    for j = 0 to 1
        value2 = a[ i×2+j ] + b[ i×2+j ]
```

(a) Fully describe the cache in terms of the cache parameters discussed in class.

(b) What is the hit rate for each of x, y, a and b?

(c) What is the overall hit rate?

(d) What are the cache contents after 1 iteration of the " i " loop?

(e) What are the cache contents after the completion of the " i " loop?

3. [20 points]

Given an LRU cache with parameters little m = 32, b = 8, little s = 0 and E = 256.

Assume that:

sizeof(element)	= 8 bytes
@x[8192]	= AAAA0000
@y[8192]	= AAAB0000
value is in a register	

Use the code segment:

```
for i = 0 to 8191
    value = x[ i ] + y[ i ]
```

(a) Fully describe the cache in terms of the cache parameters discussed in class.

(b) What is the hit rate for each of x, and y?

(c) What is the overall hit rate?

(d) What are the cache contents after the completion of the "i" loop?

4. [25 points]

Which of the following cache hierarchies will provide better AMAT?

Hierarchy A	hit time (cycles)	hit rate
L1 cache	2	25%
L2 cache	10	80%
L3 cache	80	95%
Main memory	500	

Hierarchy B	hit time (cycles)	hit rate
L1 cache	2	50%
L2 cache	5	65%
L3 cache	20	80%
Main memory	500	