LoRA-RL: Low-Rank Adaptation Enables Fast, Transferable Reinforcement Learning for Analog Circuit Optimization

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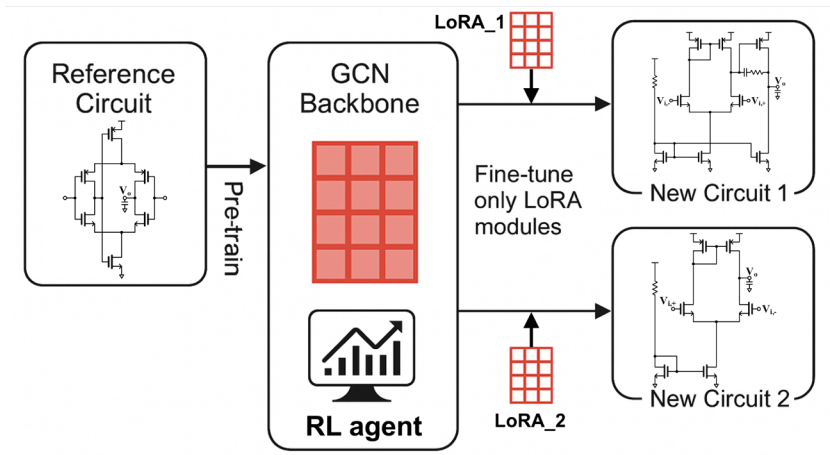

Fig. 1 Overview of proposed architecture

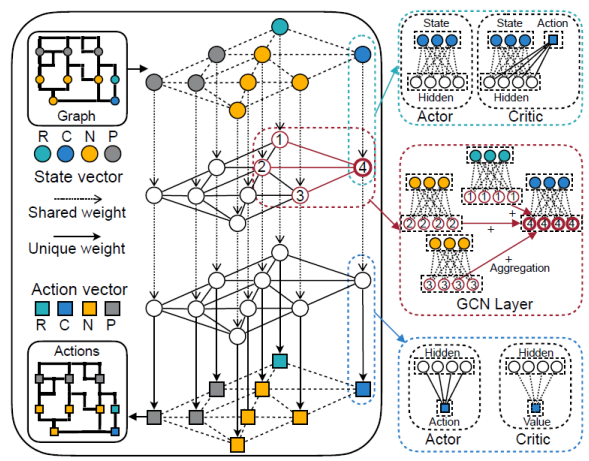

Fig. 2 GCN backbone from Ref.

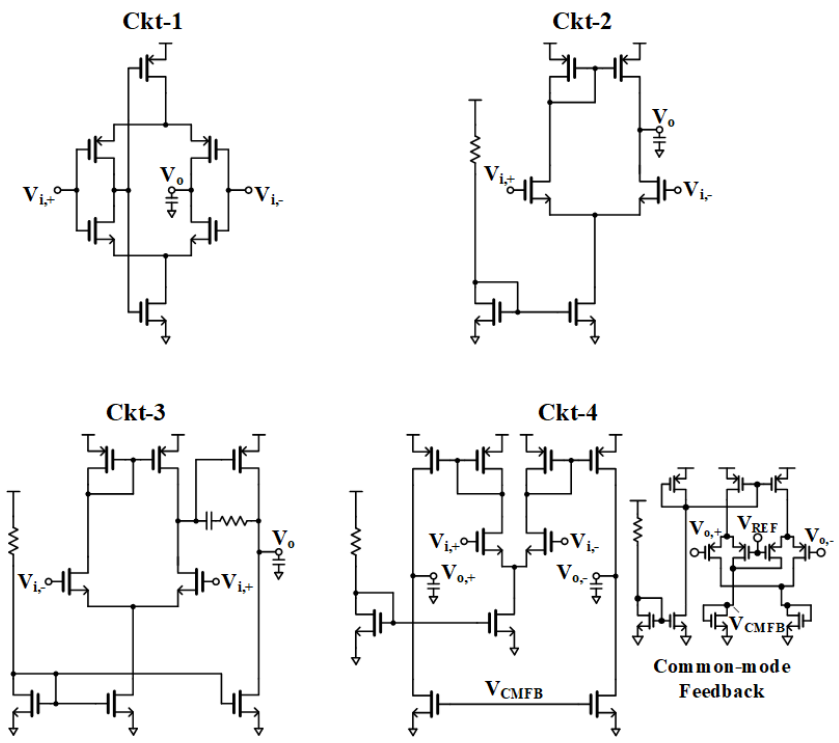

Fig. 3 Test amplifiers A–D in TSMC 45 nm.

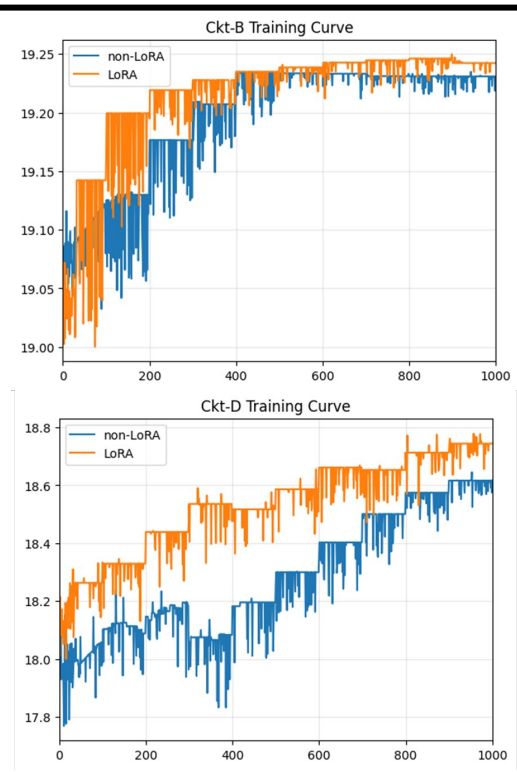

Fig. 4 Episode-wise FoM curves

Problem. Analog-transistor sizing needs senior know-how and → weeks of SPICE. Each new process node or new circuit repeats the pain.

Method. Pre-train a GCN-RL backbone on a reference amp; freeze it; fine-tune only

Rank-4 LoRA When moving to a new amplifier or a different process node. (~3% of total weights)

Benefit

✓ **Pre-train once, transfer efficiently**
✓ Only 3 % of weights updated;
✓ Fast converge 1~4x, FoM improves ~1.5 %
✓ LoRA stabilises gradients, preserves priors
✓ **Easily adapts to new process nodes** without retraining from scratch

Limitation & Future

✗ Schematic-level; no layout RC
✗ Reward uses AC/DC only; no transient response
→ Next: post-layout sizing & **PVT and mismatch tolerant design**