



















Design Rules Verification ReportFilename: D:\FishWand\PCB\FishWandTip\FishWantTip\FishWantTip.CSPcbDoc

Warnings 0 Rule Violations 0

| Warnings | |
|----------|---|
| Total | 0 |

| Rule Violations | |
|----------------------------------------------------------------------------------------------------------|---|
| Clearance Constraint (Gap=0.2mm) (All),(All) | 0 |
| Width Constraint (Min=0.2mm) (Max=1816.048mm) (Preferred=0.2mm) (All) | 0 |
| Power Plane Connect Rule(Direct Connect)(Expansion=0.102mm) (Conductor Width=0.102mm) (Air Gap=0.102mm) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint ((All)) | 0 |
| Minimum Annular Ring (Minimum=0.15mm) (All) | 0 |
| Hole Size Constraint (Min=0.2mm) (Max=6.3mm) (All) | 0 |
| Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All) | 0 |
| Hole To Hole Clearance (Gap=0.25mm) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=0.2mm) (All),(All) | 0 |
| Silk To Solder Mask (Clearance=0.127mm) (IsPad),(All) | 0 |
| Silk to Silk (Clearance=0.1mm) (All),(All) | 0 |
| Silk primitive without silk layer | 0 |
| Unpoured Polygon (Allow unpoured: False) | 0 |
| Unpoured Polygon (Allow unpoured: False) | 0 |
| Total | 0 |

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