

EXP_4 : ALU

We have to derive Arithmetic Logic Unit using Behavioral type of modelling . ALU performs 4 actions based on given select line namely

- a) Concatenate A & B.
- b) Add A & B .
- c) Perform bitwise XOR of A & B.
- d) Multiply A by 2.

The logic for ALU is given below :-

- ① If select lines are 00, we have to ~~add~~ concatenate A & B. Which done by simply A & B.
- ② If $s_{150} = '01'$; we have to give output as $A + B$. We ~~can~~ need to behavioral design, so we will use a for loop with 2 variables sum and carry.
Sum is 8-bit = {00000000}.
& carry is 1-bit = {0}.
In each iteration,
 $sum[i] = (A[i] \text{ xor } B[i] \text{ xor } carry)$
Sum[i] will be '1' if any 1 or ~~any~~ all 3 of them will be '1'.
 $carry = A[i] \cdot B[i] + carry \cdot (A[i] + B[i])$
After for loop, we will get sum vector upto 4 bits, and the 5th bit will be the remaining carry.
- ③ If $s_{150} = '10' \Rightarrow Y = A \text{ xor } B$.
- ④ If $s_{150} = '11' \Rightarrow Y = '000' \& 'A \& '0'$
& \Rightarrow concatenate operation.

TRACE file format :-

INPUT MSB = S1

INPUT LSB = B0

OUTPUT MSB = Y7

OUTPUT LSB = Y0

TRACEFILE format

<S1 S0 A3 A2 A1 A0 B3 B2 B1 B0> <Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0>

Tstcases from TRACEFILE

```
000000000 00000000 11111111
0000000001 00000001 11111111
0000000010 00000010 11111111
0000000011 00000011 11111111
0000000100 00000100 11111111
0000000101 00000101 11111111
0000000110 00000110 11111111
0000000111 00000111 11111111
0000001000 00001000 11111111
0000001001 00001001 11111111
0000001010 00001010 11111111
0000001011 00001011 11111111
0000001100 00001100 11111111
0000001101 00001101 11111111
0000001110 00001110 11111111
0000001111 00001111 11111111
0000010000 00010000 11111111
0000010001 00010001 11111111
0000010010 00010010 11111111
0000010011 00010011 11111111
0000010100 00010100 11111111
0000010101 00010101 11111111
0000010110 00010110 11111111
0000010111 00010111 11111111
0000011000 00011000 11111111
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0000011010 00011010 11111111
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0000011100 00011100 11111111
0000011101 00011101 11111111
0000011110 00011110 11111111
0000011111 00011111 11111111
0000100000 00100000 11111111
0000100001 00100001 11111111
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0000101001 00101001 11111111
0000101010 00101010 11111111
0000101011 00101011 11111111
0000101100 00101100 11111111
0000101101 00101101 11111111
0000101110 00101110 11111111
0000101111 00101111 11111111
0000110000 00110000 11111111
0000110001 00110001 11111111
```

VHDL description of ALU :-

```
entity alu_beh is
  generic(
    operand_width : integer:=4;
    sel_line : integer:=2
  );
  port (
    A: in std_logic_vector(operand_width-1 downto 0);
    B: in std_logic_vector(operand_width-1 downto 0);
    sel: in std_logic_vector(sel_line-1 downto 0);
    Y: out std_logic_vector((operand_width*2)-1 downto 0)
  );
end alu_beh;
architecture a1 of alu_beh is
```

```

function add(A: in std_logic_vector(operand_width-1 downto 0); B: in std_logic_vector(operand_width-1 downto 0))
return std_logic_vector is
    variable sum : std_logic_vector(7 downto 0) := (others => '0');
    variable carry : std_logic := '0';

begin
    bitwise_add : for i in 0 to 3 loop
        sum(i) := (A(i) xor B(i) xor carry );
        carry := ((A(i) and B(i)) or (carry and (A(i) or B(i))));
    end loop bitwise_add;
    sum(4) := carry or sum(4);

    return sum;
end add;

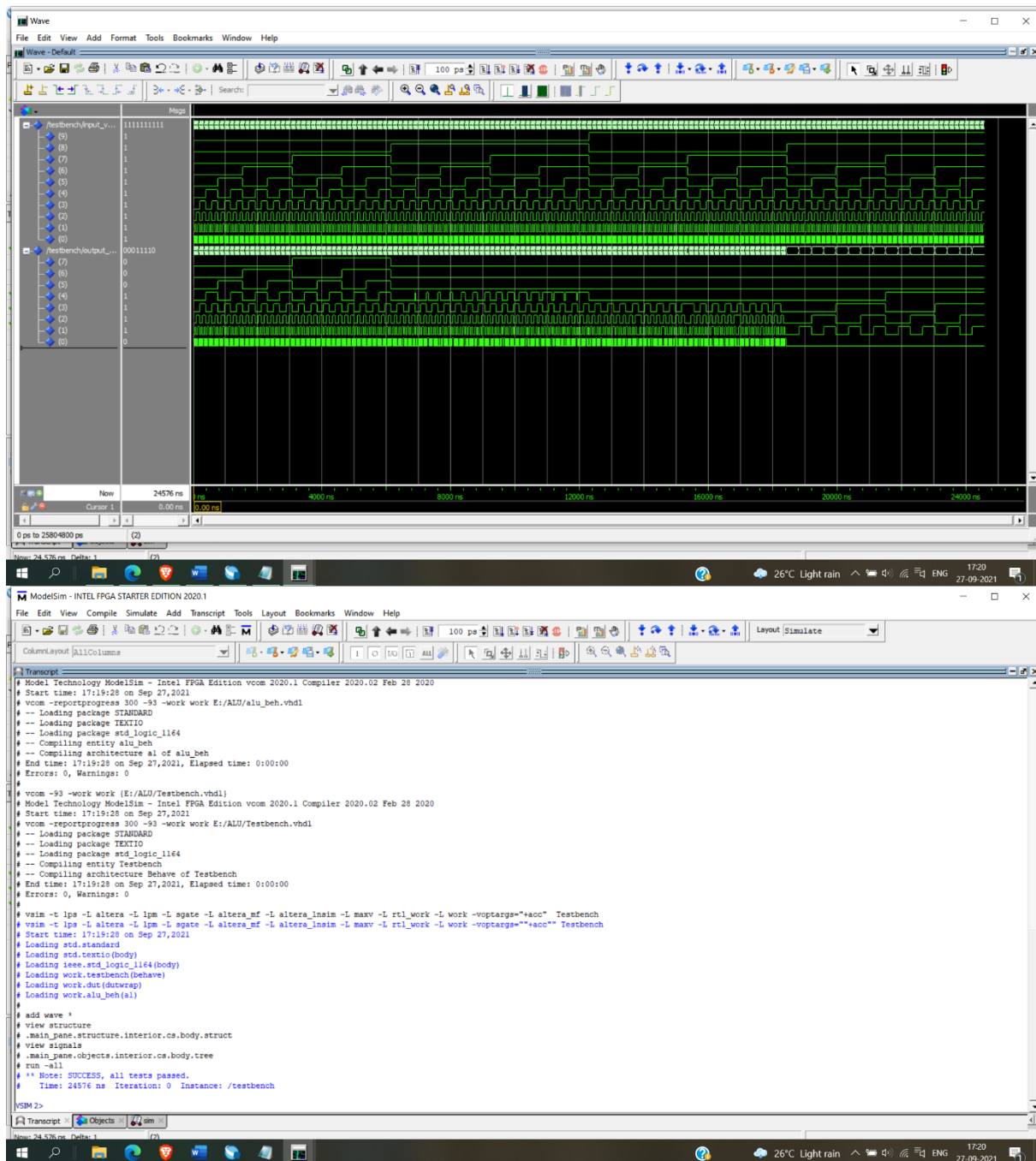
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```

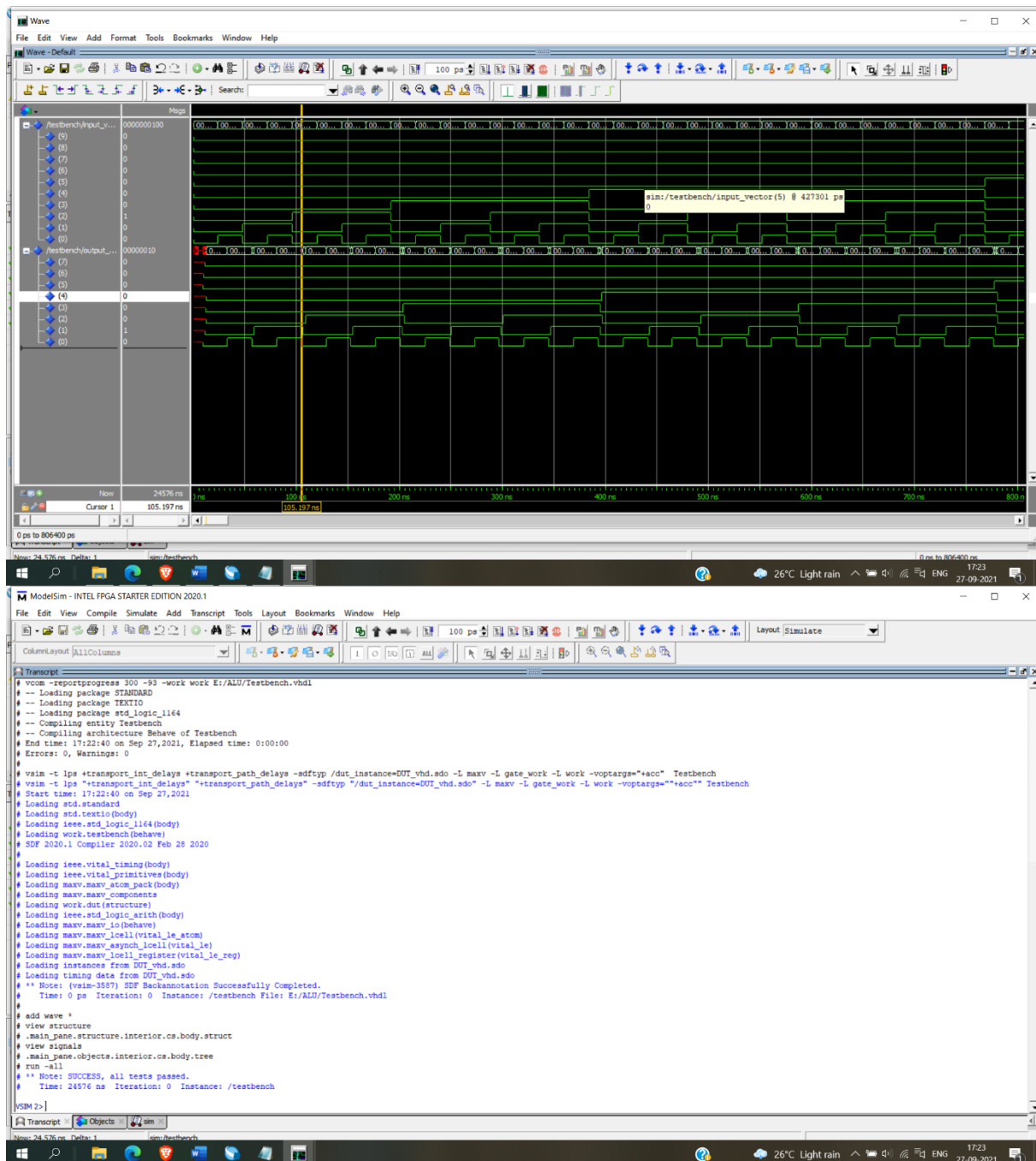
begin
alu : process( A, B, sel )
    variable temp : std_logic_vector(7 downto 0) := (others => '0');
begin
    if (sel(0)='0') and (sel(1)='0') then
        Y <= A & B ;
    elsif (sel(0)='1') and (sel(1)='0') then
        Y <= add(A,B);
    elsif (sel(0)='0') and (sel(1)='1') then
        for i in 0 to 3 loop
            temp(i) := (A(i) xor B(i));
        end loop;
        Y <= temp;
    else
        Y <= "000"&A&"0" ;
    end if;
end if;

```

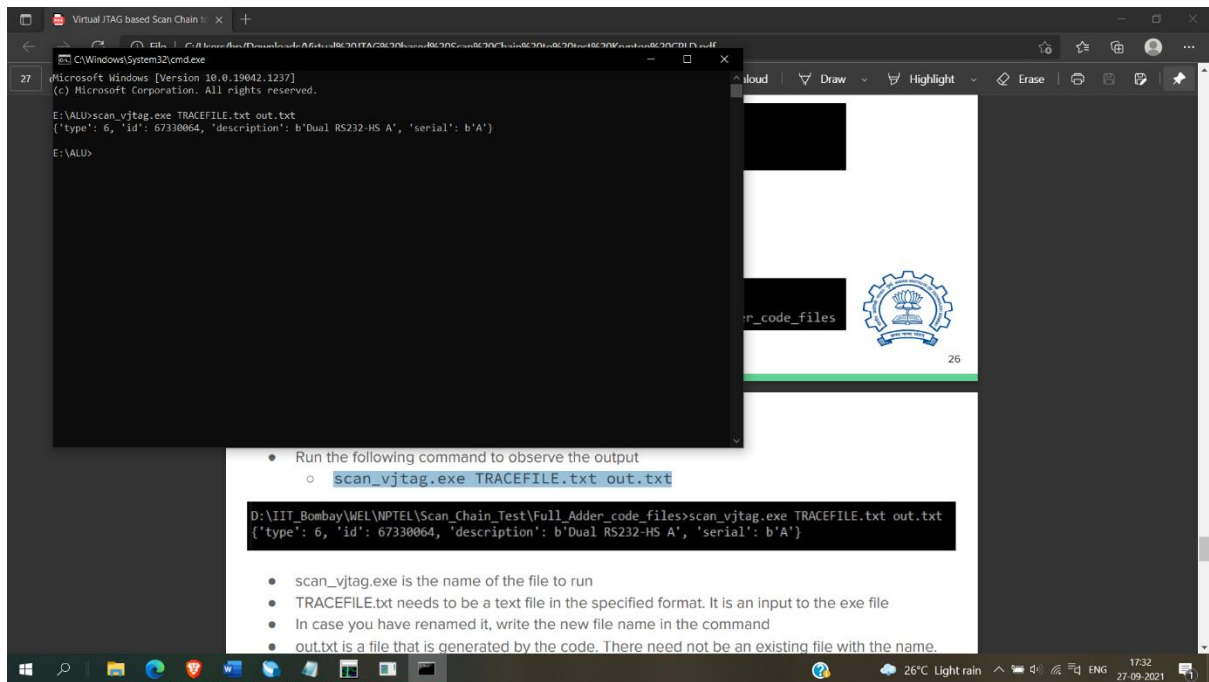
RTL Simulation :-



GATE level Simulation :-



SCANCHAIN testing:-



OUT.txt file generated :-

0000000000 00000000 Success

000000001 0000001 Success
000000010 0000010 Success
000000011 0000011 Success
000000100 0000100 Success
000000101 0000101 Success
000000110 0000110 Success
000000111 0000111 Success
000001000 0001000 Success
000001001 0001001 Success
000001010 0001010 Success
000001011 0001011 Success
000001100 0001100 Success
000001101 0001101 Success
000001110 0001110 Success
000001111 0001111 Success
000010000 0010000 Success
000010001 0010001 Success
000010010 0010010 Success
000010011 0010011 Success
000010100 0010100 Success
000010101 0010101 Success
000010110 0010110 Success
000010111 0010111 Success
000011000 0011000 Success
000011001 0011001 Success
000011010 0011010 Success
000011011 0011011 Success
000011100 0011100 Success
000011101 0011101 Success
000011110 0011110 Success
000011111 0011111 Success
000100000 0100000 Success
000100001 0100001 Success
000100010 0100010 Success
000100011 0100011 Success
000100100 0100100 Success
000100101 0100101 Success
000100110 0100110 Success
000100111 0100111 Success
000101000 0101000 Success
000101001 0101001 Success
000101010 0101010 Success
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000101101 0101101 Success
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0010000010 10000010 Success
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0111100001 00001111 Success
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