Lab03 Report

312510139 吳彧嘉

1. Block Diagram
   - Datapath & Control signals

     首先按照 workbook 提供的下圖，來完成下圖的 Testbench。

     其中：

     (1) reset_task 負責 reset 訊號

     (2) load_input_task 負責從 txt 檔案讀取測資

     (3) check_idle_task 負責檢查 design 的 ap_idle 是否為 1

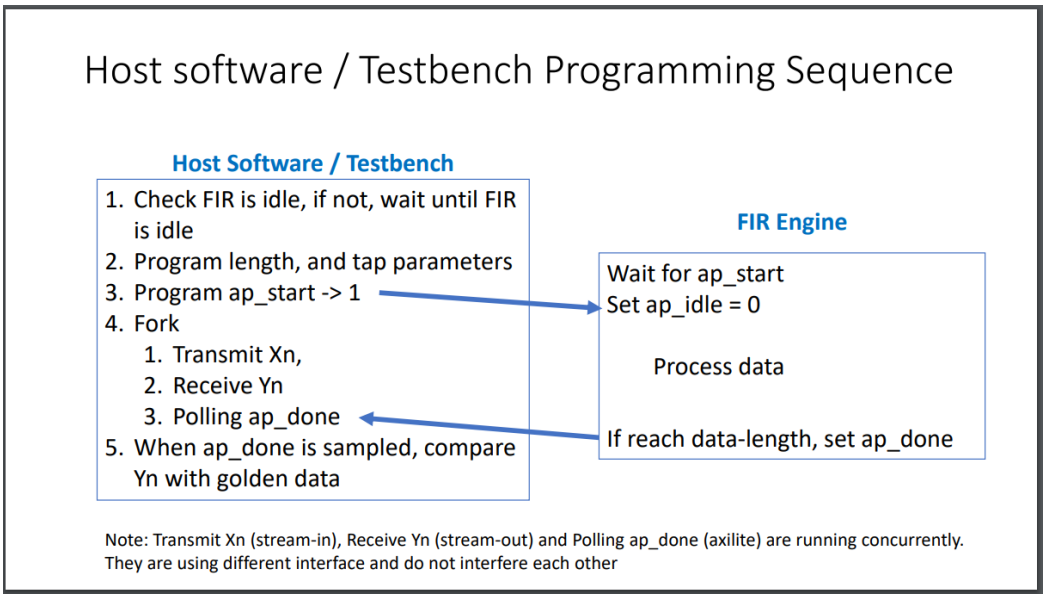
     (4) axi_in_task 負責傳輸 data_length, tap parameters, ap_start

     (5) transmit_Xn_task 負責利用 AXI_Stream 傳輸 x data

     (6) receive_Yn_task 負責利用 AXI_Stream 接收 y data(答案)

     (7) polling_ap_done_task 負責利用 AXI_Lite 檢查 ap_done，檢查 design 完成沒

     (8) cal_latency_task 負責計算 latency




```
160     initial begin
161     reset_task;
162         for(patcount = 1;patcount <= PATNUM; patcount = patcount + 1)begin
163
164             load_input_task;
165             check_idle_task;
166             axi_in_task;
167             fork
168                 transmit_Xn_task;
169                 receive_Yn_task;
170                 polling_ap_done_task;
171                 cal_latency_task;
172             join
173             @(posedge axis_clk);@(posedge axis_clk);
174             $display("-------PASS PATTERN No. %d", patcount);
175         end
176         $finish;
177     end
```

在 design 的部分，我分為 3 個 FSM 來運算，

(1) 上方一排的 FSM 負責處理

(a) 在 idle state 等待 ap_start

(b) 從 TB 得到 Xn

(c) 把 Xn 存進去 RAM

(d) 從 RAM 得到 Xn 與 tap 並計算 FIR

(e) 把計算完的答案傳給 TB

(f) 重複(1)~(4)直到完成全部 DATA

(g) 把 ap_done 傳給 TB

其中，要計算用的 coefficient, ap_start, ap_done, ap_idle 會在最左邊以及最右邊的 idle state 與 ap_done state 完成。

(2) 下方左邊的 FSM 用來完成 AXI Lite Read

(a) 在 idle state 等待 arvalid(等待訊號傳遞)

(b) 根據得到的 address，從 design 或 RAM 得到 ap 或 coef

(c) trigger arready 並等待 rready

(d) trigger rvalid 並傳遞 ap 或 coef

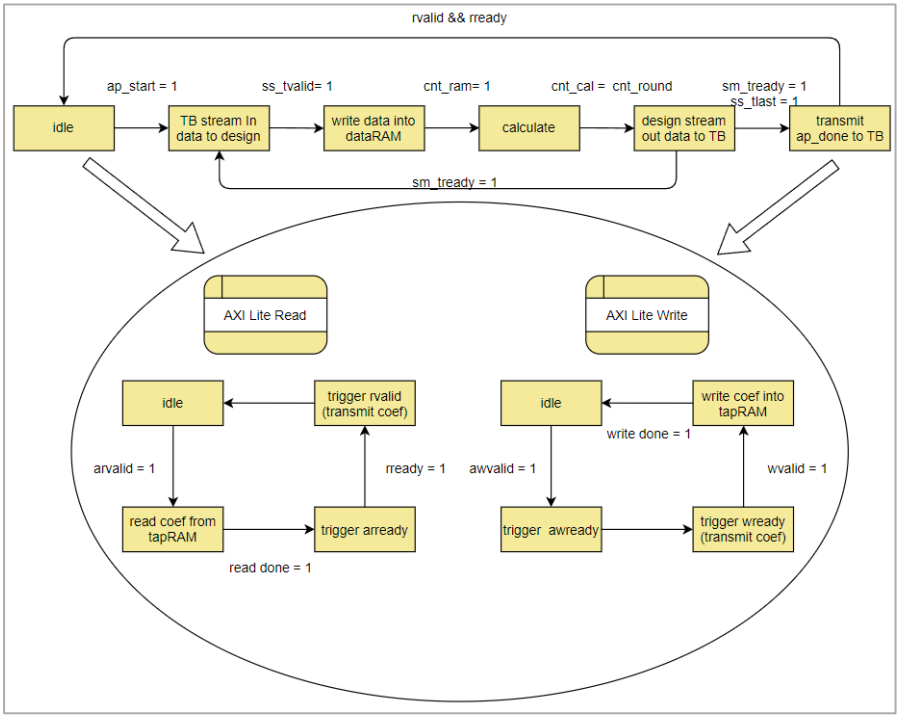
(3) 下方右邊的 FSM 用來完成 AXI Lite Write

(a) 在 idle state 等待 awvalid(等待 axi 傳遞)

(b) trigger awready 並進到下一 state

(c) trigger wready 並等待 wvalid

(d) 根據得到的 address 與 data，把 ap 或 coef 寫入 design 或 RAM



2. Describe operation

- How to receive data-in and tap parameters and place into SRAM ?

利用如上的 FSM 與 AXI Lite protocol，先等待 awvalid，接著 trigger awready 與 wready，並等待 wvalid，在此時會得到 tap parameters。而 data-in 則需要透過 AXI Stream protocol，在 ss_tvalid = 1 時，trigger ss_tready，來得到 data。

放入 SRAM 的地方我利用一個 state 來處理，並控制好訊號，用 counter 來計算需要的寫入/讀取時間，並計算寫入的地址，若為 tap parameter 則寫入 SRAM，若是其他就再做處理。(下圖中，在(1)的地方先歸零，接著在(2)的地方控制寫入/讀取，及地址，在(3)的地方為讀出 tap parameter 來計算 FIR)

```
always@(*)begin
    tap_WE = 4'b0;
    tap_EN = 1'b1;
    tap_Di = 32'b0;
    tap_A  = 32'b0;
    case(cs)
    ST_IDLE:begin
        if(cs_axiw == ST_WRITE_RAM) begin
            if(addr_write <= 'hff && addr_write >= 'h20) begin
                if(flag_ram_read_done == 'd0)begin
                    tap_WE = 4'b1111;
                end
                else begin
                    tap_WE = 4'b0000;
                end
                tap_Di = data_write;
                tap_A  = addr_write - 'h20;
            end
        end
        else if(cs_axir == ST_READ_RAM) begin
            if(addr_read <= 'hff && addr_read >= 'h20) begin
                tap_WE = 4'b0;
                tap_EN = 1'b1;
                tap_Di = 32'b0;
                tap_A  = addr_read - 'h20;
            end
        end
    end
    ST_RAM:begin
        tap_A = index_tap;
    end
    ST_CAL:begin
        tap_A = index_tap;
    end
    endcase
end
```

- How to access shiftram and tapRAM to do computation

  如上圖所言，在(3)的地方為讀取 tap parameter 的 state，在讀取時遇到最大的問題為要提早兩個 cycle 來讀取，第一個 cycle 先賦予值給 A/EN/WE/Di，第二個 cycle 讓 SRAM 吃值，第三個 CYCLE 得到 Dout 並存起來。在 dataRAM 的地方我是用一樣的方式。

- How ap_done is generated

  當 TB 在 stream in data 時，一直監測 ss_tlast(如下圖)，若發現 ss_tlast = 1，把值存起來，並確認下一筆將會輸出最後一筆答案，在按照第一題呈現的 FSM 進到 done state，來讓 ap_done = 1。

```
always@(posedge axis_clk)begin
    if(!axis_rst_n)begin
        flag_ss_last <= 0;
    end
    else begin
        case(cs)
        ST_STREAMIN:begin
            if(ss_tlast)begin
                flag_ss_last <= 1;
            end
        end
        endcase
    end
end
```

3. Resource usage: including FF, LUT, BRAM

```
1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |  332 |     0 |          0 |     53200 |  0.62 |
|   LUT as Logic          |  332 |     0 |          0 |     53200 |  0.62 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |  269 |     0 |          0 |    106400 |  0.25 |
|   Register as Flip Flop |  269 |     0 |          0 |    106400 |  0.25 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```

```
3. DSP
------

+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| DSPs           |    3 |     0 |          0 |       220 |  1.36 |
|   DSP48E1 only |    3 |       |            |           |       |
+----------------+------+-------+------------+-----------+-------+


4. IO and GT Specific
---------------------

+-----------------------------+------+-------+------------+-----------+--------+
|          Site Type          | Used | Fixed | Prohibited | Available |  Util% |
+-----------------------------+------+-------+------------+-----------+--------+
| Bonded IOB                  |  330 |     0 |          0 |       125 | 264.00 |
| Bonded IPADs                |    0 |     0 |          0 |         2 |   0.00 |
| Bonded IOPADs               |    0 |     0 |          0 |       130 |   0.00 |
| PHY_CONTROL                 |    0 |     0 |          0 |         4 |   0.00 |
| PHASER_REF                  |    0 |     0 |          0 |         4 |   0.00 |
| OUT_FIFO                    |    0 |     0 |          0 |        16 |   0.00 |
| IN_FIFO                     |    0 |     0 |          0 |        16 |   0.00 |
| IDELAYCTRL                  |    0 |     0 |          0 |         4 |   0.00 |
| IBUFDS                      |    0 |     0 |          0 |       121 |   0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |          0 |        16 |   0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |          0 |        16 |   0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |          0 |       200 |   0.00 |
| ILOGIC                      |    0 |     0 |          0 |       125 |   0.00 |
| OLOGIC                      |    0 |     0 |          0 |       125 |   0.00 |
+-----------------------------+------+-------+------------+-----------+--------+
```

7. Primitives

Ref Name	Used	Functional Category
FDRE	264	Flop & Latch
LUT2	176	LUT
OBUF	169	IO
IBUF	161	IO
LUT3	90	LUT
LUT6	69	LUT
LUT4	49	LUT
LUT5	29	LUT
LUT1	28	LUT
CARRY4	25	CarryLogic
FDSE	5	Flop & Latch
DSP48E1	3	Block Arithmetic
BUFG	1	Clock

```
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
       2 Input   32 Bit       Adders := 1
       2 Input   12 Bit       Adders := 5
       2 Input    5 Bit       Adders := 2
       2 Input    3 Bit       Adders := 1
       2 Input    1 Bit       Adders := 2
+---Registers :
                  32 Bit    Registers := 7
                  12 Bit    Registers := 5
                   5 Bit    Registers := 2
                   3 Bit    Registers := 2
                   2 Bit    Registers := 2
                   1 Bit    Registers := 3
+---Multipliers :
                 32x32  Multipliers := 1
+---Muxes :
       2 Input   32 Bit        Muxes := 20
       3 Input   32 Bit        Muxes := 3
       4 Input   32 Bit        Muxes := 2
       4 Input   12 Bit        Muxes := 2
       2 Input   12 Bit        Muxes := 9
       3 Input   12 Bit        Muxes := 1
       5 Input   12 Bit        Muxes := 1
       3 Input    5 Bit        Muxes := 1
       2 Input    4 Bit        Muxes := 4
       4 Input    4 Bit        Muxes := 2
       2 Input    3 Bit        Muxes := 2
       3 Input    3 Bit        Muxes := 1
       6 Input    2 Bit        Muxes := 2
       2 Input    2 Bit        Muxes := 3
       4 Input    1 Bit        Muxes := 5
       2 Input    1 Bit        Muxes := 25
       3 Input    1 Bit        Muxes := 5
       5 Input    1 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------
Start ROM, RAM, DSP, Shift Register and Retiming Reporting
---------------------------------------------------------------------------

DSP: Preliminary Mapping Report (see note below. The ' indicates corresponding REG is set)
+------------+-----------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+
|Module Name | DSP Mapping     | A Size | B Size | C Size | D Size | P Size | AREG | BREG | CREG | DREG | ADREG | MREG | PREG |
+------------+-----------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+
|fir         | A2*B2           | 18     | 15     | -      | -      | 48     | 1    | 1    | -    | -    | -     | 0    | 0    |
|fir         | (PCIN>>17)+A2*B | 15     | 15     | -      | -      | 48     | 1    | 0    | -    | -    | -     | 0    | 0    |
|fir         | A2*B2           | 18     | 18     | -      | -      | 48     | 1    | 1    | -    | -    | -     | 0    | 0    |
|fir         | (PCIN>>17)+A2*B | 18     | 15     | -      | -      | 48     | 1    | 0    | -    | -    | -     | 0    | 0    |
+------------+-----------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+

Note: The table above is a preliminary report that shows the DSPs inferred at the current stage of the synthesis flow. Some DSI
---------------------------------------------------------------------------
Finished ROM, RAM, DSP, Shift Register and Retiming Reporting
---------------------------------------------------------------------------
```

4. Timing Report
   - Try to synthesize the design with maximum frequency
   - Report timing on longest path, slack

```
472  ----------------------------------------------------------------------------------------------------
473  | Clock Summary
474  | -------------
475  ----------------------------------------------------------------------------------------------------
476
477  Clock     Waveform(ns)       Period(ns)      Frequency(MHz)
478  -----     ------------       ----------      --------------
479  axis_clk  {0.000 5.500}      11.000          90.909
480
```

```
547  Max Delay Paths
548  --------------------------------------------------------------------------------------
549  Slack (MET) :             0.611ns  (required time - arrival time)
550    Source:                 data_y1__0/CLK
551                              (rising edge-triggered cell DSP48E1 clocked by axis_clk  {rise@0.000ns fall@5.500ns period=11.000ns})
552    Destination:            data_y_reg[31]/D
553                              (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@5.500ns period=11.000ns})
554    Path Group:             axis_clk
555    Path Type:              Setup (Max at Slow Process Corner)
556    Requirement:            11.000ns  (axis_clk rise@11.000ns - axis_clk rise@0.000ns)
557    Data Path Delay:        10.253ns  (logic 8.142ns (79.413%)  route 2.111ns (20.587%))
558    Logic Levels:           9  (CARRY4=5 DSP48E1=1 LUT2=3)
559    Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
560      Destination Clock Delay (DCD):    2.128ns = ( 13.128 - 11.000 )
561      Source Clock Delay      (SCD):    2.456ns
562      Clock Pessimism Removal (CPR):    0.184ns
563    Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
564      Total System Jitter     (TSJ):    0.071ns
565      Total Input Jitter      (TIJ):    0.000ns
566      Discrete Jitter          (DJ):    0.000ns
567      Phase Error              (PE):    0.000ns
568
569      Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
570    -------------------------------------------------------------------    -------------------
571                           (clock axis_clk rise edge)
572                                                      0.000     0.000 r
573                                                      0.000     0.000 r  axis_clk (IN)
574                           net (fo=0)                 0.000     0.000    axis_clk
575                                                                    r  axis_clk_IBUF_inst/I
576                           IBUF (Prop_ibuf_I_O)       0.972     0.972 r  axis_clk_IBUF_inst/O
577                           net (fo=1, unplaced)       0.800     1.771    axis_clk_IBUF
578                                                                    r  axis_clk_IBUF_BUFG_inst/I
579                           BUFG (Prop_bufg_I_O)       0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
580                           net (fo=272, unplaced)     0.584     2.456    axis_clk_IBUF_BUFG
581                           DSP48E1                                    r  data_y1__0/CLK
582    -------------------------------------------------------------------    -------------------
583                           DSP48E1 (Prop_dsp48e1_CLK_PCOUT[47])
584                                                      4.206     6.662 r  data_y1__0/PCOUT[47]
585                           net (fo=1, unplaced)       0.055     6.717    data_y1__0_n_106
586                                                                    r  data_y1__1/PCIN[47]
587                           DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
588                                                      1.518     8.235 r  data_y1__1/P[0]
589                           net (fo=2, unplaced)       0.800     9.035    data_y1__1_n_105
590                                                                    r  data_y[19]_i_10/I0
591                           LUT2 (Prop_lut2_I0_O)      0.124     9.159 r  data_y[19]_i_10/O
```

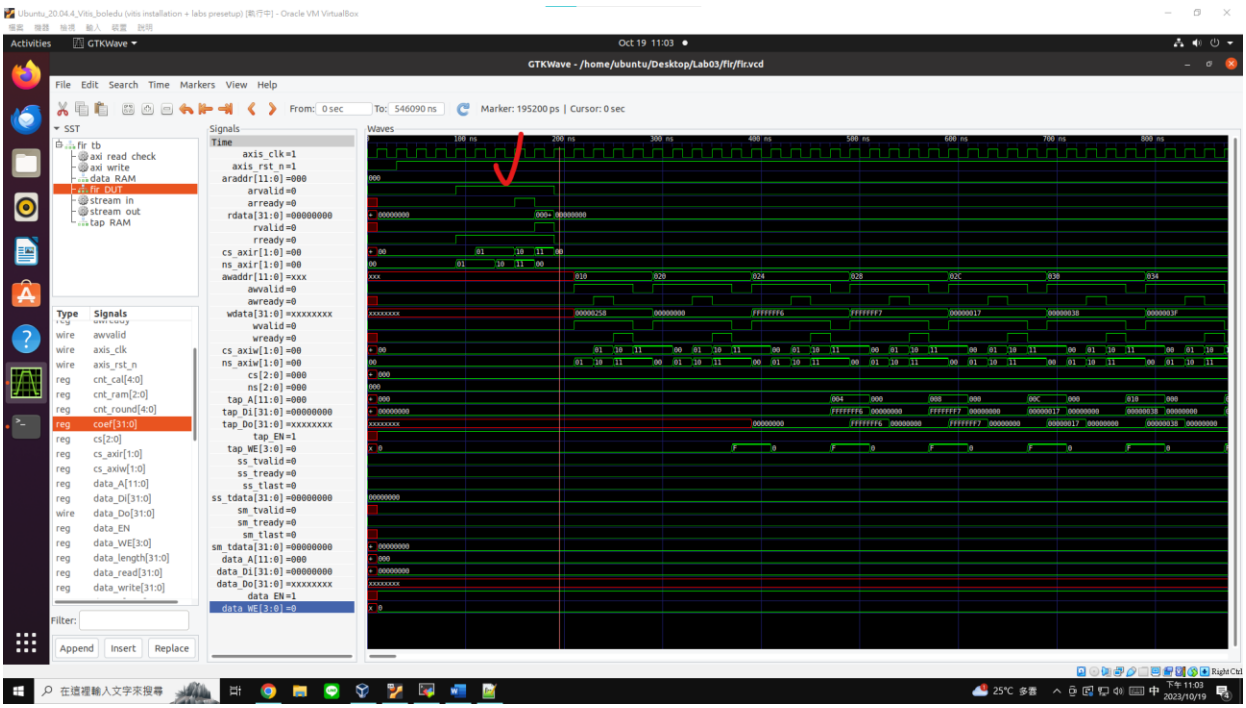
```
                          net (fo=272, unplaced)       0.584     2.456    axis_clk_IBUF_BUFG
                          DSP48E1                                       r  data_y1__0/CLK
  ------------------------------------------------------------------------    -------------------
                          DSP48E1 (Prop_dsp48e1_CLK_PCOUT[47])
                                                       4.206     6.662 r  data_y1__0/PCOUT[47]
                          net (fo=1, unplaced)         0.055     6.717    data_y1__0_n_106
                                                                      r  data_y1__1/PCIN[47]
                          DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                                                       1.518     8.235 r  data_y1__1/P[0]
                          net (fo=2, unplaced)         0.800     9.035    data_y1__1_n_105
                                                                      r  data_y[19]_i_10/I0
                          LUT2 (Prop_lut2_I0_O)        0.124     9.159 r  data_y[19]_i_10/O
                          net (fo=1, unplaced)         0.000     9.159    data_y[19]_i_10_n_0
                                                                      r  data_y_reg[19]_i_3/S[1]
                          CARRY4 (Prop_carry4_S[1]_CO[3])
                                                       0.533     9.692 r  data_y_reg[19]_i_3/CO[3]
                          net (fo=1, unplaced)         0.009     9.701    data_y_reg[19]_i_3_n_0
                                                                      r  data_y_reg[23]_i_3/CI
                          CARRY4 (Prop_carry4_CI_CO[3])
                                                       0.117     9.818 r  data_y_reg[23]_i_3/CO[3]
                          net (fo=1, unplaced)         0.000     9.818    data_y_reg[23]_i_3_n_0
                                                                      r  data_y_reg[27]_i_3/CI
                          CARRY4 (Prop_carry4_CI_O[3])
                                                       0.331    10.149 r  data_y_reg[27]_i_3/O[3]
                          net (fo=2, unplaced)         0.629    10.778    data_y_reg[27]_i_3_n_4
                                                                      r  data_y[27]_i_4/I0
                          LUT2 (Prop_lut2_I0_O)        0.307    11.085 r  data_y[27]_i_4/O
                          net (fo=1, unplaced)         0.000    11.085    data_y[27]_i_4_n_0
                                                                      r  data_y_reg[27]_i_2/S[3]
                          CARRY4 (Prop_carry4_S[3]_CO[3])
                                                       0.376    11.461 r  data_y_reg[27]_i_2/CO[3]
                          net (fo=1, unplaced)         0.000    11.461    data_y_reg[27]_i_2_n_0
                                                                      r  data_y_reg[31]_i_2/CI
                          CARRY4 (Prop_carry4_CI_O[3])
                                                       0.331    11.792 r  data_y_reg[31]_i_2/O[3]
                          net (fo=1, unplaced)         0.618    12.410    data_y0[31]
                                                                      r  data_y[31]_i_1/I1
                          LUT2 (Prop_lut2_I1_O)        0.299    12.709 r  data_y[31]_i_1/O
                          net (fo=1, unplaced)         0.000    12.709    data_y[31]_i_1_n_0
                          FDRE                                          r  data_y_reg[31]/D
  ------------------------------------------------------------------------    -------------------

                          (clock axis_clk rise edge)
                                                      11.000    11.000 r
                                                       0.000    11.000 r  axis_clk (IN)
```

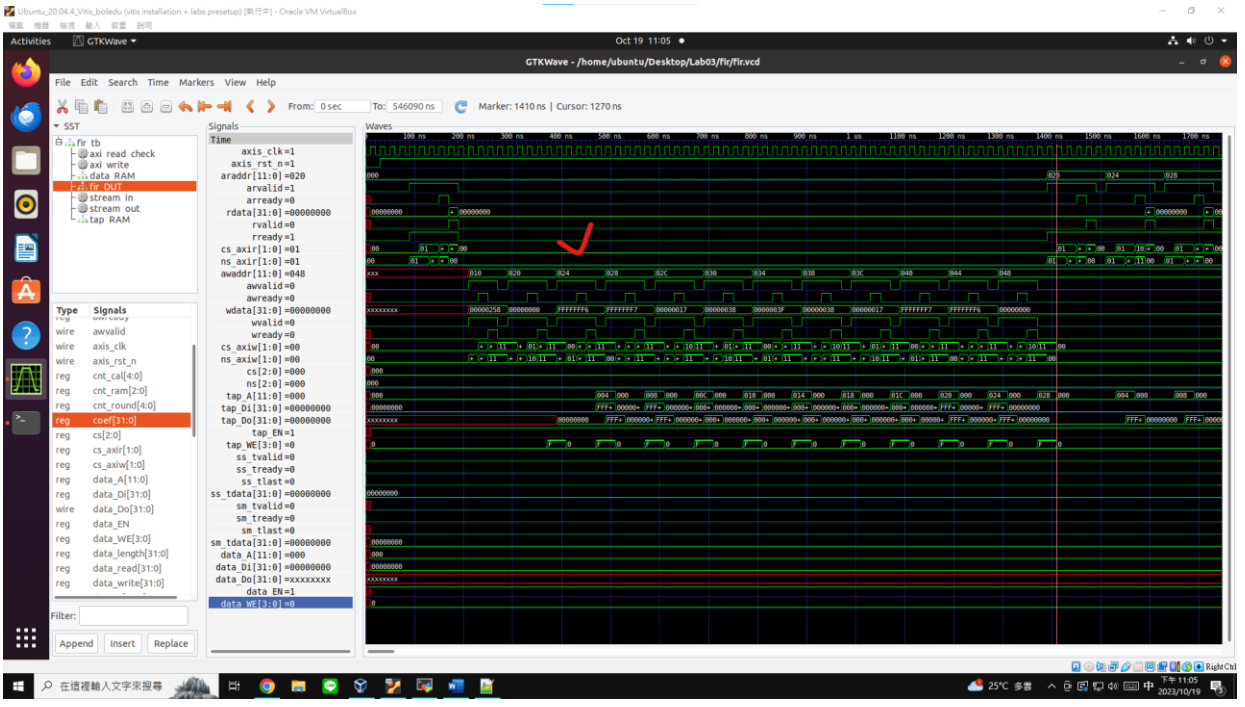
```
                          FDRE                                          r  data_y_reg[31]/D
  ------------------------------------------------------------------------    -------------------

                          (clock axis_clk rise edge)
                                                      11.000    11.000 r
                                                       0.000    11.000 r  axis_clk (IN)
                          net (fo=0)                   0.000    11.000    axis_clk
                                                                      r  axis_clk_IBUF_inst/I
                          IBUF (Prop_ibuf_I_O)         0.838    11.838 r  axis_clk_IBUF_inst/O
                          net (fo=1, unplaced)         0.760    12.598    axis_clk_IBUF
                                                                      r  axis_clk_IBUF_BUFG_inst/I
                          BUFG (Prop_bufg_I_O)         0.091    12.689 r  axis_clk_IBUF_BUFG_inst/O
                          net (fo=272, unplaced)       0.439    13.128    axis_clk_IBUF_BUFG
                          FDRE                                          r  data_y_reg[31]/C
                          clock pessimism              0.184    13.311
                          clock uncertainty           -0.035    13.276
                          FDRE (Setup_fdre_C_D)        0.044    13.320    data_y_reg[31]
  ------------------------------------------------------------------------
                          required time                         13.320
                          arrival time                         -12.709
  ------------------------------------------------------------------------
                          slack                                  0.611
```

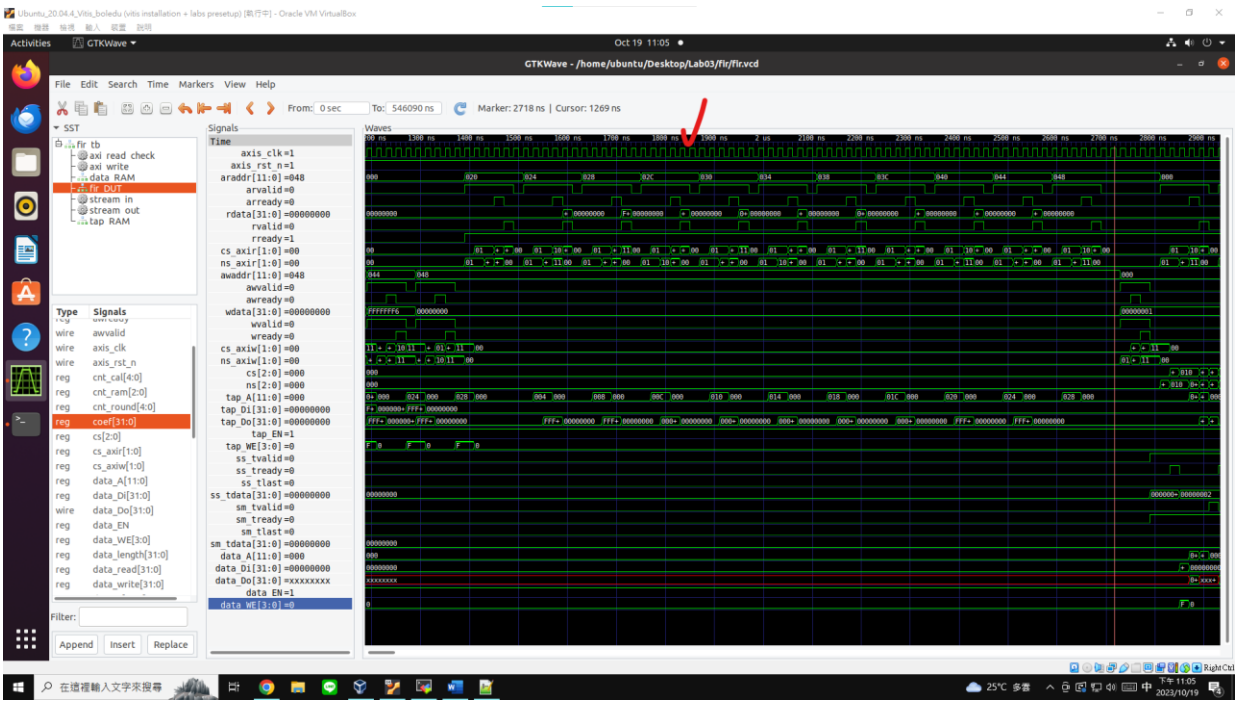
5. Simulation Waveform, show
   - Check ap_idle



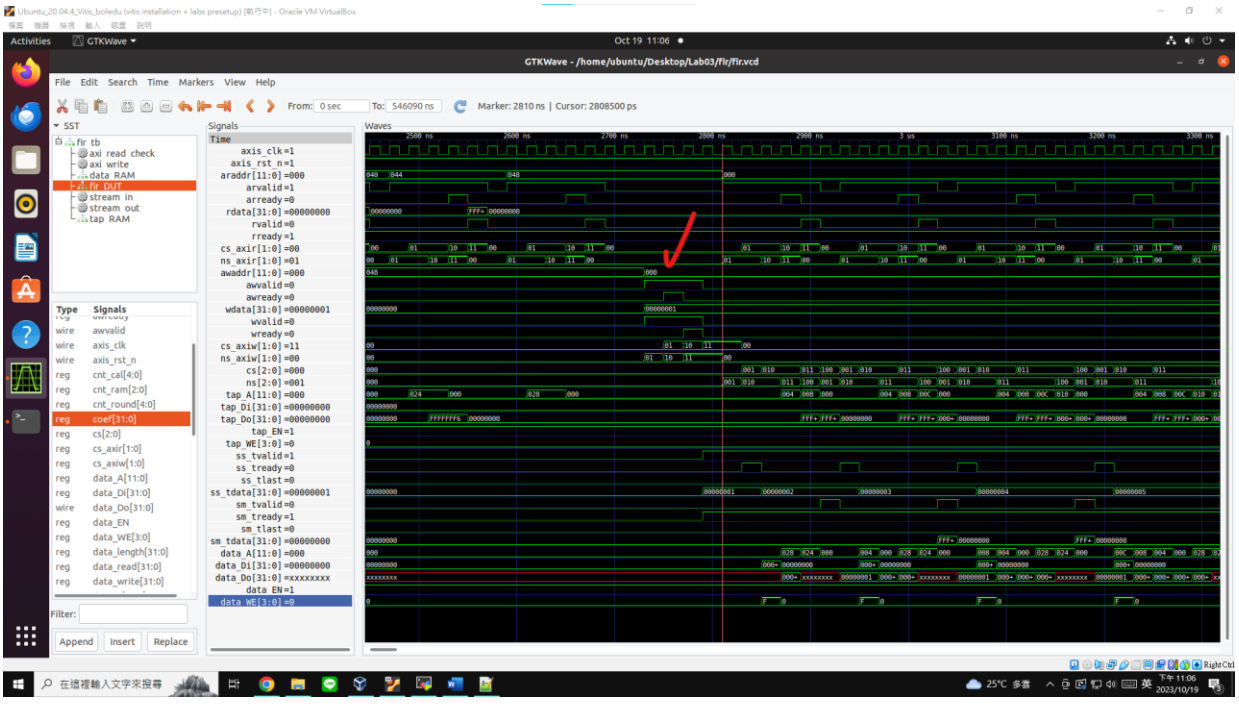
- Write tap parameter into design



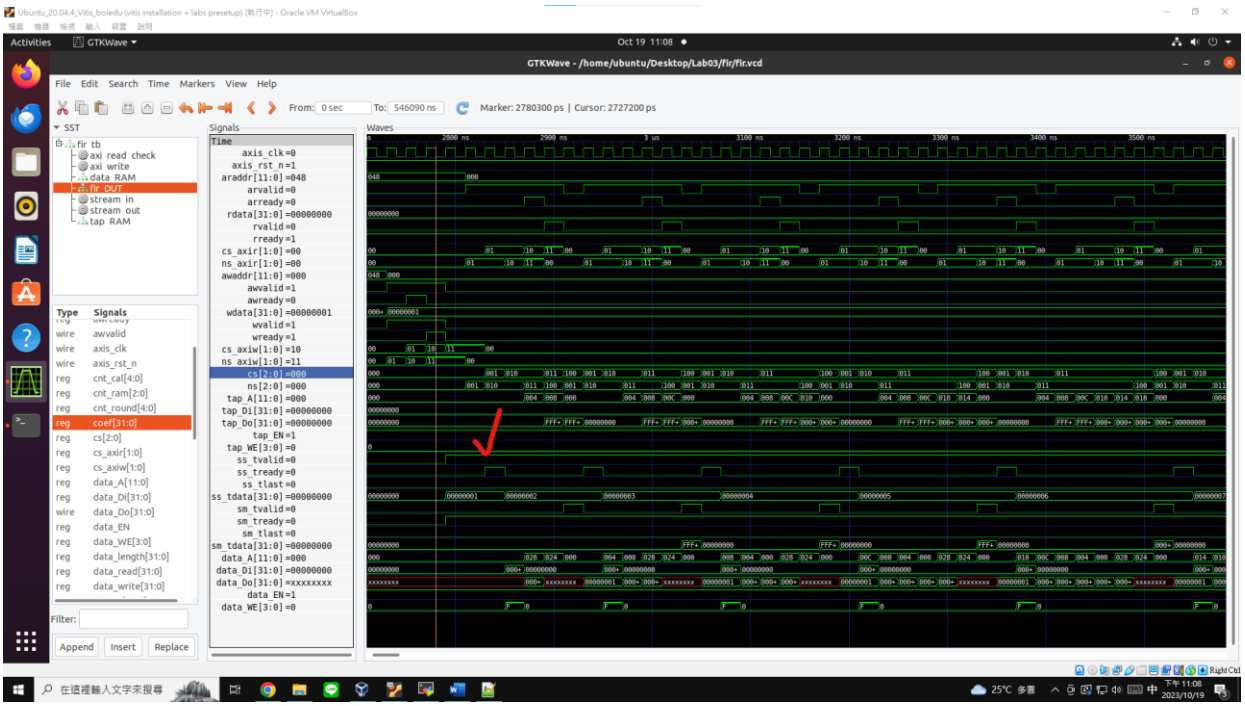
- Read back tap parameter



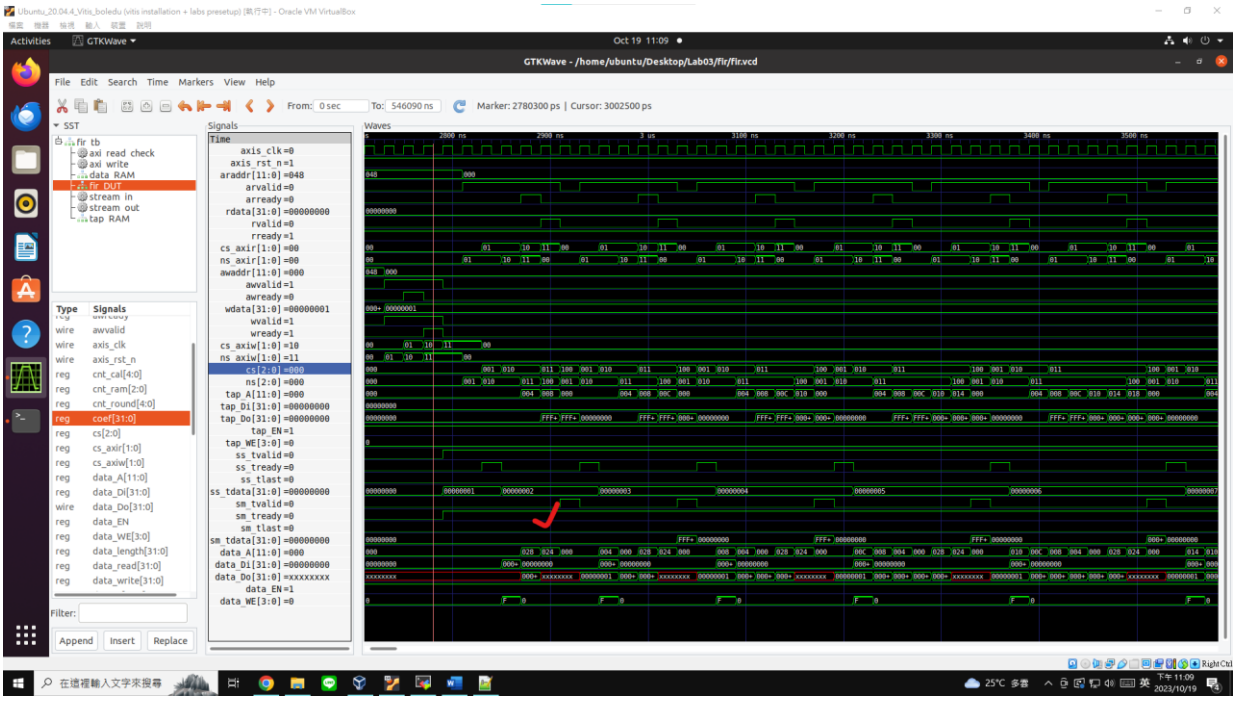
- Program ap start



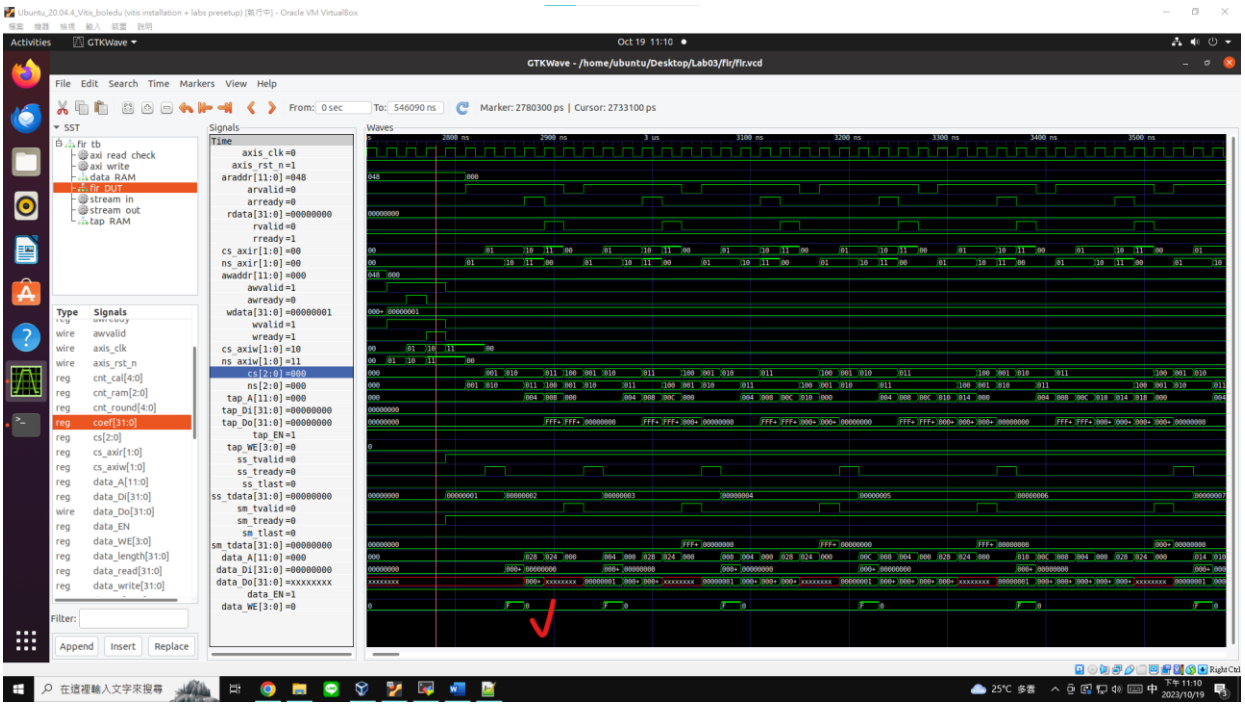
- Data-in stream-in



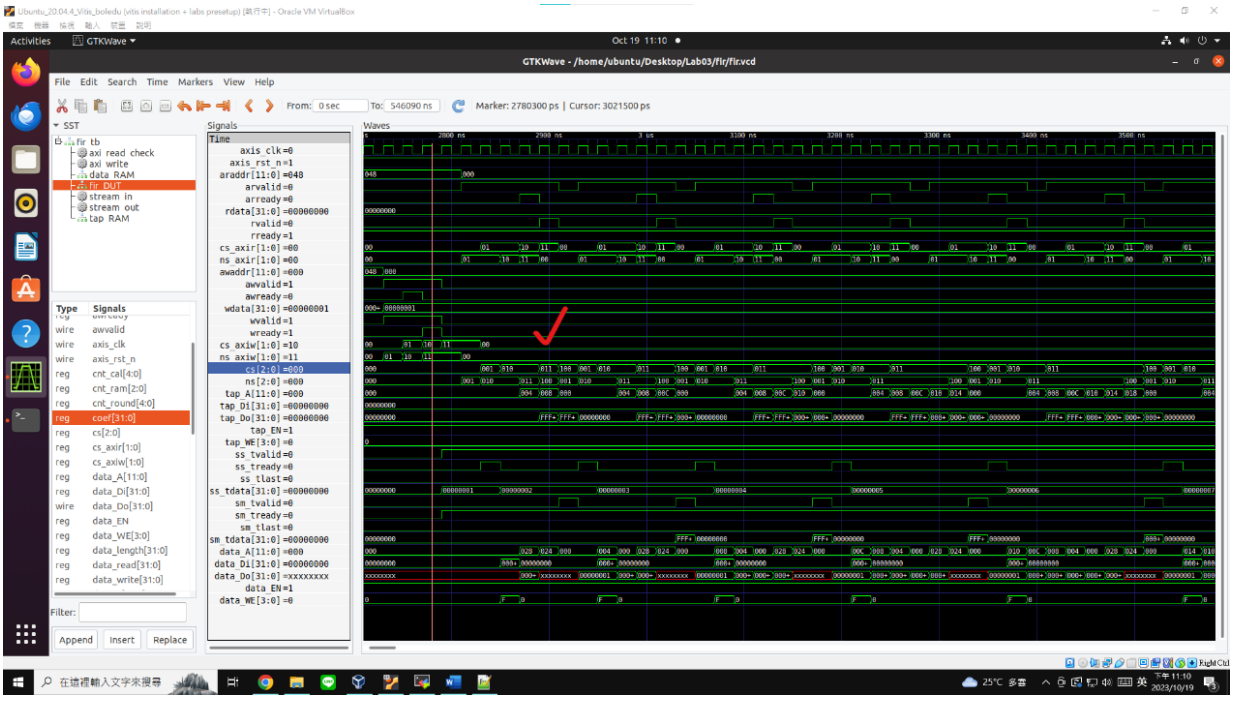
- Data-out stream-out



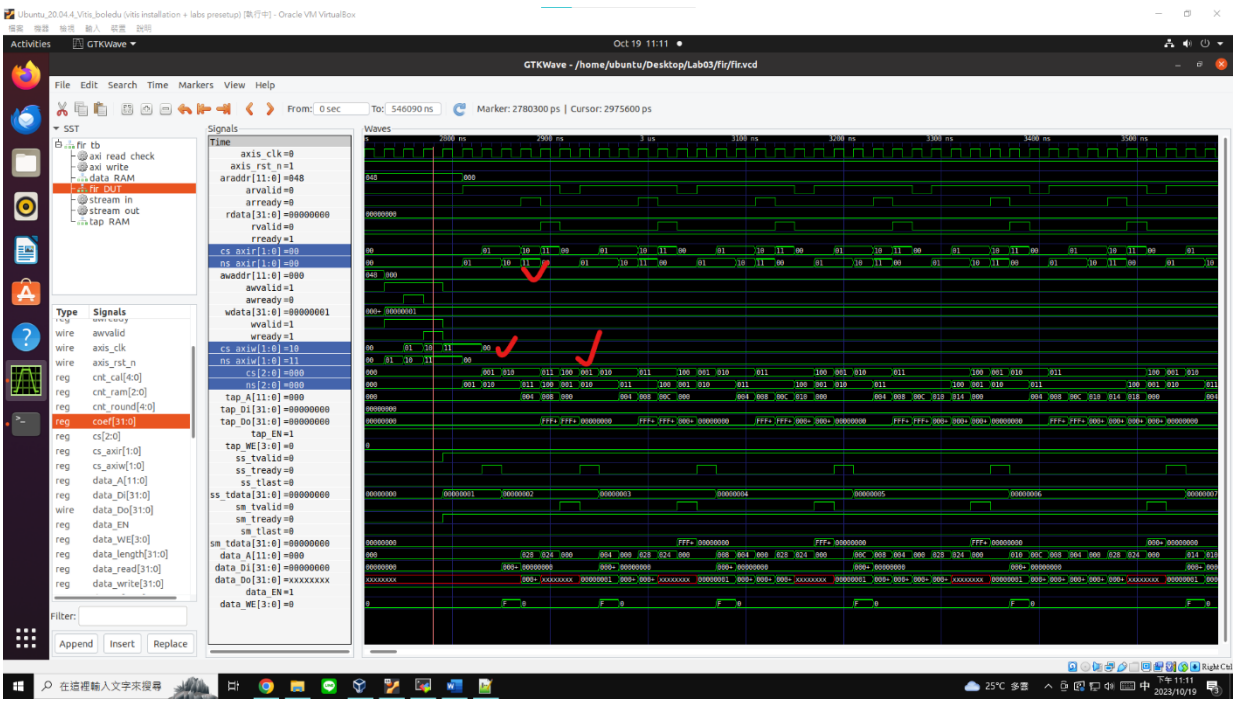
- Write data into RAM



- Read tap from RAM



- FSM


GTKWave - /home/ubuntu/Desktop/Lab03/fir/fir.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 546090 ns
Marker: 2780300 ps | Cursor: 2975600 ps
SST
fir tb
axi read check
axi write
data RAM
fir DUT
stream in
stream out
tap RAM
Signals
Time
axis_clk=0
axis_rst_n=1
araddr[11:0]=048
arvalid=0
arready=0
rdata[31:0]=00000000
rvalid=0
rready=1
cs_axir[1:0]=00
ns_axir[1:0]=00
awaddr[11:0]=000
awvalid=1
awready=0
wdata[31:0]=00000001
wvalid=1
wready=1
cs_axiw[1:0]=10
ns_axiw[1:0]=11
cs[2:0]=000
ns[2:0]=000
tap_A[11:0]=000
tap_Di[31:0]=00000000
tap_Do[31:0]=00000000
tap_EN=1
tap_WE[3:0]=0
ss_tvalid=0
ss_tready=0
ss_tlast=0
ss_tdata[31:0]=00000000
sm_tvalid=0
sm_tready=0
sm_tlast=0
sm_tdata[31:0]=00000000
data_A[11:0]=000
data_Di[31:0]=00000000
data_Do[31:0]=xxxxxxxx
data_EN=1
data_WE[3:0]=0
Type Signals
wire awvalid
wire axis_clk
wire axis_rst_n
reg cnt_cal[4:0]
reg cnt_ram[2:0]
reg cnt_round[4:0]
reg coef[31:0]
reg cs[2:0]
reg cs_axir[1:0]
reg cs_axiw[1:0]
reg data_A[11:0]
reg data_Di[31:0]
wire data_Do[31:0]
reg data_EN
reg data_WE[3:0]
reg data_length[31:0]
reg data_read[31:0]
reg data_write[31:0]
Filter:
Append
Insert
Replace
Waves