Time Borrowing

> 什么是***时间借用***
>
> 时序逻辑的两种基本组成——DFF和Latch
>
> DFF依靠时钟边沿进行采样
>
> Latch根据电平进行触发，在有效电平期间Latch透明，输出随输入改变，在无效电平期间输出被锁存
>
> ***在对Latch组成的时序逻辑电路进行静态时序分析时需要考虑Time Borrowing***

- **Time Borrowing (Cycle stealing)**

  > 在Latch组成的时序逻辑电路中产生

  - 在Latch中，使其透明的时钟边沿称作***开启边沿（Opening edge）***
  - 在接下来的边沿中，使其所存的时钟边沿称作***关闭边沿（Closing edge）***

  DFF中存在建立时间与保持时间，Latch中也存在

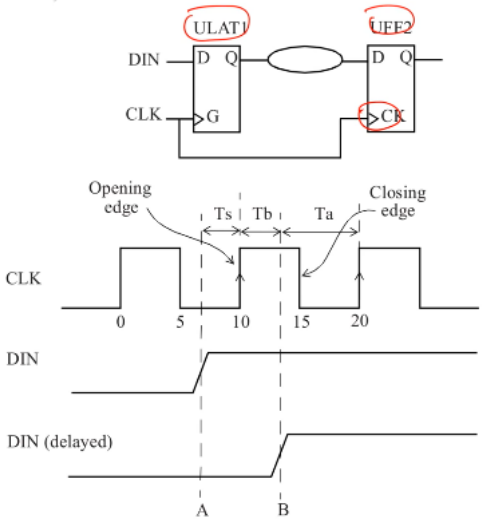
  - 要求Latch的数据端信号在开启边沿到来之前稳定
  - 实际电路中Data不一定非要在Opening edge之前到来，也***可以在Opening edge之后一段时间到来，只要在Closing edge之前数据稳定即可***
  - ***数据滞后于Opening edge时，相当于Latch向后一个周期借用一部分时间——称作Time Borrowing***

Time Borrowing

Here is an example of time borrowing using an active rising edge.

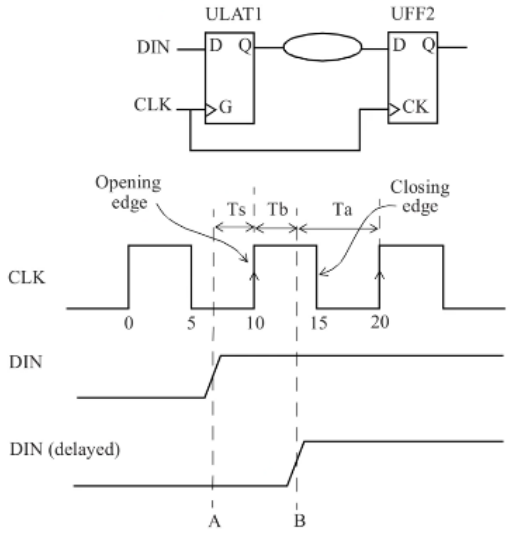
- If data DIN is ready at time A prior to the latch opening on the rising edge of CLK at 10ns, the data flows to the output of the latch as it opens.

If data arrives at time B as shown for DIN (delayed), it borrows time Tb. However, this reduces the time available from the latch to the next flip-flop UFF2 - instead of a complete clock cycle, only time Ta is available.

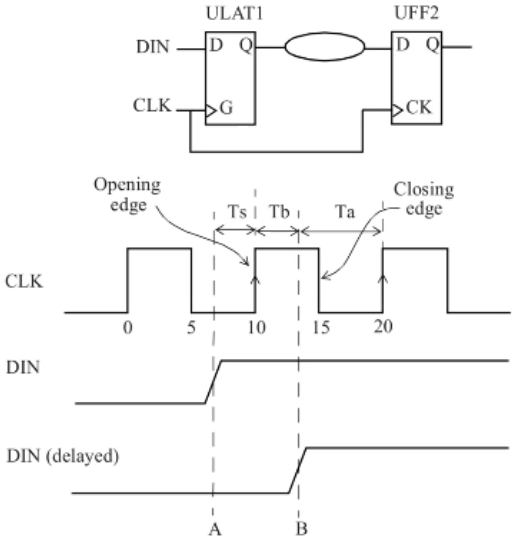


前面电路向下一周期借用时间，相当压缩了后级电路计算需要的时间

- The first rule in timing to a latch is that if the data arrives before the opening edge of the latch, the behavior is modeled exactly like a flip-flop.
- The opening edge captures the data and the same clock edge launches the data as the start point for the next path.

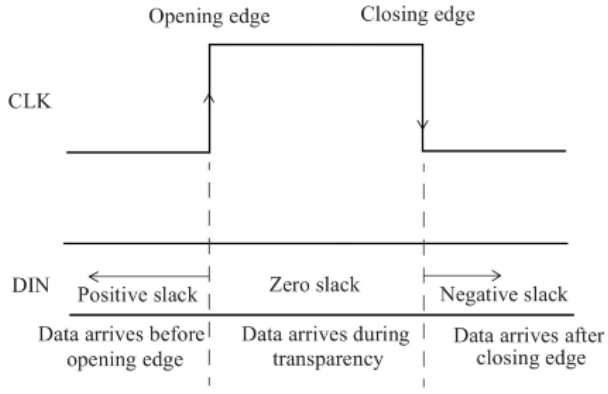


- The second rule applies when the data signal arrives while the latch is transparent (between the opening and the closing edge).
- The output of the latch, rather than the clock pin, is used as the launch point for the next stage.
- The amount of time borrowed by the path ending at the latch determines the launch time for the next stage.



- 按照数据到来时间点可以分为三种

  The timing regions for data arrival for positive slack, zero slack, and negative slack (that is, when a violation occurs).



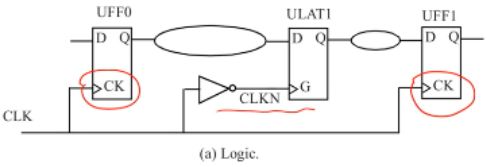
A data signal that arrives after the closing edge at the latch is a timing violation.

- **对特定电路进行分析**

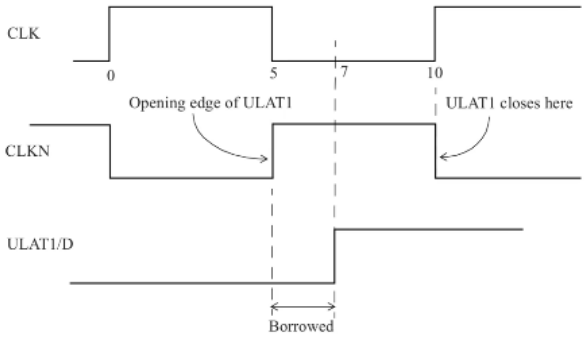
> 在逻辑电路中，门控时钟的设计中为了消除毛刺，可以使用电平相反的Latch

This is the use of a latch with a half-cycle path to the next stage flip-flop.

We next describe three sets of timing reports for the latch example of it to illustrate the different amounts of time borrowed from the next stage.



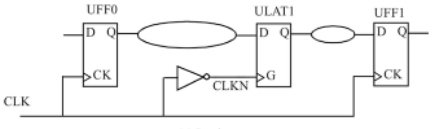
(a) Logic.



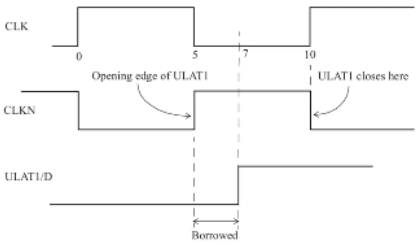
(b) Clock and data waveforms for 7ns data path.

时序报告：

> Launch网络：起点DFF -> 重点 Latch
>
> ***data arrival time = 4.65ns < 5ns***，故为***positive slack***



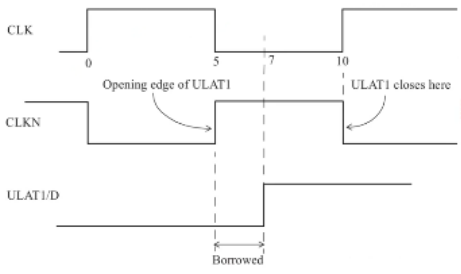
(a) Logic.



(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock CLK (rise edge)                                   0.00       0.00
clock source latency                                    0.00       0.00
clk (in)                                                0.00       0.00 r
UFF0/CK (DF  )                                          0.00       0.00 r
UFF0/Q (DF  )                                           0.12       0.12 r
UBUF0/Z (BUFF  )                                        2.01       2.13 r
UBUF1/Z (BUFF  )                                        2.46       4.59 r
UBUF2/Z (BUFF  )                                        0.07       4.65 r
ULAT1/D (LH  )                                          0.00       4.65 r
data arrival time                                                  4.65
```

> Capture网络：由于数据到达类别为***positive slack***，所以 ***time borrowed from endpoing*** 为***0***



(b) Clock and data waveforms for 7ns data path.

In this case, there is no need to borrow as data reaches the latch ULAT1 in time before the latch opens.

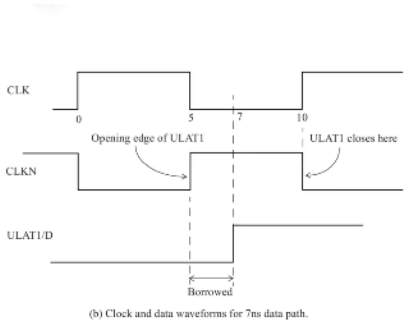
```
clock CLK' (rise edge)                                  5.00       5.00
clock source latency                                    0.00       5.00
clk (in)                                                0.00       5.00 f
UINV0/ZN (INV  )                                        0.02       5.02 r
ULAT1/G (LH  )                                          0.00       5.02 r
time borrowed from endpoint                             0.00       5.02
data required time                                                 5.02
-----------------------------------------------------------------------
data required time                                                 5.02
data arrival time                                                 -4.65
-----------------------------------------------------------------------
slack (MET)                                                        0.36

Time Borrowing Information
-------------------------------------------------------
CLK' nominal pulse width                                5.00
clock latency difference                               -0.00
library setup time                                     -0.01
-------------------------------------------------------
max time borrow                                         4.99
actual time borrow                                      0.00
-------------------------------------------------------
```

当data arrival time分别处于5到10、大于10，使用zero slack、negedge slack进行分析，时序分析中不同之处体现在Capture路径

- **zero slack**

  > 依然能够满足时序

> *此时由Latch->DFF的时序路径也依然能够满足时序要求，时序分析报告只展示Capture路径*



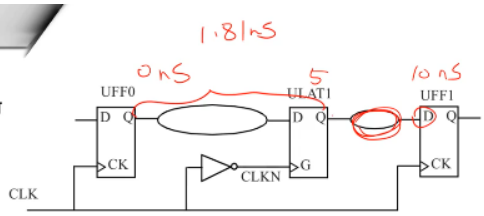
(b) Clock and data waveforms for 7ns data path.

```
clock CLK' (rise edge)                  5.00       5.00
clock source latency                    0.00       5.00
clk (in)                                0.00       5.00 f
UINV0/ZN (INV  )                        0.02       5.02 r
ULAT1/G (LH  )                          0.00       5.02 r
time borrowed from endpoint             1.81       6.83
data required time                                 6.83
-----------------------------------------------------------
data required time                                 6.83
data arrival time                                 -6.83
-----------------------------------------------------------
slack (MET)                                        0.00

Time Borrowing Information
-------------------------------------------------
CLK' nominal pulse width                 5.00
clock latency difference                -0.00
library setup time                      -0.01
-------------------------------------------------
```

In this case, since the data becomes available while the latch is transparent, the required delay of 1.81ns is borrowed from the subsequent path and the timing is still met.

Time Borrowing

Here is the path report of the subsequent path showing that 1.81ns was already borrowed by the previous path.



(a) Logic.

```
clock CLK (rise edge)                  10.00      10.00
clock source latency                    0.00      10.00
clk (in)                                0.00      10.00 r
UFF1/CK (DF  )                          0.00      10.00 r
library setup time                     -0.04       9.96
data required time                                 9.96
-----------------------------------------------------------
data required time                                 9.96
data arrival time                                 -6.95
-----------------------------------------------------------
slack (MET)                                        3.01
```

- **negedge slack**

  数据到来的非常晚，无法满足时序要求

只要数据到达时间满足 positive slack或 zero slack，即可满足时序要求，不发生违例