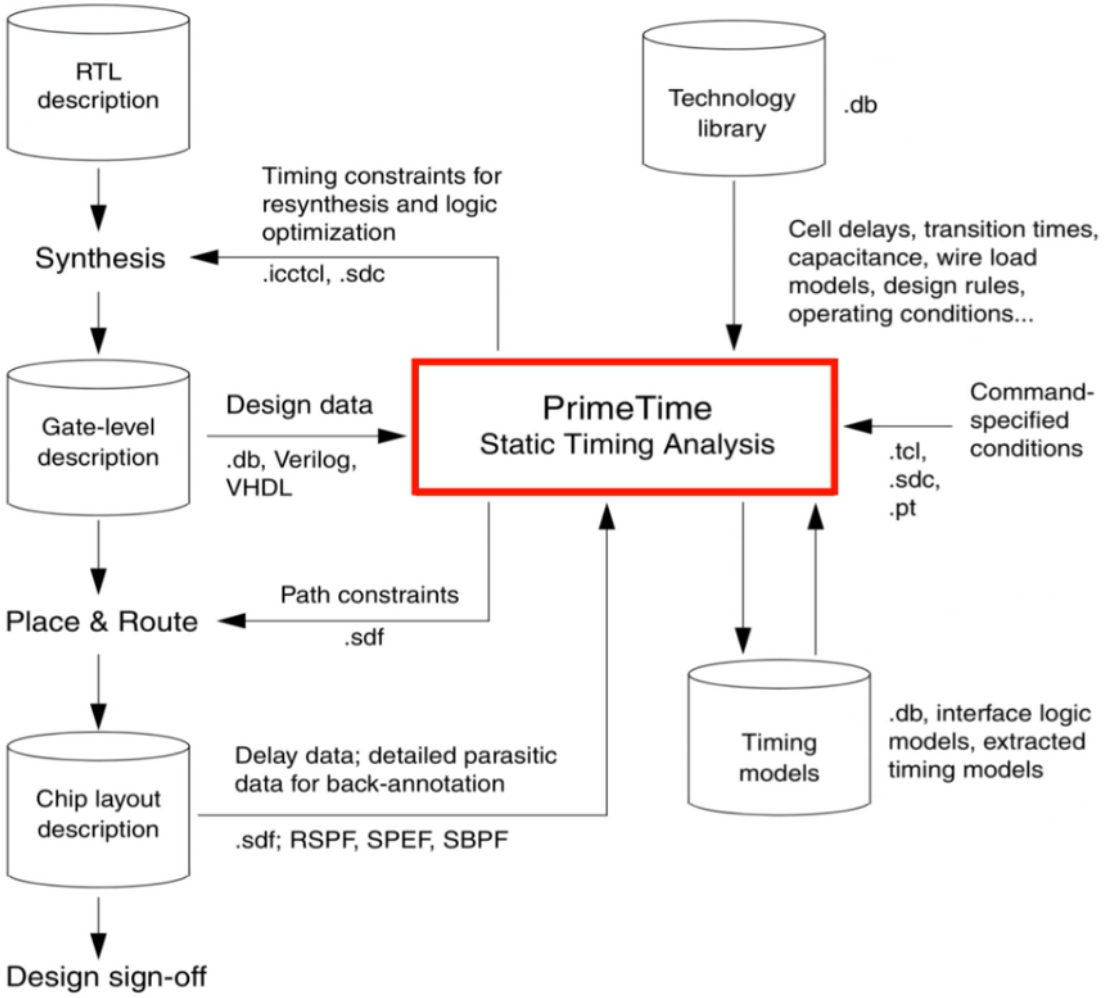
PrimeTime概述

- PrimeTime is a full-chip, gate-level static timing analysis tool that is an essential part of the design and analysis flow for today's large chip designs.
- PrimeTime exhaustively validates the timing performance of a design by checking all possible paths for timing violations, without using logic simulation or test vectors.
- PrimeTime fits ideally into the Synopsys physical synthesis flow because it uses many of the same libraries, databases, and commands as other Synopsys tools such as Design Compiler. It can also operate as a standalone static timing analyzer in other design flows.



PrimeTime 提供了两种环境

- pt_shell (Command Line & script-execution environment based on Synopsys Tcl)
- GUI

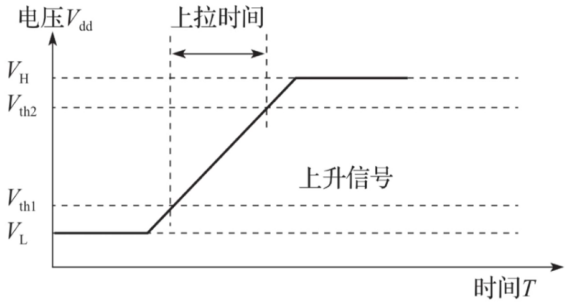
STA基本概念

- Timing Arc

  描述两个节点延时的信息（走线延时、逻辑单元延时）

Cell delay

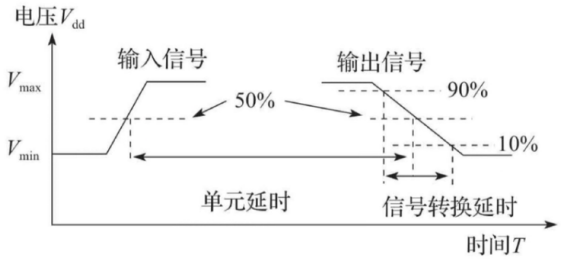
(1) Transition delay



(1) slew_lower_threshold_pct_fall
(2) slew_upper_threshold_pct_fall
(3) slew_lower_threshold_pct_rise
(4) slew_upper_threshold_pct_rise

(2) Logic gate delay

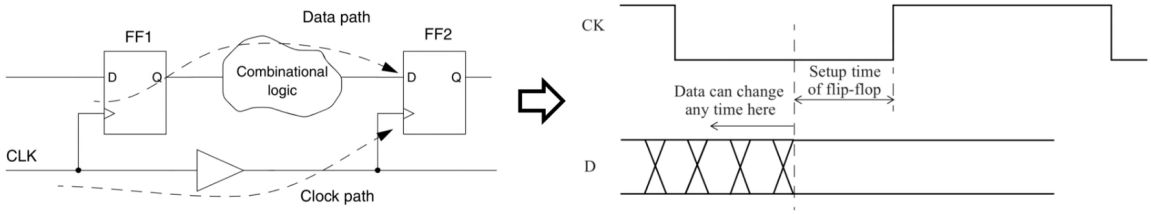
反相器逻辑延时



(1) input_threshold_pct_rise
(2) output_threshold_pct_rise
(3) output_threshold_pct_fall
(4) input_threshold_pct_fall

Setup time and hold time

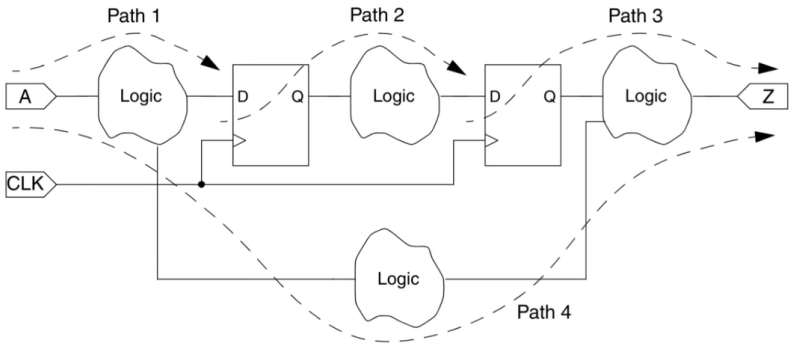
- A setup constraint specifies how much time is necessary for data to be available at the input of a sequential device **before** the clock edge that captures the data in the device.
- This constraint enforces a **maximum** delay on the data path relative to the clock path.



Timing path

The first step performed by PrimeTime for timing analysis is to break the design down into a set of timing paths.

Each path has **a startpoint** and **an endpoint**.



The **startpoint** of a path is a **clock pin** of a sequential element, or possibly an **input port** of the design (because the input data can be launched from some external source).

时序路径起点：触发器cell时钟pin & 输入port

The **endpoint** of a path is a **data input pin** of a sequential element, or possibly an **output port** of the design (because the output data can be captured by some external sink).

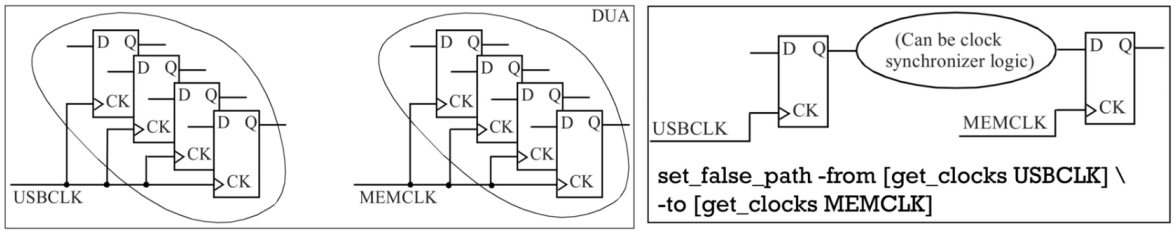
时序路径终点：触发器cell输入pin & 输出port

- 时钟域 - Clock Domains

> 现在的SoC芯片 ***全局异步，局部同步***
>
> **一般的分析软件对异步电路是无能为力的**
>
> ***---对于跨时钟域的电路需要做约束，使EDA对其不做时序分析---***

Clock Domains

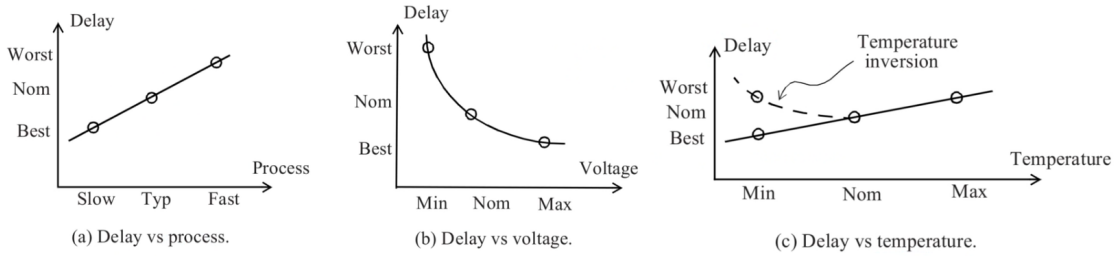
The set of flip-flops being fed by one clock is called its clock domain.



- 操作条件

Operating Conditions

- Static timing analysis is typically performed at a specific operating condition.
- An operating condition is defined as a combination of **Process, Voltage and Temperature** (PVT).
- Cell delays and interconnect delays are computed based upon the specified operating condition.
- There are **three** kinds of manufacturing process models that are provided by the semiconductor foundry for digital designs: **slow** process models, **typical** process models, and **fast** process models.
- The slow and fast process models represent the **extreme corners** of the manufacturing process of a foundry.
- For **robust** design, the design is validated at the extreme corners of the manufacturing process as well as environment extremes for temperature and power supply.



(a) Delay vs process. (b) Delay vs voltage. (c) Delay vs temperature.

It is important to decide the operating conditions that should be used for various static timing analyses.

> 三种操作等级（高温低电压(Worst) -> 一般条件(Typical) -> 低温高电压(Best_case)）

The choice of what operating condition to use for STA is also governed by the operating conditions under which cell libraries are available. Three standard operating conditions are:

- **WCS (Worst-Case Slow):** Process is slow, temperature is highest (say 125C) and voltage is lowest (say nominal 1.2V minus 10%).
- **TYP (Typical):** Process is typical, temperature is nominal (say 25C) and voltage is nominal (say 1.2V).
- **BCF (Best-Case Fast):** Process is fast, temperature is lowest (say -40C) and voltage is highest (say nominal 1.2V plus 10%).

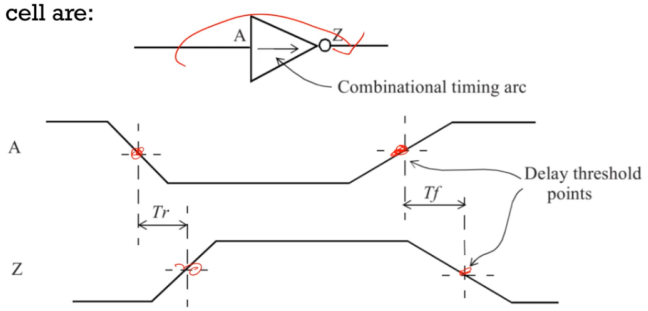
```
set_operating_conditions “WCCOM” -library mychip
# Use the operating condition called WCCOM defined in the cell library mychip.
```

线性延时模型

Let us first consider timing arcs for a simple inverter logic. Since it is an inverter, a rising (falling) transition at the input causes a falling (rising) transition at the output.

The two kinds of delay characterized for the cell are:

- Tr : Output rise delay
- Tf : Output fall delay

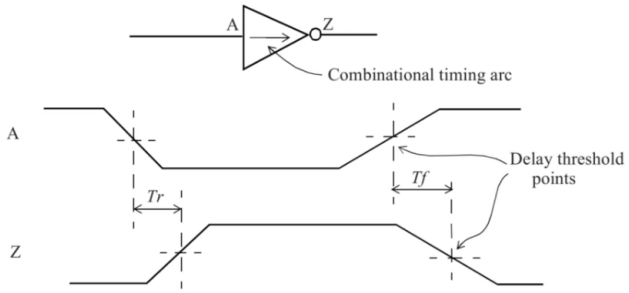


Notice that the delays are measured based upon the threshold points defined in a cell library, which is typically 50% Vdd.

The delay for the timing arc through the inverter cell is dependent on two factors:

i. the **output load**, that is, the capacitance load at the output pin of the inverter, and

ii. the **transition time** of the signal at the input.



- The delay values have a direct correlation with the load capacitance - the larger the load capacitance, the larger the delay.
- In most cases, the delay increases with increasing input transition time.

A simple timing model is a linear delay model, where the delay and the output transition time of the cell are represented as linear functions of the two parameters: input transition time and the output load capacitance.

The general form of the linear model for the delay, D, through the cell is illustrated below.

```
D = D0 + D1 * S + D2 * C
```

where D0, D1, D2 are constants, S is the input transition time, and C is the output load capacitance.

The linear delay models are not accurate over the range of input transition time and output capacitance for submicron tech nologies, and thus most cell libraries presently use the more complex models such as the non-linear delay model.

非线性延时模型（NLDM，Non-Linear Delay Model）

Most of the cell libraries include **table models** to specify the delays and timing checks for various timing arcs of the cell.

- ☐ The table models are referred to as NLDM (Non-Linear Delay Model) and are used for delay, output slew, or other timing checks.
- ☐ The table models capture the delay through the cell for various combinations of input transition time at the cell input pin and total output capacitance at the cell output.

> ***Pin(INP1) -> Pin(OUT) 的延时***
>
> 分为两种：
>
> 1. cell_rise
> 2. cell_fall
>
> 通过输入转换***(Input transition)***和输出负载电容***(Output capacitance)***对其进行查找

An NLDM model for delay is presented in a **two-dimensional form**.

The two independent variables being the **input transition time** and the **output load capacitance**, and the entries in the table denoting the **delay**.

Here is an example of such a table for a typical inverter cell:

```
pin (OUT) {
  max_transition : 1.0;
  timing() {
    related_pin : "INP1";
    timing_sense : negative_unate;
    cell_rise(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*   0.16      0.35     1.43 */ \
        /* 0.1 */   "0.0513,  0.1537,  0.5280", \
        /* 0.3 */   "0.1018,  0.2327,  0.6476", \
        /* 0.7 */   "0.1334,  0.2973,  0.7252");
      }
    cell_fall(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*   0.16      0.35      1.43 */ \
        /* 0.1 */   "0.0617,  0.1537,   0.5280", \
        /* 0.3 */   "0.0918,  0.2027,   0.5676", \
        /* 0.7 */   "0.1034,  0.2273,   0.6452");
```