Data-to-Data Check

> 什么是Data-to-Data Check
>
> 检查两个pin之间相互的时序关系，并且这两个pin之间没有clock，例如数据信号与使能等控制信号
>
> 分别将两个pin定义为***Constrained pin***和***Related pin***，检查两个pin之间相对的时序约束

与基于Flip-flop的时序检查的不同点：

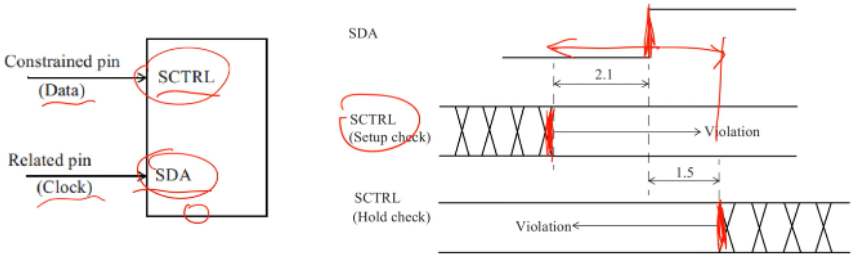
- 建立时间检查（Setup Check）时Launch和Capture在同一个边沿

  > 因此这种***Data-to-Data Check***又被称为***zero-cycle check***或***same-cycle check***

```
set_data_check -from SDA -to SCTRL -setup 2.1
set_data_check -from SDA -to SCTRL -hold 1.5
```

A data to data check is specified using the set_data_check constraint. Here are example SDC specifications. The data to data setup check is performed on the same edge as the launch edge:

```
set_data_check -from SDA -to SCTRL -setup 2.1
set_data_check -from SDA -to SCTRL -hold 1.5
```



- The setup data check implies that SCTRL should arrive at least 2.1ns prior to the edge of the related pin SDA. Otherwise it is a data to data setup check violation.
- The hold data check specifies that SCTRL should arrive at least 1.5ns after SDA. If the constrained signal arrives earlier than this specification, then it is a data to data hold check violation
- This check is useful in a custom-designed block where it may be necessary to provide specific arrival times of one signal with respect to another.
- One such common situation is that of a data signal gated by an enable signal and it is required to ensure that the enable signal is stable when the data signal arrives.

一个例子

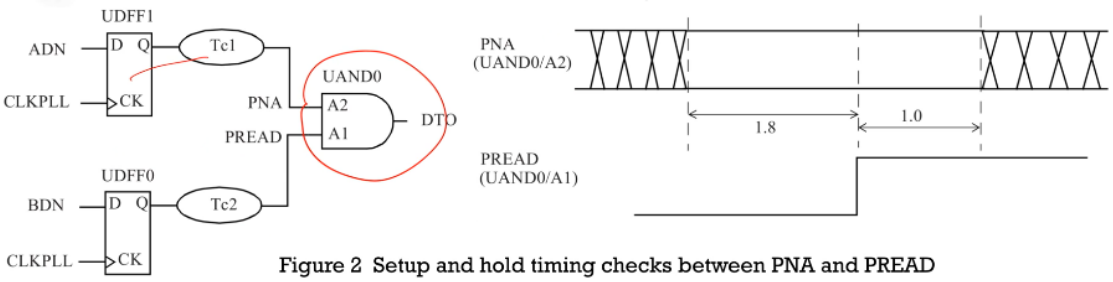


Figure 2 Setup and hold timing checks between PNA and PREAD

Consider the *and* cell shown in Figure 2. The requirement is to ensure that PNA arrives 1.8ns before the rising edge of PREAD and that it should not change for 1.0ns after the rising edge of PREAD. In this example, PNA is the constrained pin and PREAD is the related pin.

Such a requirement can be specified using a data to data setup and hold check:

- set_data_check -from UAND0/A1 -to UAND0/A2 -setup 1.8
- set_data_check -from UAND0/A1 -to UAND0/A2 -hold 1.0

Here is the setup report.

```
Startpoint: UDFF1
  (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
  (rising edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF1/CK (DF   )                         0.00       0.00 r
UDFF1/Q (DF   )                          0.12       0.12 f
UBUF0/Z (BUFF   )                        0.06       0.18 f
UAND0/A2 (AN2   )                        0.00       0.18 f
data arrival time                                   0.18

clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF0/CK (DF   )                         0.00       0.00 r
UDFF0/Q (DF   )                          0.12       0.12 r
UBUF1/Z (BUFF   )                        0.05       0.17 r
UBUF2/Z (BUFF   )                        0.05       0.21 r
UBUF3/Z (BUFF   )                        0.05       0.26 r
UAND0/A1 (AN2   )                        0.00       0.26 r
data check setup time                   -1.80      -1.54
data required time                                  -1.54
-----------------------------------------------------------
data required time                                  -1.54
data arrival time                                   -0.18
-----------------------------------------------------------
slack (VIOLATED)                                    -1.72
```

The setup time is specified as data check setup time in the report.

The failing report indicates that the PREAD needs to be delayed by at least 1.72ns to ensure that PENA arrives 1.8ns before PREAD - which is our requirement.

建立时间检查报告指定了数据检查，因此报告中出现了***data check setup time***参数，根据时序约束确定为1.8

- 对于Hold Check

  默认情况下Hold check在setup check的前一个周期，Data-to-Data Check中Capture网络向前推移了一个周期（由于Setup Check中Capture与Launch在同一个边沿，Hold Check中Capture路径早于Launch路径一个周期），需要使用一个时钟信号进行假定

  The zero-cycle setup check causes the hold timing check to be different from other hold check reports - the hold check is no longer on the same clock edge.

  Here is the clock specification for CLKPLL which is utilized for the hold path report below.

  create_clock -name CLKPLL -period 10 -waveform {0 5} [get_ports CLKPLL]

```
Startpoint: UDFF1
  (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
  (falling edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF1/CK (DF   )                         0.00       0.00 r
UDFF1/Q (DF   ) <-                       0.12       0.12 r
UBUF0/Z (BUFF   )                        0.05       0.17 r
UAND0/A2 (AN2   )                        0.00       0.17 r
data arrival time                                   0.17

clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF0/CK (DF   )                         0.00       0.00 r
UDFF0/Q (DF   )                          0.12       0.12 f
UBUF1/Z (BUFF   )                        0.06       0.18 f
UBUF2/Z (BUFF   )                        0.05       0.23 f
UBUF3/Z (BUFF   )                        0.06       0.29 f
UAND0/A1 (AN2   )                        0.00       0.29 f
data check hold time                     1.00       1.29
data required time                                  1.29
-----------------------------------------------------------
data required time                                  1.29
data arrival time                                  -0.17
-----------------------------------------------------------
slack (MET)                                         1.12
```

> 假定了一个时钟，周期为10，占空比50%

> Launch路径的时间点从1-cycle（10ns）开始，Capture路径的时间点从0-cycle（0ns）开始，***Data-to-Data Check的保持时间检查Launch路径和Capture路径时间点不在同一边沿，Launch路径时间点滞后于Capture路径一个周期***

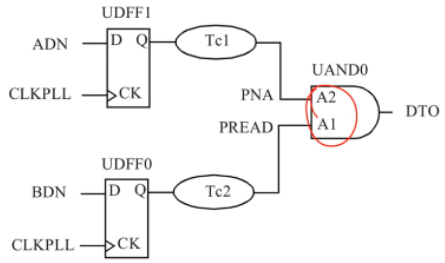
- **当需要在同一个边沿进行Hold check时**

  In some scenarios, a designer may require the data to data hold check to be performed on the same clock cycle.

  The same cycle hold requirement implies that the clock edge used for the related pin be moved back to where the clock edge for the constrained pin is.

  This can be achieved by specifying a multicycle of -1 :

  - set_multicycle_path -1 -hold -to UAND0/A2



set_multicycle_path命令，使用***-1（负一）***参数将***默认的Capture路径早于Launch路径一个周期的时间点向后推一个周期，移至同一个时间点***，数序报告：

Here is the hold timing report for the example above with this multicycle specification.

```
Startpoint: UDFF1
  (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
  (falling edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF1/CK (DF   )                         0.00       0.00 r
UDFF1/Q (DF   ) <-                       0.12       0.12 r
UBUF0/Z (BUFF   )                        0.05       0.17 r
UAND0/A2 (AN2   )                        0.00       0.17 r
data arrival time                                   0.17
```

```
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF0/CK (DF   )                         0.00       0.00 r
UDFF0/Q (DF   )                          0.12       0.12 f
UBUF1/Z (BUFF   )                        0.06       0.18 f
UBUF2/Z (BUFF   )                        0.05       0.23 f
UBUF3/Z (BUFF   )                        0.06       0.29 f
UAND0/A1 (AN2   )                        0.00       0.29 f
data check hold time                     1.00       1.29
data required time                                  1.29
-----------------------------------------------------------
data required time                                  1.29
data arrival time                                  -0.17
-----------------------------------------------------------
slack (VIOLATED)                                   -1.12
```

The hold check is now performed using the same clock edge for the constrained pin and the related pin.

Constrained Pin和Related Pin的定义并不是固定的，约束中***-from***和***-to***选项后的参数是可以互换的

- **Data-to-Data Check中也可以不针对单独某个边沿进行检查，可以使用*-rise_from*和*-fall_from*选项分别对指定边沿进行建立时间检查和保持时间检查**

  ☐ The data to data check is also useful in defining a no-change data check.

  ☐ This is done by specifying a setup check on the rising edge and a hold check on the falling edge, such that a no-change window gets effectively defined.

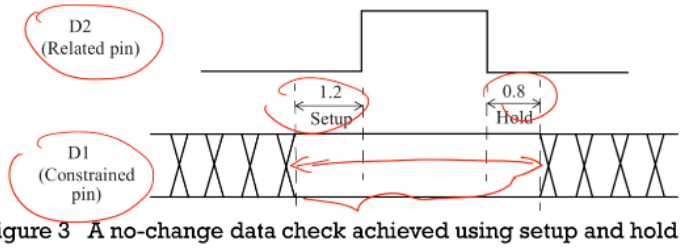


Figure 3 A no-change data check achieved using setup and hold data checks

Here are the specifications for this scenario:

- set_data_check -rise_from D2 -to D1 -setup 1.2
- set_data_check -fall_from D2 -to D1 -hold 0.8