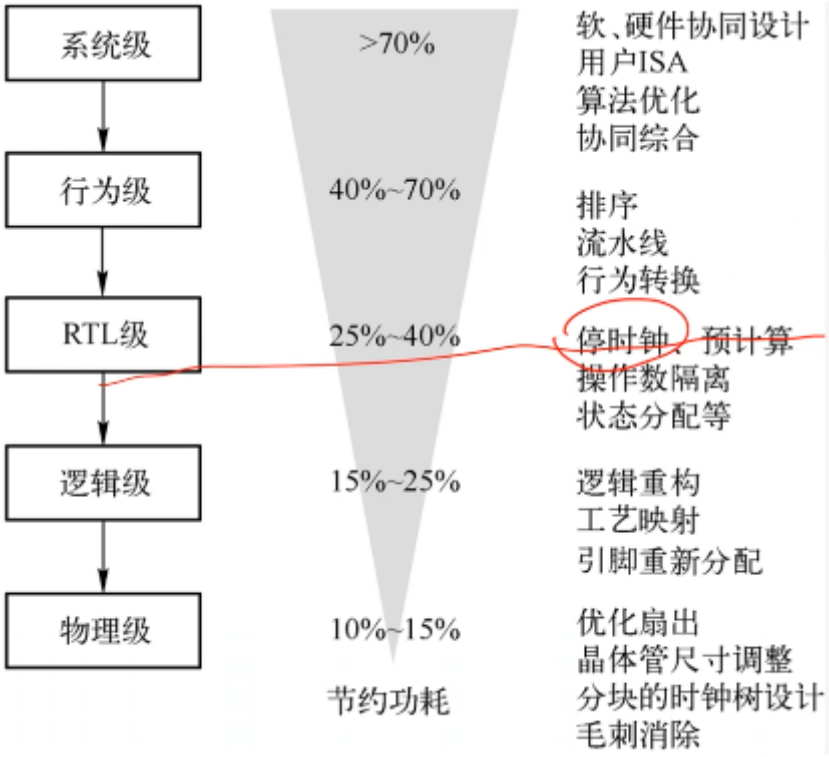
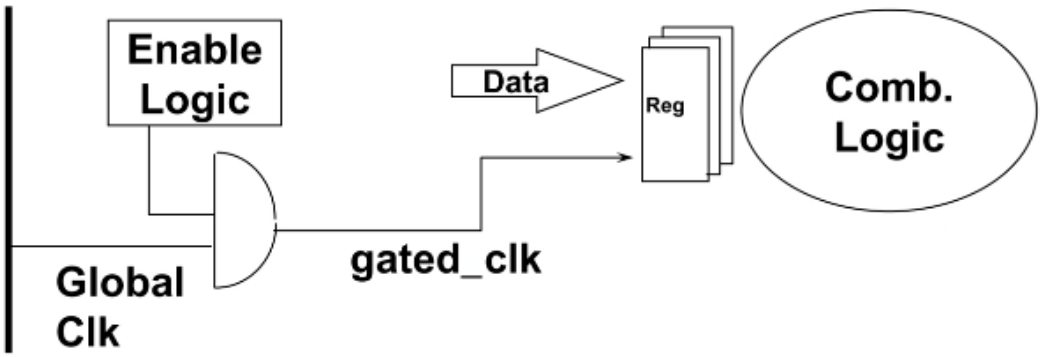
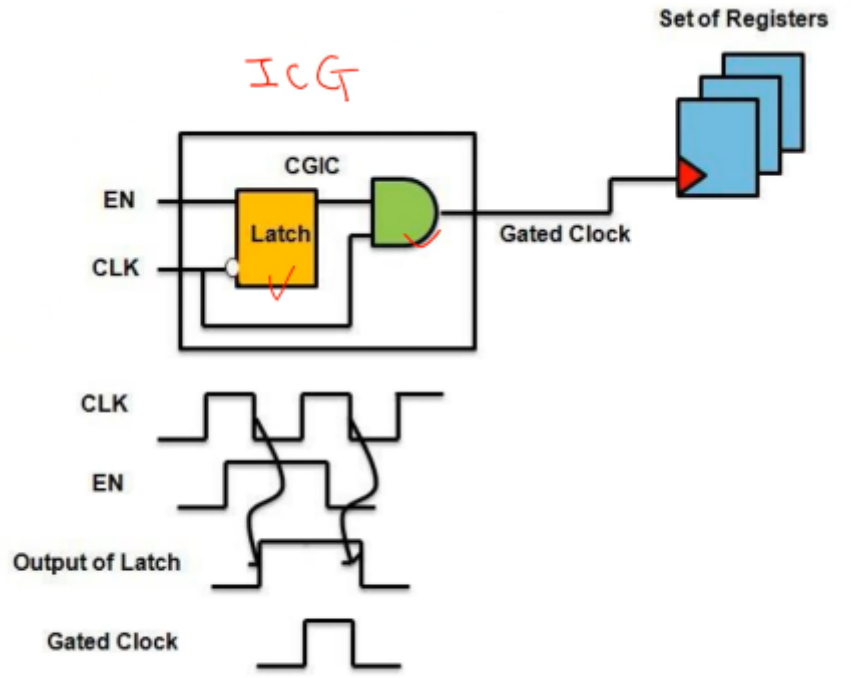
Clock Gating Checks



> 门控时钟
>
> 
>
>
> 有利于动态功耗的控制和优化

只使用一个逻辑门进行门控时会产生毛刺 *（glitch）*

一般情况下使用集成的***ICG （IP）***进行时钟门控设计



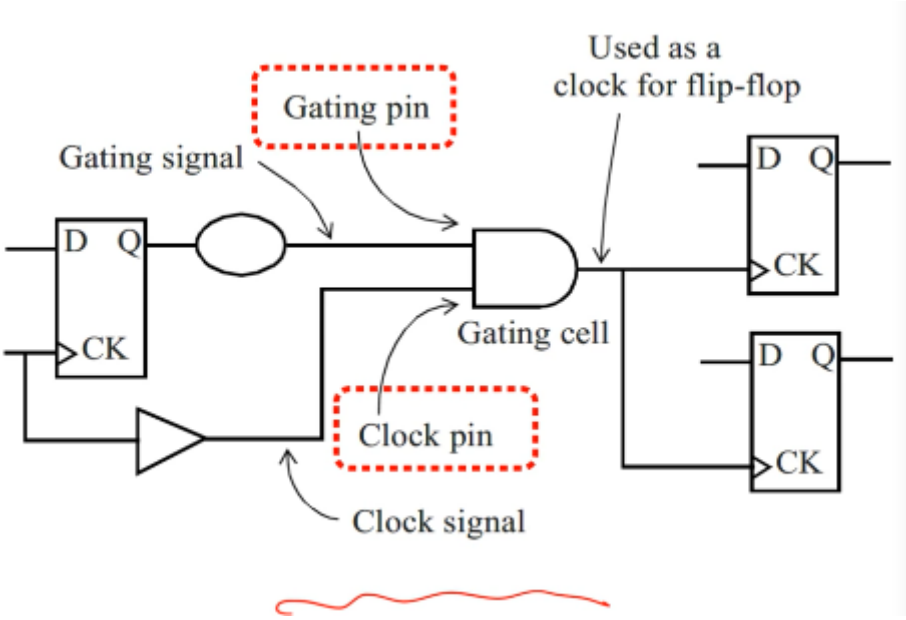
Clock gating cells and a glitch free clock gating

- **门控时钟时序检查**

> 门控时钟检查发生在 - 在一个逻辑单元上 ***(Logic Cell)*** 当一个门控信号 ***(Gating Signal)*** 可以控制时钟信号 ***(Clock Signal)*** 时

  - 门控时钟检查的条件

    1. 经过cell的时钟处于时钟下游***(Clock Downstream)***. ***若时钟信号不是在门控单元(Gating Cell)后被使用，则将不会被推断为门控时钟检查（Clock Gating Check）***
    2. 检查的条件取决于门控信号，检查中门控引脚 ***(Gating pin)*** 的信号不应该是一个时钟信号，或者，***若门控引脚的信号是一个时钟信号，则其不应该在时钟下游使用***



  - 门控时钟检查方法

    检查参考的是有效门控信号的逻辑状态 High和Low指的是时钟能够传到下一级的时候门控信号的值

    1. ***Active-high Clock Gating Check***

> 发生在：门控单元使用与门 *(and)* 或 与非门 *(nand)* 时

有时门控时钟结构相对复杂，使用***多路选择器(Multiplexer)***或***异或门(xor)***，使用命令***set_clock_gating_check***可将时钟门控的结构识别出来进行下一步静态时序分析

Assume that both clocks CLKA and CLKB have the same waveforms.

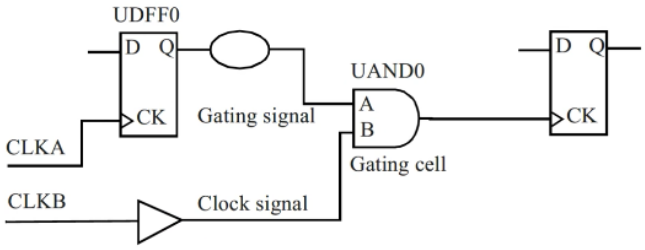


Figure 3 Active high clock gating using an AND cell.

```
create_clock -name CLKA -period 10 -waveform {0 5} [get_ports CLKA]
create_clock -name CLKB -period 10 -waveform {0 5} [get_ports CLKB]
```

> 门控结构***UAND0***中Pin(A)为门控信号，Pin(B)为时钟信号

> 假定电路中存在的两个时钟信号CLKA、CLKB相同

This can be resolved by using a different type of launch flip-flop, say, a negative edge-triggered flip-flop to generate the gating signal. Such an example is shown next.

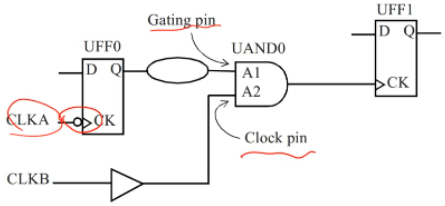
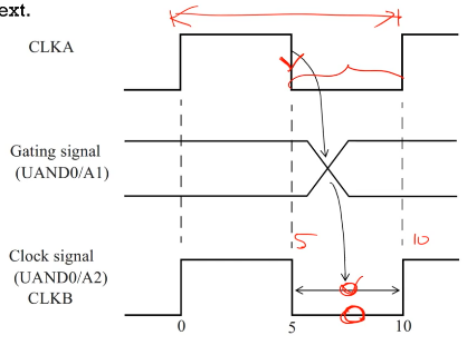


Figure 5 Gating signal clocked on falling edge.



Safe clock gating implies that the output of flip-flop UFF0 must change during the inactive part of the gating clock, which is between 5ns and 10ns.

- 建立时间检查：

Here is the setup path report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by CLKA)
Endpoint: UAND0
  (rising clock gating-check end-point clocked by CLKB)
Path Group: **clock_gating_default**
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKA (rise edge)                         0.00       0.00
clock source latency                           0.00       0.00
CLKA (in)                                      0.00       0.00 r
UDFF0/CK (DF  )                                0.00       0.00 r
UDFF0/Q (DF  )                                 0.13       0.13 f
UAND0/A1 (AN2  )                               0.00       0.13 f
data arrival time                                         0.13
```

```
clock CLKB (rise edge)                  10.00       10.00
clock source latency                     0.00       10.00
CLKB (in)                                0.00       10.00 r
UAND0/A2 (AN2  )                         0.00       10.00 r
clock gating setup time                  0.00       10.00
data required time                                  10.00
-----------------------------------------------------------
data required time                                  10.00
data arrival time                                   -0.13
-----------------------------------------------------------
slack (MET)                                          9.87
```

- The check validates that the gating signal changes before the next rising edge of clock CLKB at 10ns.

- 保持时间检查：

  The active-high clock gating hold check requires that the gating signal changes only after the falling edge of the clock. Here is the hold path report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by CLKA)
Endpoint: UAND0
  (rising clock gating-check end-point clocked by CLKB)
Path Group: **clock_gating_default**
Path Type: min

Point                                   Incr       Path
-----------------------------------------------------------
clock CLKA (rise edge)                  0.00       0.00
clock source latency                    0.00       0.00
CLKA (in)                               0.00       0.00 r
UDFF0/CK (DF  )                         0.00       0.00 r
UDFF0/Q (DF  )                          0.13       0.13 r
UAND0/A1 (AN2  )                        0.00       0.13 r
data arrival time                                  0.13

clock CLKB (fall edge)                  5.00       5.00
clock source latency                    0.00       5.00
CLKB (in)                               0.00       5.00 f
UAND0/A2 (AN2  )                        0.00       5.00 f
clock gating hold time                  0.00       5.00
data required time                                 5.00
-----------------------------------------------------------
data required time                                 5.00
data arrival time                                 -0.13
-----------------------------------------------------------
slack (VIOLATED)                                  -4.87
```

  The hold gating check fails because the gating signal is changing too fast, before the falling edge of CLKB at 5ns.

  One can see that the hold time requirement is quite large. This is caused by the fact that the sense of the gating signal and the flip-flops being gated are the same.

将门控时钟约束至半周期时序路径，能够完成想要的效果

2. ***Active-low Clock Gating Check***

> 发生在：门控单元使用或门 ***(or)*** 或或非门 ***(nor)*** 时

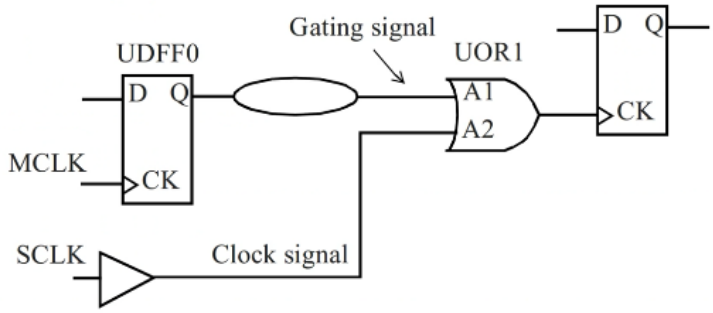


Figure 7 Active-low clock gating check.

create_clock -name MCLK -period 8 -waveform {0 4} [get_ports MCLK]

create_clock -name SCLK -period 8 -waveform {0 4} [get_ports SCLK]

Active-Low结构的门控时钟SetupCheck和HoldCheck都满足需求，不需要像Active-High一样约束至半周期

- 其他结构的门控时钟

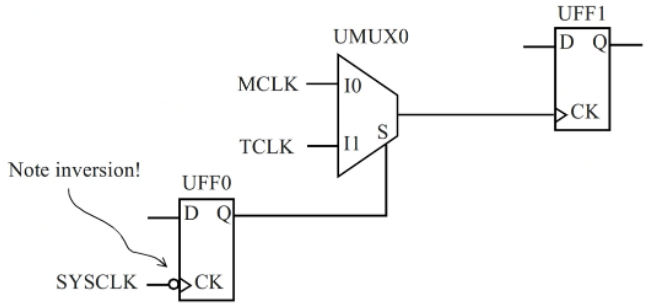


Figure 9 Clock gating using a multiplexer.

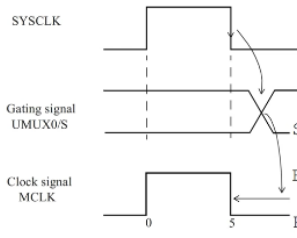
A clock gating check at the multiplexer inputs ensures that the multiplexer select signal arrives at the right time to cleanly switch between MCLK and TCLK.

使用单独的约束命令

set_clock_gating_check -high [get_cells UMUX0]

set_disable_clock_gating_check UMUX0/I1

```
# set_clock_gating_check 命令
# -high 选项指定检查的时间点处于时钟的高电平期间--即使用 Active-High方式进行检查
# -low 选项指定使用 Active-Low方式进行检查
```

> ***Setup Check Report***
>
> 
>
>
> ```
> Startpoint: UFF0
>   (falling edge-triggered flip-flop clocked by SYSCLK)
> Endpoint: UMUX0
>   (rising clock gating-check end-point clocked by MCLK)
> Path Group: **clock_gating_default**
> Path Type: max
> ```
>
> | Point | Incr | Path |
> |---|---|---|
> | **clock SYSCLK (fall edge)** | **5.00** | 5.00 |
> | clock source latency | 0.00 | 5.00 |
> | SYSCLK (in) | 0.00 | 5.00 f |
> | UFF0/CKN (DFN) | 0.00 | 5.00 f |
> | UFF0/Q (DFN) | 0.15 | 5.15 r |
> | **UMUX0/S** (MUX2) | 0.00 | 5.15 r |
> | data arrival time | | 5.15 |

```
clock MCLK (rise edge)                    10.00       10.00
clock source latency                       0.00       10.00
MCLK (in)                                  0.00       10.00 r
UMUX0/I0 (MUX2   )                         0.00       10.00 r
clock gating setup time                    0.00       10.00
data required time                                    10.00
-----------------------------------------------------------
data required time                                    10.00
data arrival time                                     -5.15
-----------------------------------------------------------
slack (MET)                                            4.85
```

Hold Check Report

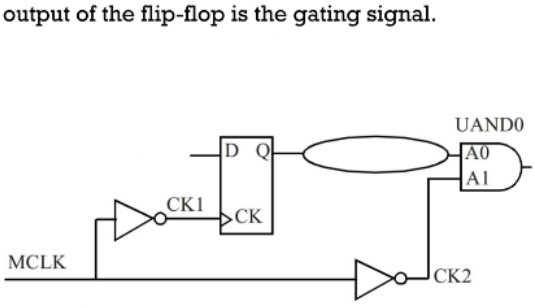
```
Startpoint: UFF0
  (falling edge-triggered flip-flop clocked by SYSCLK)
Endpoint: UMUX0
  (rising clock gating-check end-point clocked by MCLK)
Path Group: **clock_gating_default**
Path Type: min

Point                                     Incr       Path
-----------------------------------------------------------
clock SYSCLK (fall edge)                  5.00       5.00
clock source latency                      0.00       5.00
SYSCLK (in)                               0.00       5.00 f
UFF0/CKN (DFN   )                         0.00       5.00 f
UFF0/Q (DFN   )                           0.13       5.13 f
UMUX0/S (MUX2   )                         0.00       5.13 f
data arrival time                                    5.13

clock MCLK (fall edge)                    5.00       5.00
clock source latency                      0.00       5.00
MCLK (in)                                 0.00       5.00 f
UMUX0/I0 (MUX2   )                        0.00       5.00 f
clock gating hold time                    0.00       5.00
data required time                                   5.00
-----------------------------------------------------------
data required time                                   5.00
data arrival time                                   -5.13
-----------------------------------------------------------
slack (MET)                                          0.13
```

- **带有时钟反转的门控时钟**（也是比较常见的）

Figure 11 shows another clock gating example where the clock to the flip-flop is inverted and the output of the flip-flop is the gating signal.



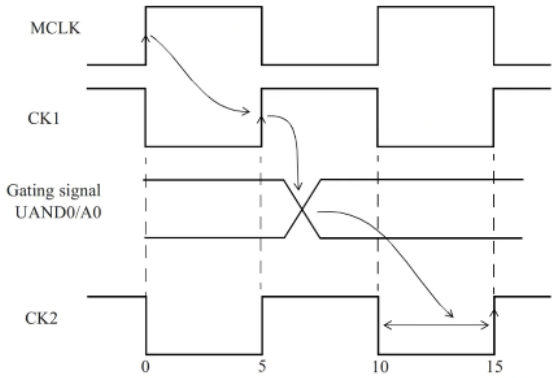


Figure 11 Clock gating example with clock inversion.

Since the gating cell is an *and* cell, the gating signal must switch only when the clock signal at the and cell is low. This defines the setup and hold clock gating checks.

> *对于这种Active-High的门控结构，通常需要让Gating Signal落在Clock Signal的低电平区间（负半周期），以确保Clock Signal能够正确的传播到下一级电路*

默认的时序报告

- SetupCheck

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by MCLK')
Endpoint: UAND0
  (rising clock gating-check end-point clocked by MCLK')
Path Group: **clock_gating_default**
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock MCLK' (rise edge)                        5.00       5.00
clock source latency                           0.00       5.00
MCLK (in)                                      0.00       5.00 f
UINV0/ZN (INV  )                               0.02       5.02 r
UDFF0/CK (DF  )                                0.00       5.02 r
UDFF0/Q (DF  )                                 0.13       5.15 f
UAND0/A1 (AN2  )                               0.00       5.15 f
data arrival time                                         5.15

clock MCLK' (rise edge)                       15.00      15.00
clock source latency                           0.00      15.00
MCLK (in)                                      0.00      15.00 f
UINV1/ZN (INV  )                               0.02      15.02 r
UAND0/A2 (AN2  )                               0.00      15.02 r
clock gating setup time                        0.00      15.02
data required time                                       15.02
-----------------------------------------------------------------
data required time                                       15.02
data arrival time                                        -5.15
-----------------------------------------------------------------
slack (MET)                                               9.87
```

- HoldCheck

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by MCLK')
Endpoint: UAND0
  (rising clock gating-check end-point clocked by MCLK')
Path Group: **clock_gating_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock MCLK' (rise edge)                        5.00       5.00
clock source latency                           0.00       5.00
MCLK (in)                                      0.00       5.00 f
UINV0/ZN (INV  )                               0.02       5.02 r
UDFF0/CK (DF  )                                0.00       5.02 r
UDFF0/Q (DF  )                                 0.13       5.15 r
UAND0/A1 (AN2  )                               0.00       5.15 r
data arrival time                                         5.15
```

```
clock MCLK' (fall edge)                  10.00       10.00
clock source latency                      0.00       10.00
MCLK (in)                                 0.00       10.00 r
UINV1/ZN (INV  )                          0.01       10.01 f
UAND0/A2 (AN2  )                          0.00       10.01 f
clock gating hold time                    0.00       10.01
data required time                                   10.01
-----------------------------------------------------------
data required time                                   10.01
data arrival time                                    -5.15
-----------------------------------------------------------
slack (VIOLATED)                                     -4.86
```

保持检查验证数据（门控信号）是否在 MCLK 下降沿之前 10ns 发生变化

加入约束，引入具体的值

```
# 指定在 Cell(U0/UXOR1)进行门控时钟检查
set_clock_gating_check -setup 2.4 -hold 0.8 [get_cells U0/UXOR1]
# -setup | -hold 指定时钟的建立时间和保持时间
```