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2. Emerging Systems Designed as Analog/Mixed-Signal System-on-Chips

2.1. Introduction

Due to the ever-decreasing cost of electronics hardware and software in last several years, more and more people are able to afford consumer electronics. Consumer electronics have a profound impact on society. The transfer of information around the globe is possible in no time and without any cost. People around the globe are staying connected every moment through social networks. This chapter discusses some examples of systems that have been used in day-to-day life or are being conceptualized for future development. It is difficult to discuss all of these systems in the limited space, though an attempt has been made to discuss the selected systems. Examples of systems discussed are biosensor systems, tablet PC, smart mobile phone, Blue-ray player, multimedia tank, TV tuner card, secure digital camera, net-centric multimedia processor, drug-delivery nano-electro-mechanical systems, radio frequency (RF) universal remote control, RF identification tag, and global positioning systems. These are typically designed as analog/mixed-signal system-on-chips (AMS-SoCs) containing analog, digital, and RF circuits, field-programmable gate array (FPGA), firmware, and software components.

2.2. Atomic Force Microscope

2.2.1. What Is It?

Atomic force microscope (AFM) is a characterization instrument of nanoscience that is used to determine topography and other properties of surfaces [15, 16, 57, 73, 86]. The AFM can analyze the thick and thin films, metals, semiconductors, polymers, and composites. The AFM is also known as scanning force microscope (SFM) or scanning probe microscope (SPM). AFM technique requires minimal specimen preparation and can be operated without vacuum. The high signal-to-noise ratio provided by this instrument allows submolecular features to be discerned. AFM can be used to image and manipulate single molecules.

2.2.2. Background

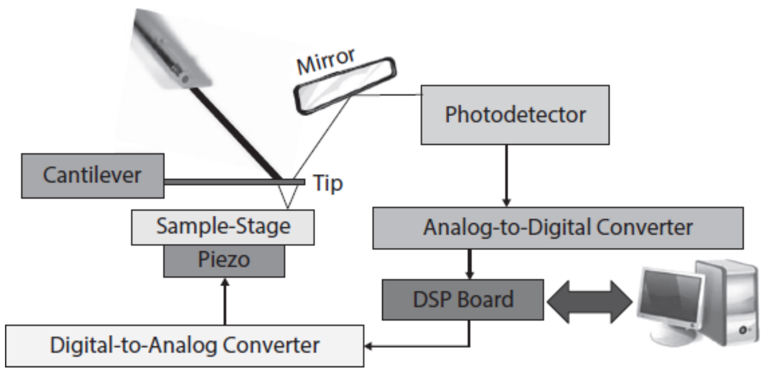
Study of surfaces has been very important right from microscale film and remains the same for the nanoscale films. Of the available techniques, SPM is most popular. It forms images of surfaces using a physical probe that scans the specimen under observation. In 1980, when the scanning tunneling microscope was invented by Gerd Binnig and Heinrich Rohrer, which earned them the Nobel Prize for Physics, it marked the beginning of the scanning microscopes. AFM is a very high-resolution type of SPM that can have a resolution on the order of fractions of a nanometer [76]. Several other microscopes frequently used in nanoscale characterization include scanning electron microscope (SEM) and transmission electron microscopy (TEM). While SEM scans the samples using a high-energy beam of electrons in a raster-scan fashion [64], TEM sends a beam of electrons through an ultra-thin specimen [152]. The interactions of the electrons are then used to create images. However, AFM is still widely used because of simplicity and low cost. From the system design point of view, AFM is presented here; however, system design for TEM or SEM can be discussed in a similar way.

2.2.3. What Is Inside?

The schematic representation of the operational parts of an AFM system is shown inFig. 2.1 [57, 86, 104, 135]. In this AFM system, the samples are scanned with a tip attached to a reflective cantilever. A diode laser is focused onto the back of the reflective cantilever. The laser beam is deflected off the back of the cantilever into a segmented photodetector, as the tip follows the contours of the sample. The position-sensitive photodetector is thus used to measure the probe motion. The photodetector converts light-intensity differences into voltage. The samples are placed on a piezoelectric transducer, which senses the force between the tip and the sample. The digital signal processor (DSP) board provides interfacing among the scanning system, piezoelectric transducer, and the computer as shown [47]. It supplies the voltages to control the piezoelectric transducer through a feedback control system. The feedback loop provides a correction signal to the piezoelectric transducer through the software control from the computer to keep constant force or constant height between the sample and tip. The rate of data acquisition depends on the speed of the feedback loop corrections. AFM feedback loops tend to have a bandwidth of about 10 kHz, resulting in image acquisition times of about 1 minute. The computer stores the local height position at each point and assembles the image. Three-dimensional topographical images of the surfaces are constructed by plotting the local sample height versus the horizontal probe tip position. There are three common modes of operations depending upon the separation of the tip from the sample. The above desktop computer-based AFM system has the following drawbacks [104]:

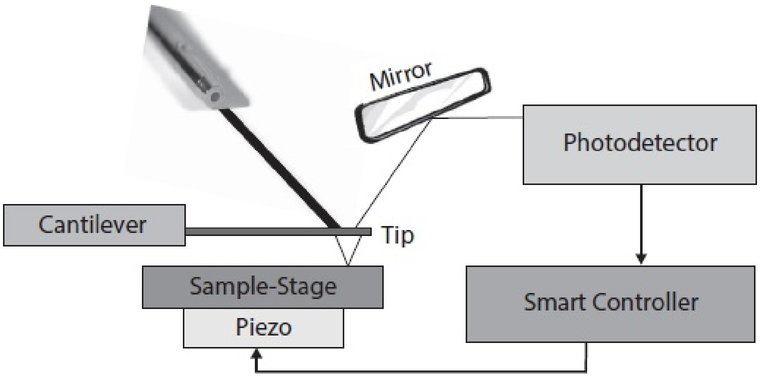
1. A separate computer with several monitors is necessary to operate the system, store images, and do postacquisition analysis.
2. The interface between the DSP and the host desktop computer limits the speed of operation to a great extent due to slower data transfer [57].
3. The use of additional desktop computer and corresponding monitors makes system portability a difficult task.
4. The AFM system including the feedback process is heavily dependent on the software installed in the host desktop computer.
5. The software used for characterization purposes needs high-skilled human intervention, and has relatively low reliability compared to the hardware components of the system.
6. The total power consumption of a typical AFM system is very large and is in the range of 600 to 1800 W [74].

Figure 2.1 The AFM system with a desktop computer and control software.



A portable very large-scale integration (VLSI) system that can replace the host desktop computer and provide a self-sufficient smart controller to operate and characterize and make low-power portable AFM systems is shown in Fig. 2.2 [74, 104]. The smart controller–based portable AFM will not only perform the conventional control operations, but will also have data acquisition, data storage, user interface, and output display. In other words, it will be a self-sufficient unit that will not need the use of separate computer and monitor systems for sample characterization. The AFM characterization system that includes such a smart controller as shown in Fig. 2.2 can be designed as an AMS-SoC. Such a system will reduce the overall power consumption of the system to a great extent. The smart controller of the portable AFM system will include at least the following components: a liquid-crystal display (LCD) for user interface, on-chip memory to store images in JPEG form for a user session, a universal serial bus (USB) port for data transfer for external storage or printing, a compact flash memory for additional storage, low-power image processor to perform various image processing functions for analysis and characterization, and a JPEG codec for compression and decompression of images.

Figure 2.2 The portable all hardware AFM which is a mixed-signal system.



2.3. Biosensor Systems

2.3.1. What Is It?

The formal definition of biosensor is quite diverse. For simplicity, the biosensor can be defined as follows. A biosensor is an analytical device incorporating a deliberate and intimate combination of a specific biological element that creates a recognition event and a physical element that transduces the recognition event [72, 81, 108]. A specific "bio" element, which is called enzyme, recognizes a specific analyte and the "sensor" element transduces the change in the biomolecule into an electrical signal. The bio-element is very specific to the analyte to which it is sensitive. It does not recognize other analytes.

The name "biosensor" signifies that the device is a combination of two parts: bio-element and sensor element (seeFig. 2.3). The bio-element may be an enzyme, antibody, antigen, living cells, tissues, etc. The large variety of sensor elements includes electric current, electric potential, intensity, and phase of electromagnetic radiations, mass, conductance, impedance, temperature, viscosity, and so on. A detailed list of these elements is presented in Fig. 2.4. However, modern-day biosensors are typically built as biosensor systems in which one or more biosensors are used together with lots of additional components for complex sensing and multiuser facility. A single-sensor biosensor system is shown in Fig. 2.5 [37]. The biocatalyst converts the substrate to product. The transducer determines this reaction and converts it to an electrical signal. The amplifier amplifies the signal for better sensing. The analog-to-digital converter (ADC) converts the analog signal to digital signal. The DSP processes this signal. The display unit displays the signal obtained from the DSP.

Figure 2.3 Basic concepts of biosensor [108].

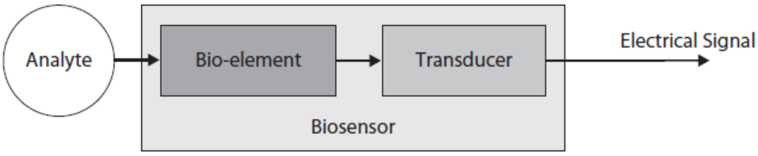


Figure 2.4 Elements of a biosensor [108].

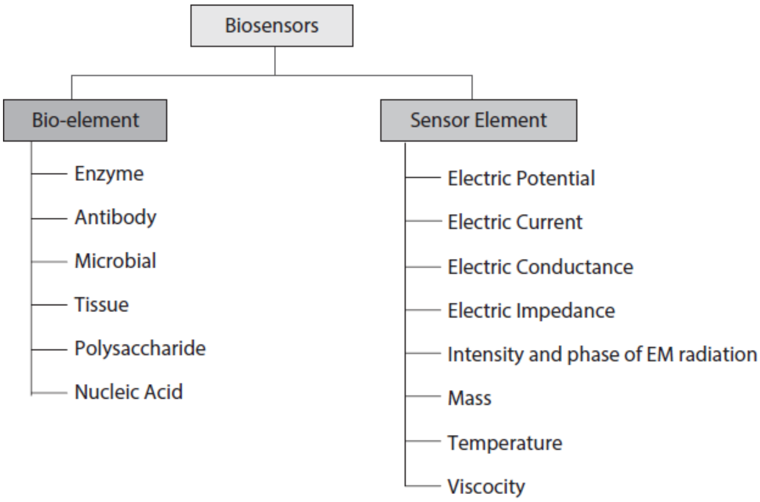
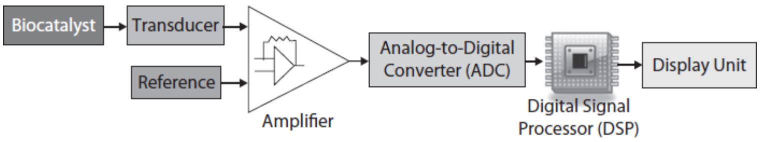


Figure 2.5 Basic concepts of biosensor systems [37].



Depending on the transducing mechanism used, the biosensors can be of many types, as follows [93, 108]:

1. Resonant Biosensors. In this type of biosensors, an acoustic wave transducer is coupled with an antibody (bio-element). The resonant frequency of the transducer is measured.
2. Optical-Detection Biosensors. The output-transduced signal that is measured is a light signal for this type of biosensors.
3. Thermal-Detection Biosensors. This type of biosensors is constructed combining enzymes with temperature sensors.
4. Ion-Sensitive FETs (ISFETs) Biosensors. These are basically semiconductor field-effect transistors (FETs) having an ion-sensitive surface whose electrical potential changes when the ions and the semiconductor interact. The change is then measured.
5. Electrochemical Biosensors. The underlying principle for this class of biosensors is that many chemical reactions produce or consume ions or electrons, which, in turn, cause some change in the electrical properties of the solution that can be sensed out and used as a measuring parameter.

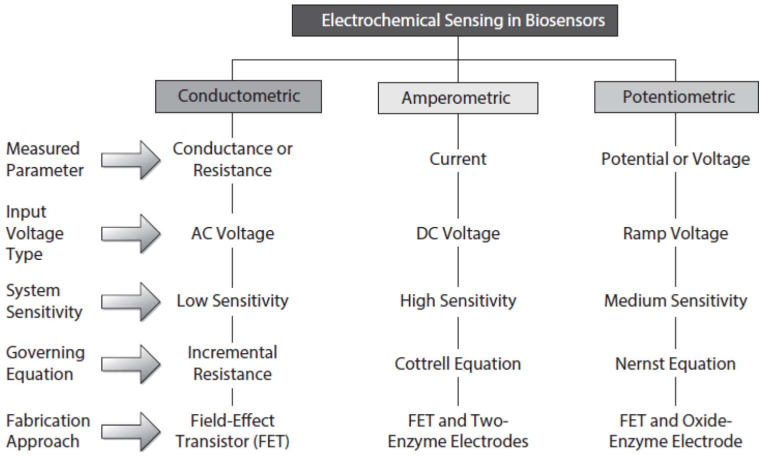
The electrochemical biosensors based on the parameter measured can be further classified in the following types [138]:

1. Conductometric. The measured parameter is the electrical conductance/resistance of the solution.
2. Amperometric. In this case, the measured parameter is current.

3. Potentiometric. In this type of sensors, the measured parameter is oxidation/reduction potential of the electrochemical reaction.

A comparative discussion of these three types is given in Fig. 2.6.

Figure 2.6 Different types of electrochemical sensing [108].

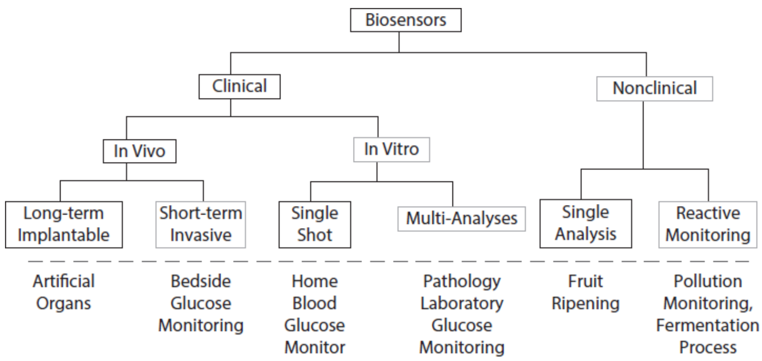


2.3.2. Background

There has always been tremendous interest in improving the quality of human life and life expectancy. The history of biosensors starts in 1950 with the first experiment by L.C. Clark (who is addressed as the father of biosensors) to measure the dissolved oxygen in blood [60, 108, 126]. This experiment became a commercial reality in 1973 with the development of Glucose Analyser in Ohio, USA. This is considered as the first of many biosensor-based laboratory analyzers. The first bioaffinity biosensor was developed in 1980 in which radiolabeled receptors were immobilized on a transducer surface. The blood-glucose biosensors were launched in 1987. In 1992, the handheld blood biosensors were developed. Since then the biosensors have strived for the simple solutions to measurement in complex matrices. The individual biosensors have been doing an excellent job; however, pragmatic solutions to many problems involve the construction of biosensor systems that include associated electronics, fluidics, and separation technology.

In the last decade, tons of biosensors have been developed for diverse applications. The biosensors can have a variety of biomedical and industry applications [91, 132, 134]. Some of the possible applications are shown inFig. 2.7. Though the major application so far is in blood glucose sensing, because of abundant market potential [81] biosensors have tremendous opportunities for commercialization in other fields of application as well. Depending on the field of applications, biosensors are known by many other names, including immunosensors, optrodes, chemical canaries, resonant mirrors, glucometers, biochips, and biocomputers [56].

Figure 2.7 Potential applications of biosensors [81, 108].



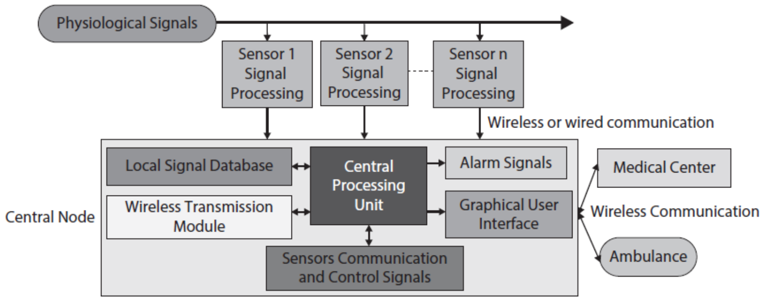
2.3.3. What Is Inside?

The type of biosensors and their systems are quite diverse in nature. So, it is difficult to present a common architecture for biosensor system. However, several representative biosensor systems are presented for better understanding.

2.3.3.1. A Wearable Biosensor System with Multiple Biosensors

The architecture of a biosensor system is shown in Fig. 2.8. The wearable biosensor system may include a variety of components such as sensors, wearable materials, smart textiles, actuators, power supplies, wireless communication modules, control units, processing units, user interface, and firmware. These biosensor systems can measure several physiological parameters such as heart rate, blood pressure, body temperature, oxygen saturation, respiration rate, and electrocardiogram. The measured parameters are communicated using a wireless or wired link. The parameters are displayed in a personal digital assistant (PDA) or a microcontroller board-based display.

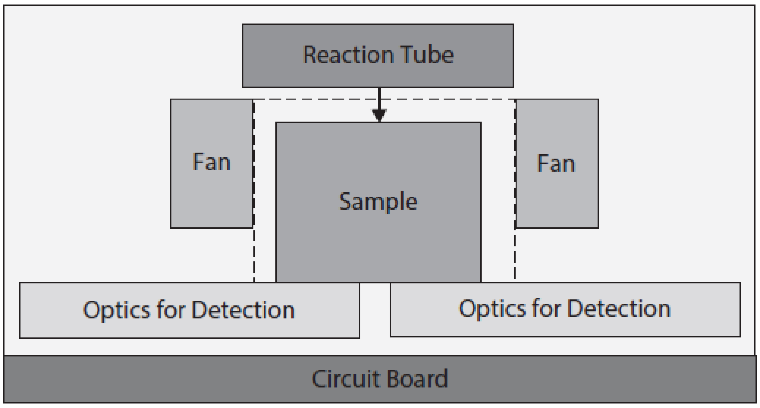
Figure 2.8 Components of a typical biosensor system [127].



2.3.3.2. DNA Detection Biosensor System with a Single Biosensor

The category of biosensors used for DNA detection is also known as biodetectors. The biodetectors are used to identify a small concentration of DNA of microorganism such as virus or bacteria. This relies on comparing sample DNA with DNA of known microorganisms, which is called probe DNA. Because the sample solution may contain only a small number of bio-organic molecules, multiple copies of the sample DNA need to be created for proper analysis. This is achieved with the help of polymerase chain reaction (PCR). PCR starts by splitting samples of double-helix DNA into two parts by heating it at about 95°C. If the reagents contain proper growth enzymes, then each of these strands will grow the complementary missing part and form a double-helix structure again. This happens when temperature is lowered. In one heating/cooling cycle, the amount of sample DNA is doubled (one cycle time is about 1 minute). Thus, for *n* cycles, 2^n copies are made. Twenty-five to 40 cycles are needed to produce approximately 1 billion copies. This amount is sufficient enough to be detected optically. With the use of fluorescent DNA probes, the identification of DNA is also possible while copying DNA in PCR. PCR is very power-consuming because of successive heating/cooling cycles that take about 30 minutes. Hence, it was previously not possible to fabricate portable battery-operated biodetectors that can do PCR. But, by using micro-electro-mechanical system (MEMS), such kinds of biodetectors, which are basically lab-on-a-chip systems, have been developed. In these MEMS-based devices, the amount of reagent used is scaled down. Figure 2.9 shows a microfluidic device [45, 130]. This lab-on-a-chip system contains channels, valves, and chambers [56].

Figure 2.9 Biodetector designed as a microfluidic device [45, 130].



2.4. Blu-Ray Player

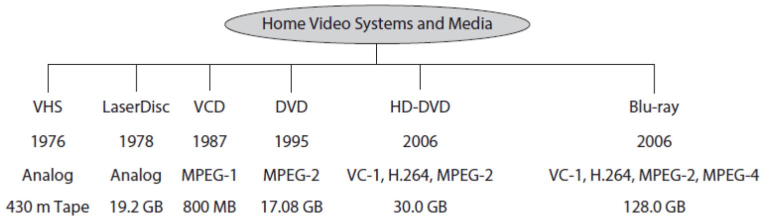
2.4.1. What Is It?

Blu-ray players are the players that can play the Blu-ray disc (BD; and other old formats such as DVD) along with online content streaming. The name Blu-ray is derived from the underlying technology, which utilizes a (blue-)violet laser to read and/or write data. The name comes from "Blue" (blue-violet laser) and "Ray" (optical ray) [2, 17]. The BD format was developed by the Blu-ray Disc Association (BDA), a large group of leading consumer electronics, personal computer, and media manufacturers [17].

2.4.2. Home Video Systems Background: From Video Cassette Player to Blu-Ray Player

The first popular home video system, which is abbreviated as VHS, was introduced in 1976. The first commercial optical home video disc storage medium known as the LaserDisc (LD) was introduced in 1978. In 1978, the video compact disc (VCD), which was digital video recorded on a compact disc (CD), came to market. This could support only low-resolution Motion Picture Export Group-1 (MPEG-1). In 1995, the digital video disc (DVD) started the era of high-quality video. DVD discs could store much more information than CDs while having the same dimensions. The high-quality video further improved to high-definition DVD (called HD-DVD) and the corresponding HD-DVD player was invented in 2006. The Blu-ray player was officially released in 2006 and emerged as a successor of the HD-DVD [17, 41]. This is known to be supporting the full-HD resolution. The various home video media and systems are listed in Fig. 2.10. In addition, recently, ultra-HD resolution TVs, media, and media players, which support much higher resolution than full HD, have started entering the market.

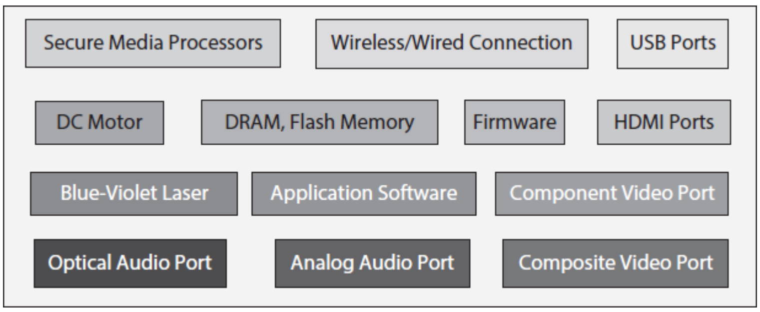
Figure 2.10 Different types of home videos discs with the supported format and maximum size.



2.4.3. What Is Inside?

The various components of a typical Blu-ray player are shown inFig. 2.11. The most important and unique component of a Blu-ray player is the "Secure Media Processor (SMP)." It is a high-performance and low-power chip designed using system-on-a-chip (SoC) technology. In addition, a wide variety of digital rights management (DRM) and Conditional Access (CA) solutions are supported in it [34]. The processor supports a large number of video and audio codec including H.264, MPEG-4, DTS, Dolby Digital. The Blu-ray player supports different ports including a high-definition multimedia interface (HDMI) port for full HD, i.e., 1080p display. The "Wireless/Wired Connections" is used by the player for streaming of the online contents in the player using the "Application Software."

Figure 2.11 Different components of a Blu-ray player.



2.5. Drug-Delivery Nano-Electro-Mechanical Systems

2.5.1. What Is It?

Drug-delivery nano-electro-mechanical systems (DDNEMS) are implantable drug-delivery systems designed using NEMS. The function of DDNEMS is to administer drugs in predetermined targets and doses using implantable chips that are controlled or programmed externally through an RF interface. These can be visualized as "bioactuators" that are complementary to "biosensors" in terms of functionality.

2.5.2. Background

There has always been a strong interest in improving the quality of human life and increasing life expectancy. This has led to multifold research and development in the area of self-health management and care giving. Efficient and reliable drug delivery is an effort in this direction. Drug delivery is the process of administering a pharmaceutical compound to achieve a therapeutic effect in living beings [95]. The type and variety of drug delivery systems are as many in number as the number of diseases. Thus, a comprehensive classification is difficult and beyond the scope of mixed-signal system design. The drug delivery systems can either be passive or active in nature.

In 1970, the first drug delivery system was introduced that was based on lactic acid polymers [78, 100, 149]. Since then, various drug delivery systems, such as insulin pump, self-adhesive skin patch, and sublingual drop, have been developed. The field of controlled drug delivery uses mechanisms such as transdermal patches, polymer implants, bioadhesive systems, and microencapsulation [100]. Conventional controlled-release formulations are designed to deliver drugs at a predetermined, preferably constant rate. Most of the conventional drug delivery schemes suffer from drawbacks that can seriously limit their effectiveness in the area of self-health management. The drawbacks of the conventional drug delivery system include the following [21, 140, 150, 154]:

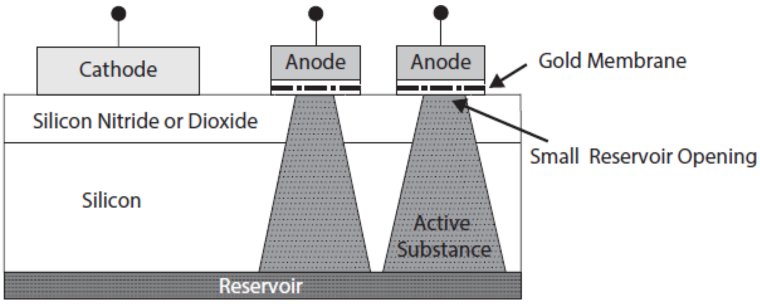
1. Drug release rate typically decreases exponentially with time.
2. Effective long-term treatment is difficult and costly.
3. Over-dosage and under-dosage.
4. It may take a long time to inject the drug, hence diminishing its effect.
5. A narrow therapeutic window.
6. A complex dosage schedule.
7. Difficult to establish individualized or emergency-based dosing regimens.

There is an urgent need to develop novel drug delivery systems that will have profound impacts on the health care industry. Future generations of the drug delivery systems are inherently expected to have a high degree of multifunctional activities. This implies that these systems, consisting of electrical, mechanical, and chemical subsystems, will be highly complex and will require a shift in design paradigm. Recent advances in nanotechnology and implantable devices suggest that it is an opportune time to framework a toolset that will enable design of future generations of drug delivery systems. They can be implemented using miniaturization technology of MEMS or more recent NEMS that are essentially microfluidic devices [56, 158]. They are called DDNEMS [115, 116]. One of the earliest attempted MEMS-based drug delivery systems is presented in [147]. NEMS are a technological solution for building miniature systems that can be deployed in small spaces [69, 70, 90, 140, 143, 154]. Such devices can be beneficial in terms of safety, efficacy, or convenience.

2.5.3. What Is Inside?

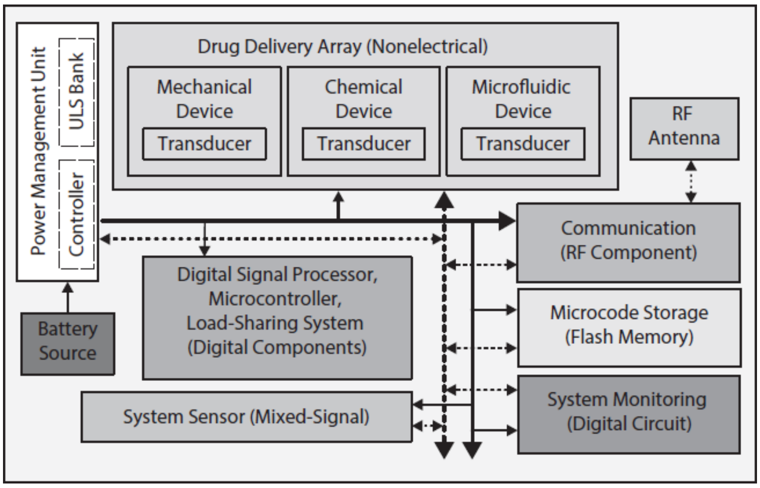
One of the earliest MEMS-based drug delivery systems is shown inFig. 2.12 [29, 100, 147]. This microchip drug reservoir contains multiple sealed compartments, which are opened on demand to deliver a dose of a drug [147]. The drug reservoirs are pyramid-shaped square holes in shape. The hole size is from 20 to 50 µm and the depth is from 200 to 500 µm. On one side, the reservoir is covered with an approximately 100-nm thick gold membrane. In total, an array of approximately 500 holes is available. The backside of the reservoirs is sealed with either biocompatible solder materials or polymers.

Figure 2.12 Microchip drug reservoir [147].



An SoC-based architecture that consists of several vital components is shown inFig. 2.13 [115, 116]. The typical components of a DDNEMS architecture are presented later. The most important and active component of the DDNEMS is the drug delivery subsystem, which is typically nonelectrical in nature (e.g., mechanical, chemical, and microfluidic). The array could be homogeneous containing all elements of the same kind or heterogeneous. The array elements may include micropumps, microfluidic devices, stents, and microneedles. The array elements also include appropriate transducers to allow their control and interfacing to the electronic portion of the DDNEMS. The data processing, controlling, and interfacing aspects of the DDNEMS are handled by electrical integrated circuit (IC) subsystems. These circuits are analog, digital, or mixed-signal in nature. The monitoring and control of the drug array elements are performed by the system sensor subsystem that receives information from and sends control signals to the transducers. Its front-end (transducer side) is analog but the back-end, interfacing to the DSP, is digital. The DSP subsystem analyzes and processes the on-line data generated by the sensors and, under the control of the program stored in the flash memory subsystem, generates control signals to affect the drug delivery, load sharing, and drug mixing. The power management unit (PMU) is one of the most important components of the entire DDNEMS. Under the control of the DSP and the stored microcode, it manages the power distribution to the various subsystems to optimize energy consumption. It has built-in timers that put the system to "sleep" or "wake-up" mode and can be induced to activate the system via external signals received by the RF subsystem (e.g., to force an emergency drug delivery). The RF subsystem, comprising an antenna and transmitter/receiver, will be built using well-established RFID principles for the shape and placement of the antenna and communication protocol. Its function is to allow noninvasive maintenance of the system, e.g., modification of the microcode stored in the flash memory. It allows remote collection of data, such as the amount of drug remaining in the reservoir, drug array element failures, and battery status. It also allows emergency drug delivery or system deactivation.

Figure 2.13 The system architecture of a DDNEMS [115, 116].

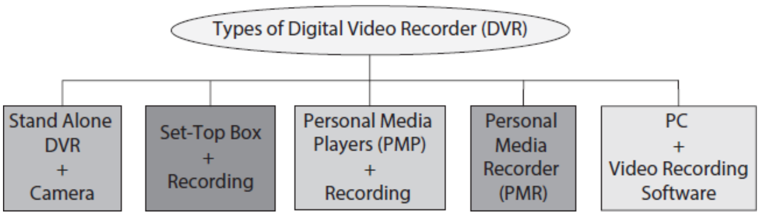


2.6. Digital Video Recorder

2.6.1. What Is It?

The digital video recorder (DVR) is a system that records digital video to enable permanent storage. The permanent (nonvolatile) memory may include hard disk, USB flash drive, secure digital (SD) memory card, or networked mass storage [141]. The DVR is also known as personal video recorder (PVR). The different types of DVR include the following (seeFig. 2.14): stand-alone DVR with camera (e.g., surveillance system), set-top boxes (STB) with recording facility, personal media players (PMP) with recording facility, personal media recorder (PMR; e.g., digital camcorder), and desktop/laptop computer containing software for video capturing and playback.

Figure 2.14 Different types of DVR or PVR.



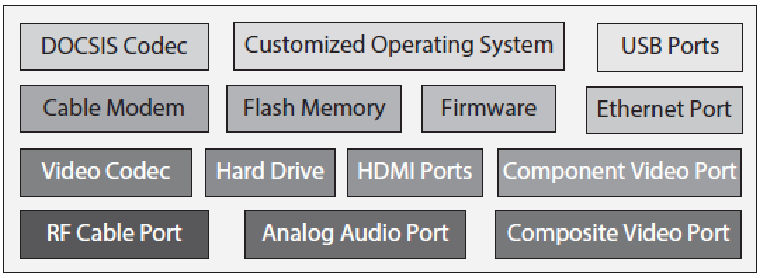
2.6.2. Background

In the beginning of 1999, consumer digital video recorders, ReplayTV [12] and TiVo [39], were launched at the Consumer Electronics Show [26]. Microsoft demonstrated a DVR unit and made it available by the end of 1999. A TV set with built-in DVR facilities was introduced by LG in 2007, and other manufacturers followed. An alternative to a stand-alone DVR is a PC-based DVR. There are several free and open-source DVR applications available for Microsoft Windows, Linux, and Mac OS-based personal computers. In Microsoft Windows, the applications include GB-PVR [3] and MediaPortal [4]. Freevo is an open-source DVR for Linux-based computers [11]. The open-source DVR called MythTV is useful for both Linux- and Mac-OS-based computers [30].

2.6.3. What Is Inside?

As evident from the discussions of the previous subsection, the DVR system is quite diverse in nature. The DVR system can be software based in a computer. The DVR can be a stand-alone system with major hardware components. The schematic representation of a stand-alone DVR is shown in Fig. 2.15. One of the main components of the DVR, the cable modem streams the data and video on demand. Data over cable service interface specifications (DOCSIS) codec is the main receiver chip, which decodes the DOCSIS and is the main network interface. The DVR has other components and ports as shown in the figure.

Figure 2.15 ***Different components of a stand-alone DVR.***



2.7. Electroencephalogram System

2.7.1. What Is It?

The electroencephalogram (EEG) is a noninvasive method for measuring brain waves of a person. EEG measures and records the electrical activity of the brain over a desired period of time [99, 133]. In an EEG, special electrodes are attached to the head and hooked by wires to a computer. The computer records electrical activity of the brain. An EEG can detect certain conditions, such as seizures in the brain, which are characterized by the changes in the normal pattern of the electrical activity. An EEG is used in a large number of fields such as epilepsy, sleep disorder diagnosis, and brain-computer interfaces [55].

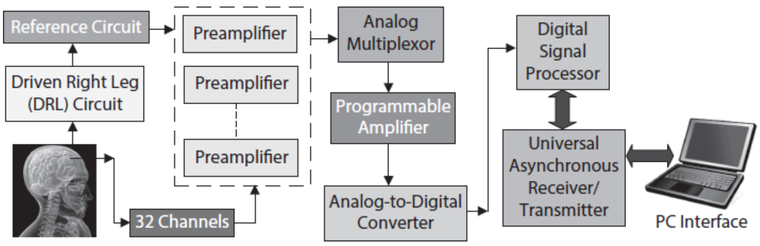
2.7.2. Background

The electrogram is derived from Electro (in Greek), i.e., electricity and gram (in Greek), i.e., measurement. The electrograms, including electrocardiogram (ECG), EEG, electrooculogram (EOG), electromyogram (EMG), and electroretinogram (ERG), are used to measure physical and cognitive function for diagnosis and monitoring of health [133]. Electrograms are thus very crucial for effective health care.

2.7.3. What Is Inside?

In an EEG, the neurophysiological electrical activity is measured in the brain using the electrodes placed on the scalp, subdurally, or in the cerebral cortex. The resulting voltage signal, which is the EEG, is the summation of postsynaptic potentials from a large number of neurons. The basic idea is that when the wave of ions reaches the electrodes on the scalp, they can move electrons on the metal electrodes that are measured as a voltage. These voltages when recorded over time represent the EEG. A block diagrammatic representation of an EEG system is shown in Fig. 2.16 [151].

Figure 2.16 Block diagram of a EEG [151].



In the EEG system presented above, 32 channels with single- or dual-pole measurements are included [151]. The driven right leg (DRL) circuit is connected to a reference (REF) circuit to provide the desired common-mode gain. DRL circuit is a biological signal amplifier that reduces common-mode interference by actively canceling the interference. As the common-mode noise voltage of the human body is much higher than the EEG signals, the preamplifier is used to measure the EEG signals by offsetting the common-mode signals. The EEG signals are of different frequencies, thus needing an adjustable amplifier and filter. An ADC provides DC voltages for further processing. The signal is then processed through DSP to reduce the occurrence of error and to achieve better measurement results. The universal asynchronous receiver/transmitter (UART) is used to interface with a PC for visual display and recording.

2.8. GPS Navigation Device

2.8.1. What Is It?

Overall, the GPS consists of three basic components [5]:

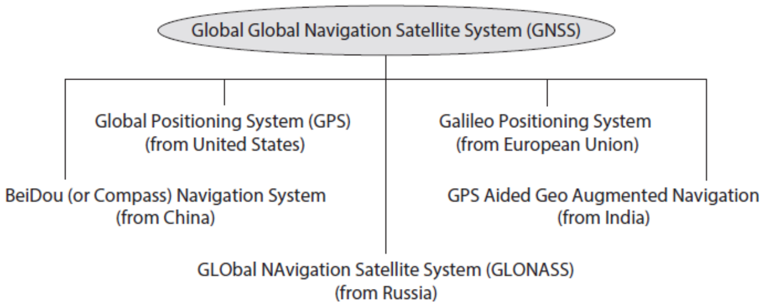
1. Space component such as satellites.
2. Control component such as control stations.
3. User-end component such as GPS receivers.

The space component of the GPS consists of at least 24 satellites. The control components are monitoring stations at different parts of the globe that are set up for monitoring the satellites. A GPS navigation device, or GPS device, is any device that receives GPS signals to determine its current position on the earth [159]. The modern GPS devices are able to find much more information, e.g., paths or roads for travel, safer or faster routes for travel, and nearby gas stations and hotels.

2.8.2. Background

Autonomous geo-spatial positioning has been of tremendous importance for a quite long time. During World War II, ground-based radio navigation systems, such as LORAN and the Decca Navigator, were developed. In 1960, the first satellite navigation system, Transit, was used by the US Navy. In 1967, the US Navy developed the Timation satellite that proved the ability to place accurate atomic clocks in space. Different types of Global Navigation Satellite System (GNSS) are presented in Fig. 2.17. In the 1970s, the first worldwide radio navigation system, the Omega Navigation System, was developed. In 1994, the US GPS became the only fully operational GNSS. Though GPS is a commonly used term, it is accurately described as Navigation System for Timing and Ranging (NAVSTAR) [5, 66]. In 2007, GLObal NAvigation Satellite System (GLONASS) of Russia became available for civilian use. The BeiDou (or Compass) Navigation System of China is in its initial phase of covering the entire globe. The Galileo positioning system from the European Union is in its initial deployment phase too. GAGAN, which stands for GPS-Aided Geo-Augmented Navigation or GPS and Geo-Augmented Navigation, is the system under development by India. *Gagan* is the Hindi word of Sankrit origin for *sky*. GPS receivers or GPS navigation devices that capture GPS signals are integral parts of mobile phones, notebooks, automobiles, ships, aircrafts, and so on.

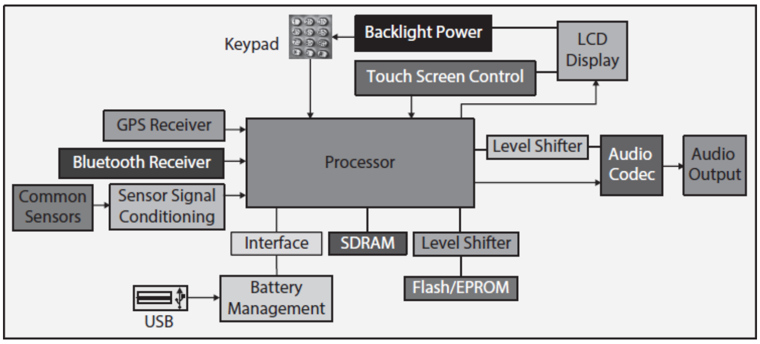
Figure 2.17 Different GNSS.



2.8.3. What Is Inside?

The schematic representation of a GPS receiver device is shown in Fig. 2.18 [84, 159]. The overall AMS-SoC of the GPS device is quite complex as it consists of analog, digital, RF, firmware, and software components. Several communication components including GPS receiver, Bluetooth receiver, frequency-modulation (FM) transmitter/receiver, and wireless local area network (WLAN) technology (WiFi) receiver are integral parts of GPS device. The digital processor is typically an enhanced advanced RISC machines (ARM)-based architecture mobile entertainment application-specific processor. The GPS AMS-SoC has many sensors including altimeter, humidity, temperature, Gyro, and accelerometers to calculate position. Audio features such as music players are integrated entertainment applications. Special DC-to-DC converters with advanced dynamic voltage scaling meet the needs of the newest processors. Touchscreen LCD or light-emitting diode (LED) display with electrostatic discharge (ESD) protection is the key user interface. Phase-locked loop (PLL)-based programmable clock synthesizers generate multiple clocks from a single input frequency. Firmware and software ensure the control of the components and user interfacing. The GPS receiver has a built-in map stored in a flash or magnetic drive.

Figure 2.18 Different components of GPS portable navigation devices (GPND) [84, 159].



2.9. GPU-CPU Hybrid System

2.9.1. What Is It?

The GPU-CPU hybrid (GCH) system is still at its early stage of full-fledged realization for common use. The GCH system is a system that uses GPU and CPU together in a heterogeneous coprocessing computing model (see Fig. 2.19) [1]. In this system, the sequential parts of the applications run on the CPU and the computationally intensive parts are accelerated by the GPU. This model is followed by applications such as medical imaging and electromagnetics due to excellent floating point performance in GPUs. This model is also used in mini home theater PCs that uses a high-end GPU for the high-definition video processing (its target application) and a low-end CPU for holding the operating system. However, with the emergence of nanoscale complementary metal oxide semiconductor (CMOS) technology and billion transistor packing era, it has been possible to make chips using the wafer-scale integration that has both CPU and GPU. For example, Intel i7 Sandy Bridge chip contains both CPU and GPU (see Fig. 2.20) [25].

Figure 2.19 GCH multicore system for high-performance computing [1].

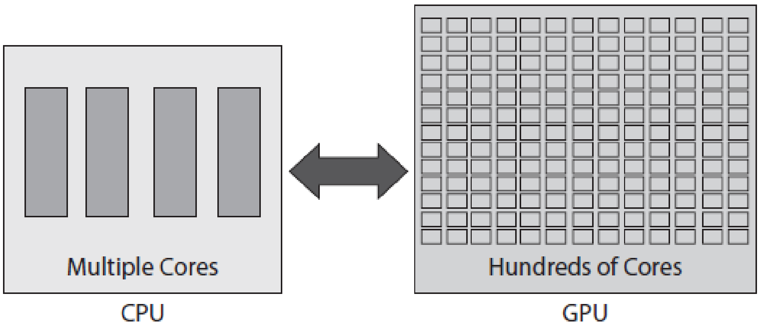
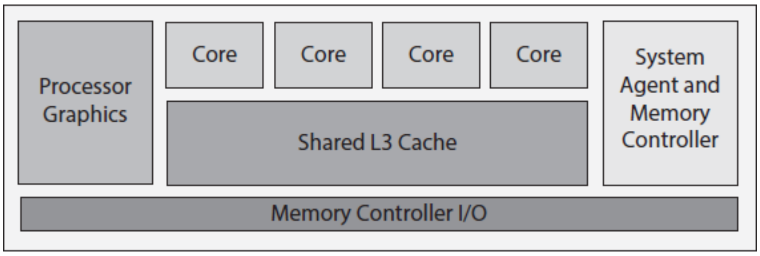


Figure 2.20 Schematic representation of a chip that has both GPU and CPU in one die [25].



2.9.2. Background

High-quality display has been one of the desired and routine operations of a typical computing device. However, the graphic processing through general-purpose microprocessor has been quite slow, which was affecting the overall system performance. In 1991, ATI introduced its product, the Mach8, which performed the process of graphics without the CPU. In 1999, NVIDIA marketed GeForce 256 as "the world's first Graphics Processing Unit (GPU)." In 2002, ATI used the term "Visual Processing Unit (VPU)" while releasing Radeon 9700. However, GPU is a more widely used term [1, 71]. A GPU (or VPU) is a special-purpose processor that performs the graphics rendering without the use of CPU or central microprocessor. The GPUs are designed to perform a specific number of operations on large amounts of data [71, 146]. The GPUs are an integral part of embedded systems, mobile phones, personal computers, workstations, and game consoles. The GPU is either part of the graphics card or part of the motherboard or chip set.

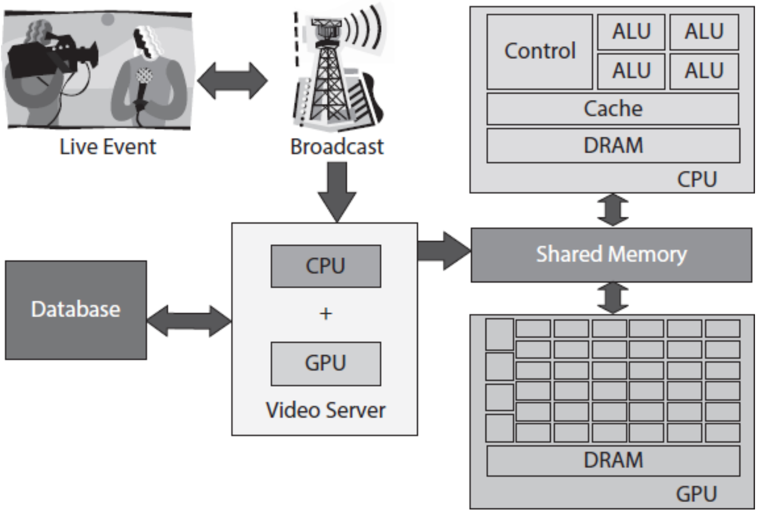
The complexity of GPUs is increasing at an extraordinary rate. The GPU IC consists of a couple of billion nanoscale transistors. The performance of the GPUs is increasing at a higher rate. The computing power of the GPUs is increasing much faster than Moore's law. The performance gap of GPU and CPU is widening. The GeForceFX 5900 GPU operating at 20 GigaFlopsis is equivalent to a 10 GHz Pentium 4 processor [53]. As the GPUs are becoming faster and evolving to incorporate additional programmability, the challenge is to provide new functionality without sacrificing the performance advantage over conventional GPUs [106, 110]. GPUs use a different computational model than the classical von Neumann architecture used by the CPUs [125]. In this context, the question that arises is whether the GPU and CPU of a desktop computer can be used together for high-performance and low-cost computing [1, 106, 110].

2.9.3. What Is Inside?

2.9.3.1. A GPU-CPU Architecture

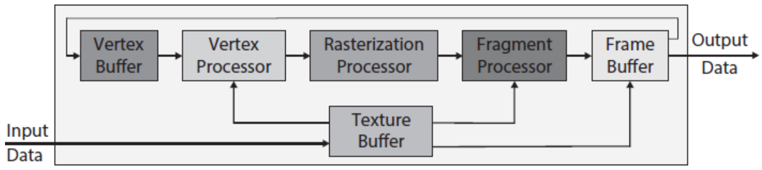
A GCH architecture in the context of digital video broadcasting (DVB), which is a far more computationally intensive application, is shown in Fig. 2.21. In this application, a server containing GPU and CPU performs tasks, such as video compression/decompression (e.g., MPEG-4 and H.264) and DRM. In one working model of the GPU-CPU–based video processing, the video data that arrives at shared memory is directed by the CPU and sent to the GPU, which is then mapped into GPU memory. The GPU processes the video data. After the GPU completes the processing, the control from the CPU initiates copying the data back to the CPU, and the video is then stored in a database. This GPU-CPU coprocessing approach ensures faster video processing for vast amounts of data and will not add extra hardware cost to either video providers or receivers. The video data is sent to the GPU as textures; in other words, the video data is treated as a group of pictures.

Figure 2.21 The IP-TV broadcasting scenario showing the shared architecture for GPU-CPU multicore processing in a video server [1, 106, 110].



In order to get a detailed perspective of high-performance capability of the GPU, a block diagram of a modern programmable GPU is shown in Fig. 2.22 [71, 106, 110, 125]. The GPU architecture offers a large degree of parallelism at a relatively low cost through the well-known vector-processing model known as single instruction, multiple data (SIMD). A GPU includes two types of processing units: vertex and pixel (or fragment) processors. The programmable vertex and fragment processors execute a user-defined assembly-level program having four-way SIMD instructions. The vertex processor performs mathematical operations that transform a vertex into a screen position. This result is then pipelined to the pixel or fragment processor that performs the texturing operations.

Figure 2.22 The programmable graphics pipeline [106, 110].



2.9.3.2. Theoretical Speed-Up Using GPU-CPU Hybrid

The overall best performance can be achieved when both GPU and CPU work together and complete the execution at the same time so that both are available at the same time for other computations. For GPU-CPU as multicore architecture, the following relationship can be derived [106, 110]. Let us assume the following: T_{CPU}, CPU execution time; T_{GPU}, GPU execution time; α, ratio of execution time of GPU and CPU; P, total number of primitive operation in an algorithm; β, a fraction; and Q, the penalty due to Amadahl's law in terms of number of primitive operations due to parallel execution of GPU and CPU. The throughput of a GPU is higher than that of the CPU due to long pipelining of the GPU. However, the execution time of GPU is lower than CPU, thus, $\alpha < 1$. So, for best hybrid system performance with GPU-CPU multicore, the following relation must be satisfied [106, 110]:

$$\alpha = \left(\frac{T_{\mathrm{GPU}}}{T_{\mathrm{CPU}}}\right)$$

(2.1)

$$\beta \times (P+Q) \times T_{\mathrm{GPU}} = (1-\beta) \times (P+Q) \times T_{\mathrm{CPU}}$$

(2.2)

Algebraically, the following relation can be deduced:

$$\beta = \left(\frac{1}{1+\alpha}\right)$$

(2.3)

Thus, the algorithm of an application needs to be partitioned to $\left(\frac{1}{1+\alpha}\right)$ and $\left(\frac{\alpha}{1+\alpha}\right)$ primitive operations to run in GPU and CPU, respectively, for optimal hybrid system performance.

For experimental analysis, a case study is performed for the following: (1) using CPU only, (2) using GPU only, and (3) using both GPU and CPU [106, 110]. The simulation environment computes 100 iterations of discrete cosine transformation (DCT). In the experimental setup, the CPU is a Pentium 4, 3.20 GHz with random access memory (RAM) of 1 GB and the GPU is NVIDIA GeForce FX 5200. The simulation results are reported in Table 2.1. The three parameters used to express results are CPU Time, GPU Time, and CPU Release Time. The CPU Time refers to the total "Elapsed Time," in the system for case (1). The GPU Time refers to the total "Elapsed Time" in the system for case (2). In case (3), these refer to the total "Elapsed Time" in the system when one half is executed by CPU and the other half by GPU. It is observed from Table 2.1 that CPU is free for more than 50% of the time when at least half of the computation is performed by the GPU. Although the computation power of GPU is much higher than CPU in terms of throughput, the fastest DCT technique on GPU is still slower than the implementation on CPU. The reason is that the speed of GPU is limited by memory access. However, the scenario may change with the use of more advanced GPU and interface.

Table 2.1 Experimental Results for Execution Time for GCH System [106, 110]

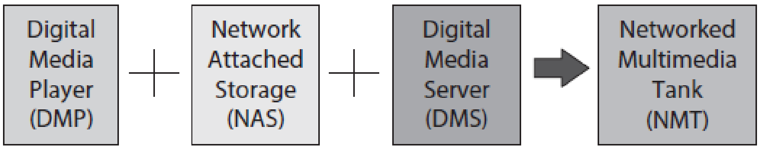
Test Cases	CPU Time	GPU Time	CPU Release Time
CPU only	4.376 ms	Free	Fully Occupied
GPU only	Free	44.789 ms	Fully Free
GPU and CPU together	2.15 ms	21.16 ms	50.87% Free

2.10. Networked Media Tank

2.10.1. What Is It?

The networked media tank (NMT) is an all-in-one network-connected media system [31]. It is a state-of-the-art integrated digital multimedia entertainment system that allows a user to play, access, store, and share digital multimedia contents in a computer network. As far as the operations are concerned, NMT is a combination of a digital media player (DMP), a network-attached storage (NAS) device, and a media server (see Fig. 2.23). The NMT allows for seamless integration among digital media, entertainment systems, and the Internet.

Figure 2.23 Conceptual representation of a NMT.



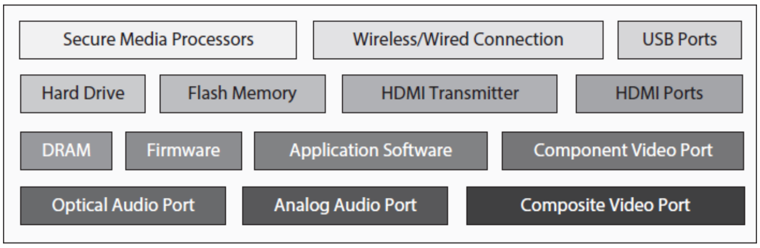
2.10.2. Background

The consumer electronics devices are no longer stand-alone, single-tasking systems like old DVD players. Selected Blu-ray players can now be connected to the Internet for streaming video. One key development in the consumer electronics multimedia content player is the "Digital Media Receiver," "Media Player," "Multimedia Jukebox," "Networked Media Jukebox," or "Networked Media Tank." This device can do all the operations of DVD players and Blu-ray players in addition to their new capabilities. In some cases additional external peripherals may need to be connected. The battle among different companies for this very important consumer electronics product is in full swing. It is difficult to accurately point out who developed the first NMT. The major products include Apple TV®, Popcorn Hour® players, and WD TV® HD Media Player [54]. However, Asus® O!Play HD2 is the first to support USB 3.0. Xbox® from Microsoft® and PlayStation® from Sony®, which supports a variety of different media formats, including high-definition video, can be considered ancestors of the NMT [54].

2.10.3. What Is Inside?

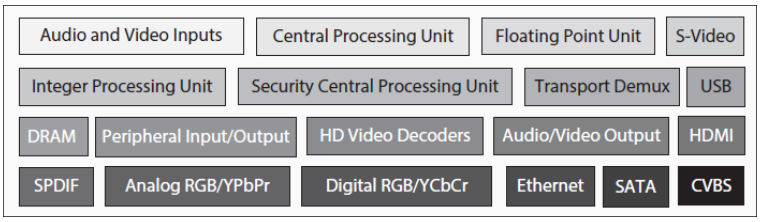
The typical components of NMT are shown in Fig. 2.24. The SMP is the most important workhorse of the NMT. This supports decoding of a wide variety of video and audio. More powerful the SMP, more the multimedia formats that the player supports. The dynamic RAM (DRAM) is quite small compared to a PC and may be spread around different parts of the motherboard supporting the chips. The HDMI transmitter enables the delivery of rich digital video and audio content.

Figure 2.24 The schematic representation of a NMT.



The architecture of a typical SMP is shown in Fig. 2.25. The high-definition video decoders handle the decoding needed to play the compressed video in real time. At the same time, audio decoder handles the audio portion of the multimedia. The security processor handles several decryption algorithms.

Figure 2.25 Architecture of SMP [67].

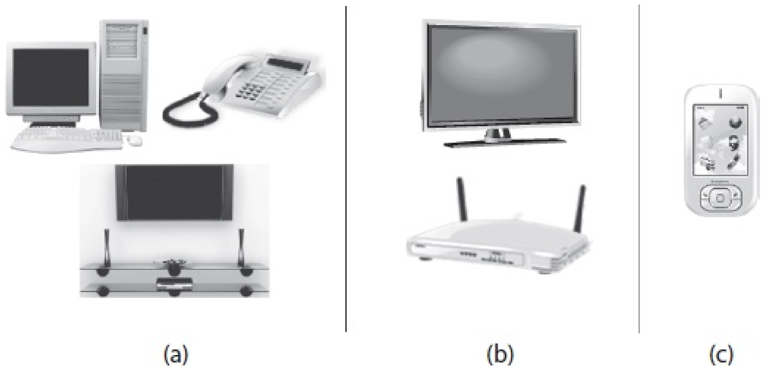


2.11. Net-Centric Multimedia Processor

2.11.1. What Is It?

The NMP is a SoC that performs Internet Protocol (IP) packet processing, video processing, and DRM without using the main CPU [107, 116, 144]. This is essentially possible due to hardware-amenable DRM algorithms, efficient architectures for net-centric operations, and their efficient VLSI implementation. To understand the application perspective of NMP see Fig. 2.26. The major motivation is its use in DVB over an IP network, the IP-TV service. Figure 2.26(a) shows the existing and widely used scenario in which three different bills are paid for three different appliances, and overall a high-energy bill. Figure 2.26(b) shows the future broadband Internet scenario using the NMP in which one bill and one appliance is used. Figure 2.26(c) shows the portable mobile TV application, which can also have similar applications as Fig. 2.26(b) in which battery life is a crucial constraint of the system, demanding energy-efficient solutions [6]. The major advantage of merging digital TV transmission and IP network technologies in a common framework is that accessibility will be provided in a single box. Transmission of digital TV signals through the IP network will potentially provide several advantages, such as better quality of service (QoS), low cost, and single (low) energy bill. The NMP is still in the conceptual stage [113]. The NMP can completely offload computationally intensive multimedia processing and network packet processing from the main CPU of a computer, thus making the CPU available for other applications. The NMP can be a part of line cards of common routers, network cards, STBs, smart-home gateways, or other high-speed communications devices in the IP network cloud.

Figure 2.26 Motivation for DVB over an IP network using NMP.

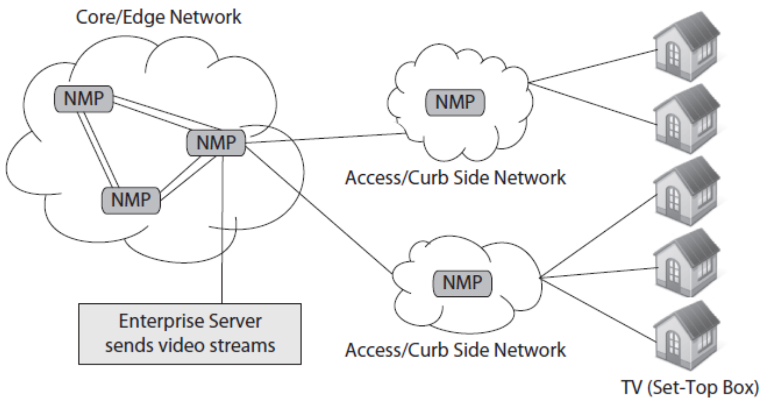


2.11.2. Background

IP-TV is a system in which digital TV services (digital video streams) are delivered to subscribing consumers using the IP over a broadband connection [43, 58, 85]. In essence, it is a service, not a protocol, which offers the traditional aggregate of a retail video product that is available on digital broadcast TV using an IP network as the transport medium as well as the platform. This, in turn, creates the potential for digital cable and satellite replacement. IP-TV requires two-way communication and therefore typically uses broadband technology over the local loop. The typical network topology is of "star" form, which is different from the traditional cable TV systems that use a ring network topology. The hub of the star, called a head end, uses a "digital subscriber line access multiplexer (DSLAM)." IP-TV needs a new STB with storage mechanisms for providing the full scope of services. Even though IP-TV is available from different vendors, several issues and challenges still need the attention of researchers. The NMP, proposed to solve the security and copyright issues, takes video streams of digital data standardized by a compressed video, processes the stream, inserts DRM attributes, and then broadcasts them. Many entertaining and educating applications, such as commercial TV, video on demand, time-shifted TV, video phones, game portals, personal digital libraries, etc., will be supported by IP-TV.

A possible deployment scenario for an NMP in an IP network cloud is shown inFig. 2.27. This figure shows a scenario by which digital video can be transported from the source to the receiver's STB while using real-time DRM through a judicious combination of encryption, scrambling, invisible-robust watermarking, and visible watermarking for video. The selective and judicious use of such DRM is needed for security, power dissipation, and real-time performance trade-offs. The NMPs at different nodes of the IP network cloud would perform different operations and may be needed to have slightly different hardware capabilities. In particular, different on-chip memory and throughput requirements may be needed at different nodes and different DRM operations. For example, NMPs in the core/edge network are different from NMPs close to access, curb, and user's home in terms of bandwidth and amount of data-processing capabilities. However, the proposed research activities intend to build a single NMP with the DRM features, on-chip memory, and throughput capability, which can be programmed or configured through the use of a firmware. This solution is expected to be cost effective for mass production. In Fig. 2.27, the enterprise server, or a particular channel, or a vendor for a certain number of channels injects the compressed video in MPEG format into the IP network via the NMP, which is maintained by the core/edge network owner. The bandwidth requirements of this NMP are in gigabits/s because the NMP processes data from several channels for each enterprise server and may process several enterprise servers at the same time. Therefore, the buffer and the queue size requirements are very high. The packets received are then processed and broadcast to the users through the IP network. The STB contains a user-end NMP. Even when a single user requests video (video on demand), it is broadcast through the network by the NMP. Once the packets reach the user, the STB splits Internet data and digital TV into two different streams so that the user can view them separately.

Figure 2.27 Deployment of the NMP for secure and copyrighted broadcasting for IP-TV.

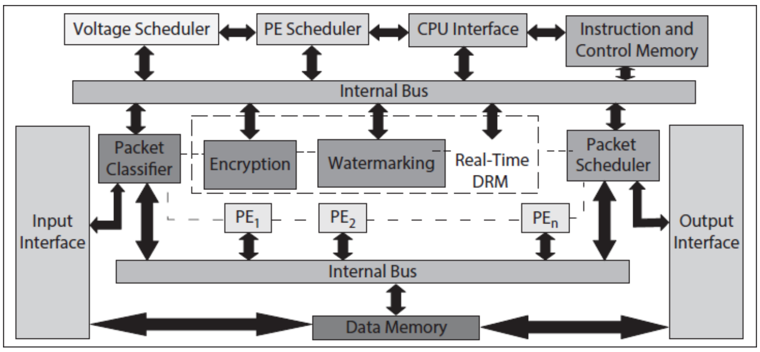


2.11.3. What Is Inside?

The architecture proposed for the NMP to be designed as a SoC is shown in Fig. 2.28. The SoC consists of several processing elements (PEs), each with dedicated operational capabilities and all of them connected through an internal bus. The internal bus forms the physical communication channel between the PEs and other components of the NMP. Packet classification is an intensive task in an NMP and is carried out by the packet classifier. It reads the header of an incoming packet, determines the stream to which the packet belongs, decides the outgoing interface using routing lookup, and passes the packet to the appropriate PE for further processing. The outgoing packet is dynamically buffered by the packet scheduler until it is sent to the outgoing link. The instruction and control memory is used to store the instructions corresponding to the program that will be executed using the NMP. The data memory is used to store or buffer the data, and an appropriate mechanism is needed to avoid data conflict among the PEs. Input and output interface are two ports through which the proposed NMP will communicate with the external environment. A brief description of some of the important units of the NMP is as follows:

1. *Packet classifier:* The design of a low-power-consuming packet classifier that performs classification in real time is needed. Such a design needs to exploit structure and characteristics of packet classification rules [92, 124].
2. *Packet scheduler:* The packet scheduler is needed to control different traffic streams and to determine the stream's quality [157]. Wide ranges of scheduling algorithms whose hardware implementation is needed for the NMP are described in the literature.
3. *PE scheduler:* The PE scheduler will activate and deactivate each PE, depending on the application requirement to be executed. The inactive PEs will be shut off with a switching mechanism to reduce standby power consumption [83].
4. *Voltage (frequency) scheduler:* It will dynamically assign the operating voltage of each PE depending on the traffic load and application requirements so that power and performance specifications are met [111].
5. *Encryption and watermarking units for real-time DRM:* These units together form the set of units to provide real-time DRM facility in the NMP [109, 112]. The sequence in which they will be used depends on the application and location of the NMP in the IP network cloud.

Figure 2.28 Architecture for the NMP to be realized as a low-power SoC [107, 113, 116, 144].

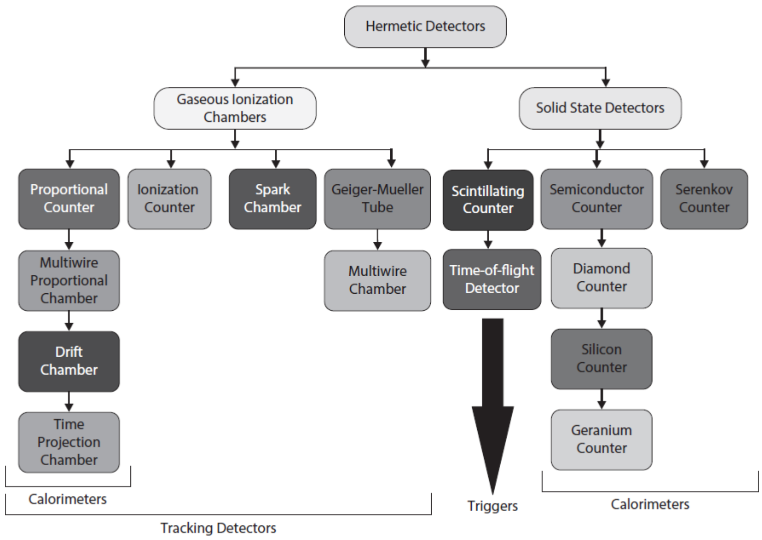


2.12. Radiation Detection System

2.12.1. What Is It?

A radiation detection system (RDS) or particle detector is a device used to detect and track high-energy particles, such as those produced by nuclear decay or cosmic radiation. If their primary purpose is radiation measurement, then they are called radiation detectors. However, for photons that are massless particles, the term *particle detector* is still correct [128]. Modern detectors are also used as calorimeters to measure the energy of the detected radiation. They may also be used to measure other attributes including momentum, spin, and charge of the particles. Detectors designed for modern accelerators are large in size and expensive. When the detector counts the particles but does not resolve its energy or ionization, the term *counter* is often used instead of *detector*. The detectors are of many types based on the different operation and application (Fig. 2.29). The ionization detectors such as gaseous ionization detectors and semiconductor detectors are more common.

***Figure 2.29** Various types of particle detectors.*



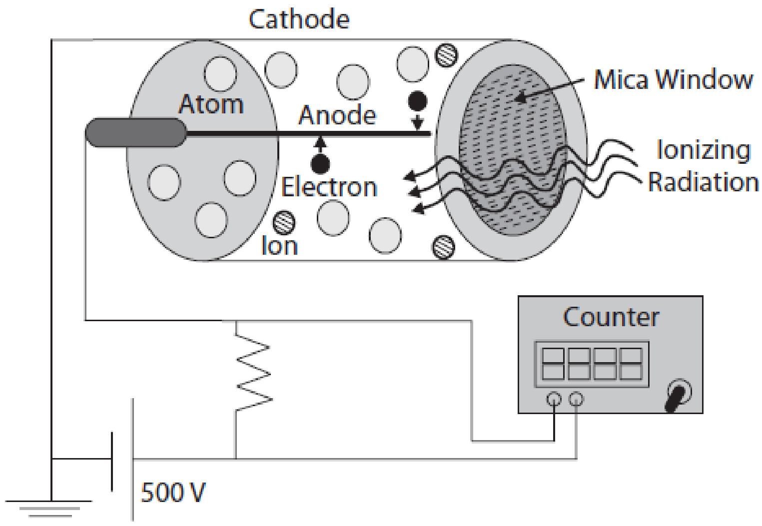
2.12.2. Background

The history of nuclear particle detectors starts way back in 1908, when Hans Geiger and Ernest Rutherford developed the Geiger counter [137]. The Geiger counter was only detecting the alpha particles; however, after undergoing several modifications, its particle detection efficiency and other features were enhanced. In 1947, the updated version of the Geiger counter that was known as the *halogen counter* was developed by Sidney H. Liebson [98]. This halogen-based Geiger counter has a much longer life and lower operating voltage than its predecessors. Currently, a widely used device called "Radiation Dosimeter" can measure exposure to ionizing radiation, such as X-rays, alpha rays, beta rays, and gamma rays [44, 49, 77].

2.12.3. What Is Inside?

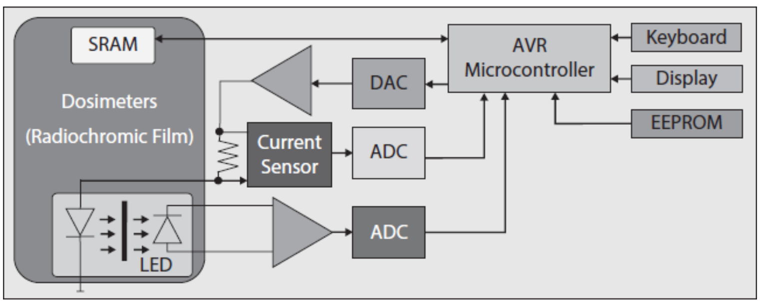
A specific and simple example of an RDS is a Geiger-Mueller counter (Fig. 2.30) [119]. In a Geiger-Mueller counter, an inert gas-filled tube briefly conducts electricity when a particle or photon of radiation makes the gas conductive. The tube amplifies this conduction by a cascade effect and generates a current pulse, which is then often displayed by a needle or lamp and/or audible sound. The inert gas used is typically helium, neon, or argon with halogens added.

Figure 2.30 Schematic representation of a basic Geiger-Mueller counter.



The schematic representation of a portable dosimeter reader is provided in Fig. 2.31 [94]. The components of a typical radiation dosimeter reader include the following: radiochromic film readout head, LED-based dosimeter readout head, SRAM socket, and electronic systems. The main component of the electronic system is the AVR microcontroller that is responsible for the user interface handling, USB interface, and control of the readout system. For an accurate measurement, the radiation dose is calculated on the basis of the ratio between light intensity of the LED before irradiation and after irradiation. In this process, the new LEDs are labeled, their light intensity is measured with the readout system, and the data is stored in the system memory. The irradiated LEDs are also read out using the same readout system. The driving circuit of the LED consists of ADC, DAC, and operational amplifier (OP-AMP). The current of LED is monitored using a current-sensing circuit and a shunt resistor. The initial value of the DAC is set by the microcontroller. The LED current measurement and the DAC setting correction are performed by the microcontroller. The voltage output of the readout circuit is proportional to the light intensity of the LEDs.

Figure 2.31 Schematic representation of dosimeter reader system [94].



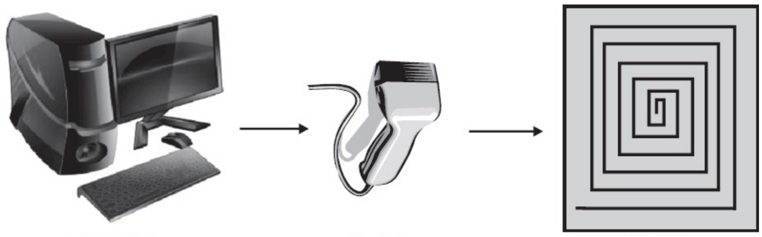
2.13. Radio Frequency Identification Chip

2.13.1. What Is It?

The RFID chip is a small microchip that performs wireless data transmission for automated identification of objects and people [33, 82, 88]. It is also known as RFID device, RFID tag, RFID transponder, smart tag, smart label, or radio barcode. The RFID tag may be present in any single product, case, pallet, or container. The cost of an RFID tag is decreasing significantly, and hence it is expected that several trillion RFID tags will be part of every consumer product. Several leading retailers around the world are in the process of evaluating the use of RFID.

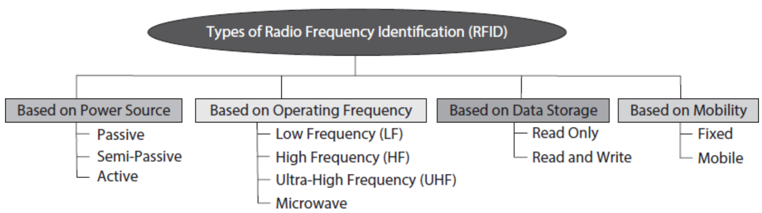
The broad concept of RFID is shown in Fig. 2.32 [82]. The crucial component of an RFID tag embedded in an item contains unique information about the item and is always ready to communicate through its antenna. The RFID reader or scanner is used to send and receive RFID data to the RFID tag as well from the RFID tag using its built-in antennas. The host computer gets the data from the RFID reader, which uses specialist RFID software to filter the data and route it to the correct applications.

Figure 2.32 Basic operations of RFID.



The RFID tags can be classified into different types based on various criteria (Fig. 2.33). Based on the source of power supply, they can be passive, semi-passive, or active [88]. The semi-passive RFID tags (a.k.a. battery-assisted passive) have a battery which is used to initiate communication when they are interrogated. The active RFID tags use batteries to initiate communication and transmissions. Depending on the operating frequency, RFID tags are low frequency (LF), high frequency (HF), or ultra-high frequency (UHF). The LF tags operate in the range of 124 to 135 kHz. The HF tags operate at 13.56 MHz. The UHF RFID tags operate in the range of 850 to 950 MHz. The microwave RFID tags operate in the range of 2.4 to 5.8 GHz. RFID tags can either be read-only or read-write type based on their data storage mode [33, 82, 88]. The read-only RFID tags are programmed with unique information stored on them during the manufacturing process that cannot be changed. The read-only RFID tag is also known as "write-once, read-many" (WORM) RFID tags [33]. The read-write RFID tags allow writing over existing information when the tag is within the range of the RFID reader. Depending on the mobility, RFID readers are classified into two different types: fixed RFID and mobile RFID. In fixed RFID, the reader reads tags in a stationary position. In mobile RFID, the reader is mobile when the reader reads tags.

Figure 2.33 Different types of RFID tags [82, 88].



2.13.2. Background

A specific type of barcode called universal product code (UPC) is widely used to identify objects. The UPC barcode was invented in 1973 [96, 97]. In 1974, the first UPC-marked object was scanned at a retail checkout (Marsh's supermarket in Troy, Ohio) [7, 122]. These are omnipresent and are used almost everywhere on the planet. However, they have several disadvantages that are as follows:

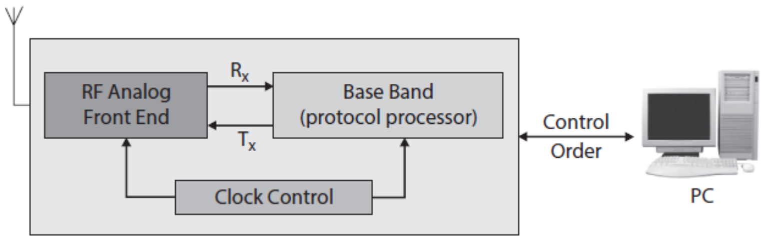
1. UPC only identifies the type of object; no other information is provided.
2. UPC is optically scanned, hence line-of-sight contact with the reader is required.
3. UPC needs careful physical positioning for reading.
4. UPC cannot provide information on the location of the item.
5. UPC reading is a slow process as only one item is scanned at a time.
6. UPC requires human intervention.

In order to overcome the above-mentioned limitations and to deploy it in diverse applications, RFID technology is being further explored. During World War II, an RFID tag was first used by Britain to identify friend and foe aircraft [82, 136]. The commercial application of RFID started during mid-1980. The RFID technology has been more widely accepted now. Applications including automated toll payment and the ignition keys in automobiles are common [88]. However, several issues involving privacy, authentication, and volume of data handling need to have advanced solutions for universal acceptability of RFID [82, 88]. An RFID tag contains a unique identification number called an electronic product code (EPC). The standardization of RFID tags is handled by EPCglobal Inc. [22, 88]. In addition to EPC, the RFID tag potentially can contain other information that is of interest to manufacturers, health care organizations, military organizations, logistics providers, retailers, and other users who need to track the physical locations of goods or equipment.

2.13.3. What Is Inside?

The simplified view of the block diagram of an RFID is shown inFig. 2.34 [155]. The RFID chip needs to be a single integrated monolithic structure; however, for clarity each component is described in this subsection [28, 50]. The RFID chip consists of an RF antenna, RF analog front end (AFE), the base band circuit, and a clock control. The antenna receives information from the RFID and also translates information to the RFID. One antenna is used for transmission and reception at the same frequency and at the same time. The AFE circuit of the RFID is responsible for transmission and reception of the RF signals. The baseband circuit is responsible for performing coding/decoding, modulation/demodulation, communication protocol, and the anticollision mechanism. The clock control circuit provides the system clock and also resets the signal. The PC is not a part of the RFID chip; it is used for communication of a user with the RFID chip.

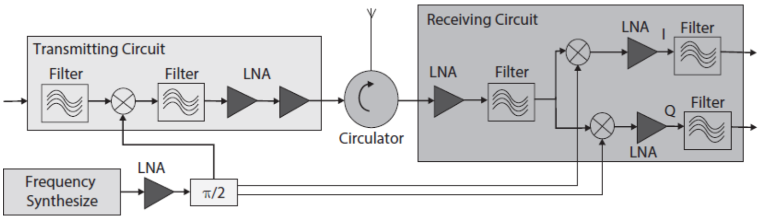
Figure 2.34 Block level representation of a RFID chip.



An RFID AFE circuit is shown in Fig. 2.35 [155]. The primary components of the AFE circuit include the following:

1. Transmission circuit.
2. Reception circuit.
3. Frequency synthesizer circuit.
4. The circulator.

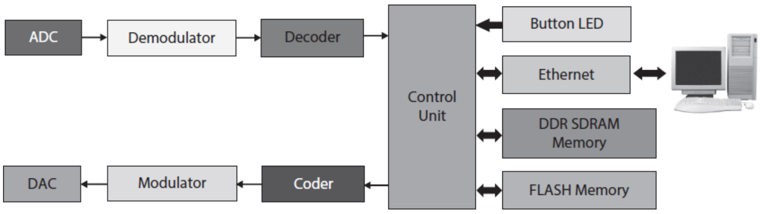
Figure 2.35 A RF AFE circuit of the RFID.



The transmission circuit is used for RF signal transmission and the reception circuit is used for receiving RF signals. The frequency synthesizer circuit is responsible for generating appropriate frequency. The circulator determines the performance of the RFID reader system. A good-quality circulator is required to isolate transceivers.

The block diagram of the baseband circuit of the RFID is shown inFig. 2.36 [155]. The baseband circuit contains various units including the coding/decoding unit, modulator/demodulator unit, DRAM, flash memory, ADC, and DAC, which are needed for managing the communication protocols.

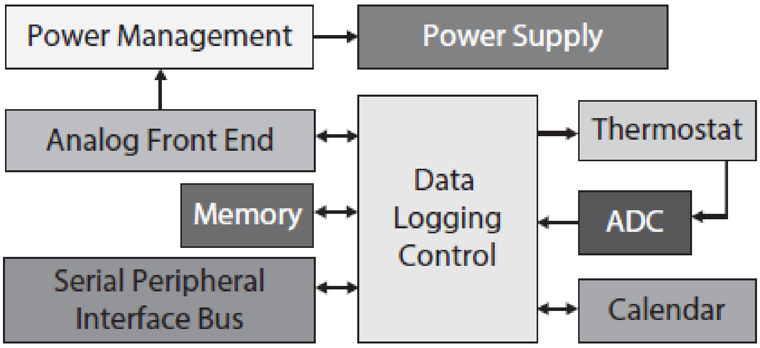
Figure 2.36 The block diagram of the baseband circuit of the RFID.



An industrial standard RFID chip is now discussed (Fig. 2.37) [28, 50]. This RFID chip can be used for various applications as follows:

1. Tracking of temperature-sensitive products.
2. Temperature monitoring of medical products.
3. Monitoring of fragile goods transportation.

Figure 2.37 *Schematic representation of structure of a RFID chip.*



The temperature sensor that is fully integrated has a maximum accuracy of 0.5°C with an operating temperate range from –20°C to 60°C. The optional external sensor can be connected through the analog sensor interface. The serial peripheral interface (SPI) is used for parameter setting and connection of other external circuits. The RFID has an on-chip 8k bit electrically erasable programmable read-only memory (EEPROM). The real-time clock is used for data logging. Data logging control coordinates the RFID chip components. The RFID chip is powered using a thin and flexible battery or electromagnetic waves from an RFID reader.

2.14. Secure Digital Camera

2.14.1. What Is It?

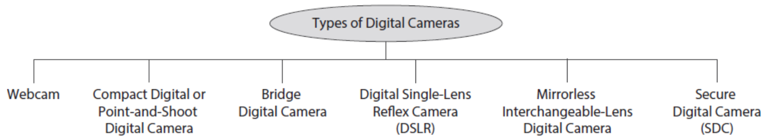
SDC is an appliance with the standard features of a digital camera and a built-in facility for real-time, low-cost, and low-power DRM and is typically designed as an SoC. SDC performs many DRM-related tasks including copyright information, extent of tampering, source of multimedia, and owner's, creator's, or camera operator's information.

2.14.2. Background

The history of photography can be traced back to the 12th century with the invention of simple glass lenses [123, 129, 142]. In 1787, the first photograph was taken by Nicephore Niepce using in-house cameras [129, 142]. In 1885, George Eastman introduced the use of photographic film. In 1888, he built the first camera called the "Kodak" [129, 142]. In 1975, a scientist from Kodak presented the world's first digital camera [20]. In 1988, Fuji DS-1P became the first true digital camera that recorded images as a computerized file in 16 MB internal memory. In 1990, Logitech Fotoman became the first commercially available digital camera that used a CCD image sensor, stored pictures digitally, and connected directly to a computer for download. In 1991, Kodak DCS-100 marked the beginning of a long line of professional Kodak DCS SLR cameras [19].

The existing digital cameras are quite diverse in terms of size, price, and capability. They can be classified into different types as shown in Fig. 2.38. The simplest type of digital cameras are the webcams that are typically compact CMOS sensors–based cameras and are used along with the computing appliances, such as PCs, PDAs, or slate-PCs, etc. Compact cameras have portable designs that are particularly suitable for casual use. Bridge digital cameras are mid-end digital cameras with a more classical single-lens reflex (SLR) look and with advanced features. Digital SLR cameras (DSLRs) are digital cameras that are based on classical SLR cameras. Mirrorless interchangeable-lens cameras are the ones that combine the larger sensors and interchangeable lenses of DSLRs with the live-preview system of compact cameras.

Figure 2.38 ***Different types of digital cameras.***

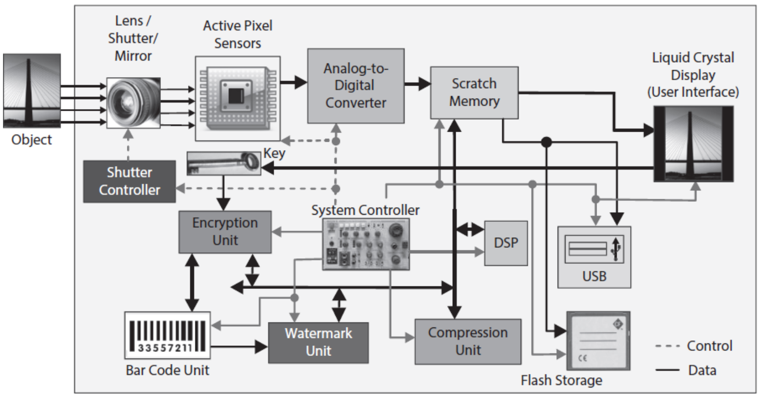


The explosive growth of the Internet has made it possible to transfer multimedia information worldwide without any effort and time. Flexibility in using digital multimedia has many issues including copyright protection and enforcement of intellectual property rights. In order to provide real-time DRM, SDC is introduced [52, 117].

2.14.3. What Is Inside?

The block-level representation of the SDC is shown in Fig. 2.39 [105, 114, 116, 118]. The system presented for SDC is in a generic context and the exact architecture depends on specific applications. The main components of the SDC include active pixel sensor (APS), LCD, memory unit (including volatile and nonvolatile), encryption unit, compression unit, bar code unit, and watermarking unit. In the SDC, the multimedia is captured by a sensor and converted to a digital signal by the ADC. While there are other alternatives, a nanoscale CMOS pixel sensor with an embedded ADC is preferred. The captured multimedia is stored temporarily in the scratch memory, after which it is displayed on the LCD panel. The multimedia is then further transmitted over the network or transferred to flash memory, a computer hard drive, or optical discs. The flash memory is a nonvolatile memory used for permanent storage of multimedia in SDC. The controller unit is responsible for controlling the entire sequence of events. The invisible-robust, visible watermarking algorithms are used along with encryption and data compression for different purposes. The choice of operations performed on the multimedia depends on the user of the SDC.

Figure 2.39 Block-level representation of an SDC [114, 116].



2.15. Set-Top Box

2.15.1. What Is It?

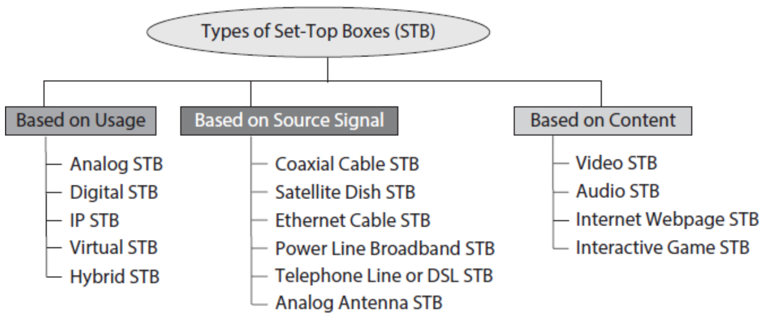
An STB is an appliance that is connected with the TV (or other similar display devices) to receive the external signal and to display the signal content [59, 79]. STBs receive and select broadcast signals, decode and decompress the signals, and convert them into a format that can be displayed by the end-user devices. It is also known as a set-top unit (STU).

2.15.2. Background

In the 1980s, the use of the cable converter box marked the beginning of the STB for TV and other display devices [9]. The cable converter box received the additional analog cable TV channels and converted them to frequencies that could be seen on a regular TV, thus bringing cable TV to the masses. These boxes could be used to shift one selected channel to a low-range very high frequency (VHF). In the mid-1990s, the digital STBs were introduced. These STBs could be used to descramble paid cable channels along with using interactive services such as video on demand, pay per view, and home shopping through TV.

The STBs are of diverse types as shown in Fig. 2.40. Based on the usage, the types of STBs include analog STB, digital STB, IP STB, virtual STB, and hybrid STB. The analog STB is essentially a converter box; however, as broadcasting is mostly digital, this has now limited usage. The digital STBs are the current standard boxes used in digital TV receiving. An IP STB converts IP-TV data into a format that can be used by user-end display [27]. The virtual STB (V-STB) [75] is an application that enables specific subscription channels and packages to be viewed online that can be used with regular STB service. A hybrid STB handles DVB and IP-based video to allow users to view digital cable channels and Internet videos from an IP network.

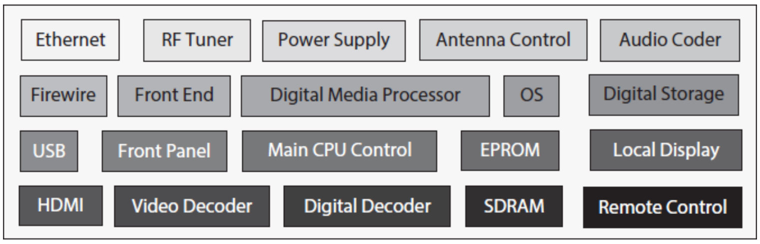
***Figure 2.40** Different types of STBs.*



2.15.3. What Is Inside?

The schematic representation of a typical STB is shown in Fig. 2.41 [42, 59, 79]. The main components are now briefly discussed. The "power supply" provides the voltage to run various peripherals inside an STB. The "front panel" is a small microcontroller that takes the user input and interacts with the main processor. The front panel also contains an infrared (IR) receiver to listen to remote control input. The "front end" that is a "network interface module" (NIM) has two important modules, the "tuner" and the "demodulator." The NIM is a peripheral device that interacts with the input signal source to receive the signal and provides the signal to the "digital decoder" in the form of a transport stream. The "digital decoder" receives the transport stream from the front end and then demultiplexes and decompresses. The many types of data include graphics, audio, video, and software programs. The "CPU (or processor)" takes care of interactions of all the hardware peripherals and software modules inside an STB. The operating system (OS) of the STB is different from a PC's OS in that it operates with limited memory and a low-end processor. It responds to services in real time, and is highly reliable. An STB contains various types of "memory" for different roles, including dynamic RAM (DRAM), nonvolatile RAM (NVRAM; including EEPROM and Flash), and read-only memory/one-time programmable (ROM/OTP). The most important module of STB, the "conditional access module" (CAM) is used for descrambling an encrypted signal and provides a smart card interface for various security features. The "return path" such as cable/DSL modem and Ethernet jack is used to communicate with the head end and send data packets. An STB can contain various peripherals including RS-232 port, USB port, WiFi enablers, and Bluetooth devices for enhanced interactivity and user experience.

Figure 2.41 Main components of a typical STB.



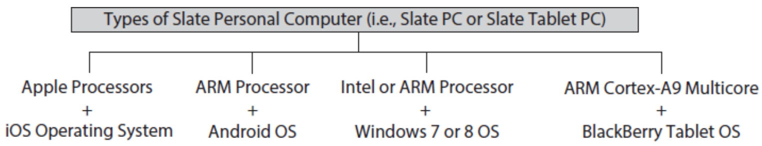
2.16. Slate Personal Computer

2.16.1. What Is It?

The slate personal computer (Slate PC), also called Slate Tablet PC, is a small form factor portable PC equipped with touchscreen as a primary input device. The Slate PC is a lighter and slimmed down PC without a dedicated physical keyboard and other extra components [48, 80]. This is different from a convertible tablet with rotating screen and a dedicated key board, the concept presented by Microsoft in 2001 [63]. The advantages of Slate PC include instant-on, ease of use, speedy operation, and wireless Ethernet.

At present, each and every semiconductor and/or consumer electronics industry has or is in the process of having a Slate or Tablet PC. They are of different form factors, processors, and mobile OS (refer to Fig. 2.42). The majority of them are based on the Android OS and ARM processor. The vast use of ARM processors can be attributed to the fact that, unlike other semiconductor companies (e.g., Intel and AMD), ARM licenses its technology as intellectual property rather than manufacturing its own. Thus, there are several companies making processors based on ARM's designs. Apple iPad has its own Apple A4/A5 custom-designed, high-performance, low-power SoC and iOS and hence has longer battery life. A few Slate PCs are in the market with some Intel processors (e.g., Intel Atom, Intel Dual-Core, Intel i3, and Intel i5) and Window 7 OS [46]. Research in Motion (RIM) and BlackBerry Tablet OS are making a Slate PC called PlayBook. Several other variants of Slate PCs are going to come in the next few years.

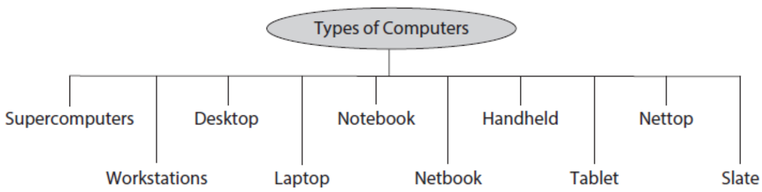
Figure 2.42 The slate PCs.



2.16.2. Background: The Developmental Trend of General-Purpose Computer Reaches Slate PC

The computer that is highly essential for automation and accurate repetitive computation is a machine that takes inputs and processes them using the predefined instructions and generates outputs. The history of automated computing starts from 3000 BC with the invention of the abacus in Babylonia [103]. With the growth of civilization and consequent increase in the demand for faster, high-performance computations, various computing machines have been tried to meet the requirements. The different forms of computing machines attempted include slide rules, mechanical calculators, analytical machines. The first digital computer, complex numerical calculator was demonstrated in Bell Laboratory in 1940. The first general purpose computer, "electronic numerical integrator and computer" (ENIAC) was made in 1946 using vacuum tubes during the World War II. The modern computer age started with invention of transistors in the Bell Laboratory in 1959. After that the computers have undergone rapid changes in speed, size, and other features. The computer's size has changed from the dimensions of square feet as big as a bedroom to the size of a palm. Various types of computers are presented in Fig. 2.43. The current personal computing devices are slate computers and tablet computers.

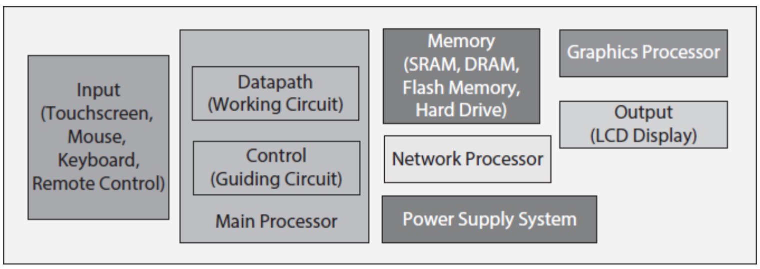
Figure 2.43 Different types of computers.



The typical components of a computer include the following (see Fig. 2.44):

1. *Input:* Touchscreen, stylus, mouse, keyboard, track ball, remote control.
2. *Memory:* Static RAM (SRAM), DRAM, flash memory, magnetic drive (a.k.a. hard disk), and optical disc.
3. *Datapath:* The main workhorse that does the computation in the computer.
4. *Control:* The intelligent portion that makes the datapath work.
5. *Output:* LCD monitor, CRT monitor, and Digital TV display.

Figure 2.44 Typical components of a computer.

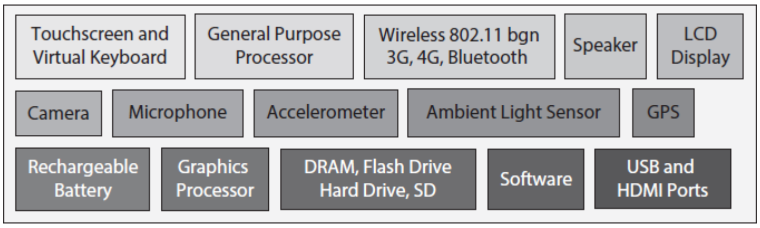


Both datapath and control together are called "central processing unit" (CPU), or processor. A "microprocessor" is a CPU on a single chip [62]. In 1971, the first microprocessor Intel 4004 was built with only 2300 transistors. In 1993, the Pentium processor with 3.1 million transistors was a major milestone, and now microprocessors are available with billions of transistors.

2.16.3. What Is Inside?

There are several variants of the slate PC tablet that have been designed keeping in mind the target cost and market share. Besides some common features such as touchscreen and small form factor, the components of slate PCs differ from one type to the other [46]. The typical components of a slate PC are shown inFig. 2.45. The touchscreen and virtual keyboard are input devices [139]. The multimedia devices include camera, microphone, and speaker. The processors include general-purpose and GPU. The "accelerometers" are used to align the screen depending on the direction in which the device is held, i.e., switching between portrait and landscape modes. GPS is built-in to have a navigation system. DRAM, solid state flash drive, SD expandable drive, and magnetic hard drive are various types of memory devices used in the slate PC. The network connectivity includes wireless 802.11 b/g/n, cellular 3G/4G, and Bluetooth. Ambient light sensors are used in the slate PCs for adjusting the brightness of the screen based on the environment. USB and HDMI ports are used for data transfer in the slate PC. An LCD (which is also the input for touchscreen) is also the main output of the slate PC. One rechargeable battery is a lithium polymer battery that provides very good operation life to the slate PC [61].

Figure 2.45 ***Typical components of a slate PC.***



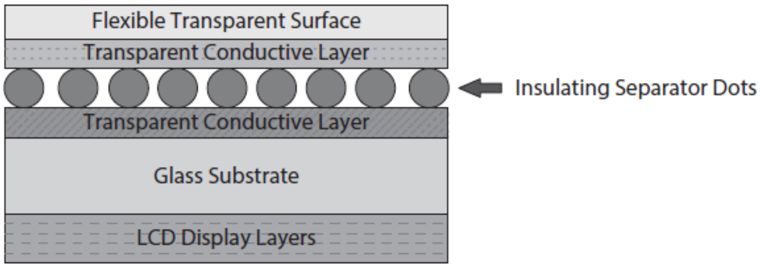
The unique aspect of the slate PC is the touchscreen input [139, 153]. There are two key aspects of a touchscreen:

1. Sensing methodology to sense the touching of the LCD.
2. Special construction of the LCD screen compared to a regular LCD screen.

The above two are related on the basis of the type of sensing method on which the LCD has to be constructed. Typical sensors and circuitry are used to monitor changes in a particular state, e.g., to monitor changes in electrical current. This can be performed by capacitive and resistive approaches. In addition, the touchscreen following the capacitive or resistive approaches have the following layers (see Fig. 2.46):

1. Layer 1: Flexible transparent surface layer.
2. Layer 2: Transparent metallic conductive coating on the bottom of layer 1.
3. Layer 3: Adhesive spacer consisting of nonconducting separator dots.
4. Layer 4: A transparent metallic conductive coating on the top of layer 5 below.
5. Layer 5: Glass substrate.
6. Layer 6: Adhesive layer on the backside of the glass for mounting.
7. Layer 7: LCD layers.

Figure 2.46 Schematic representation of construction of a touchscreen of a slate PC.



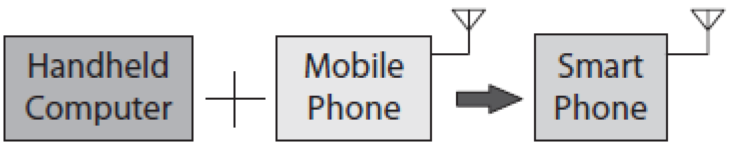
The capacitive touchscreens use a capacitive material layer to hold an electrical charge that is initiated by touching the screen at a specific point of contact. In resistive touchscreens, the pressure from touching causes conductive and resistive layers of circuitry to touch that changes the circuit resistance.

2.17. Smart Mobile Phone

2.17.1. What Is It?

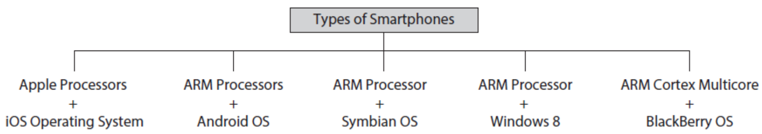
The smartphone can be conceptualized as a handheld computer integrated with a mobile phone as presented in Fig. 2.47. The smartphones allow the users to install new applications as new applications are made available in the market. Smartphones may contain complete operating systems that provide platforms for application developers and high-end users.

Figure 2.47 The concept of smart phones.



As the market for smartphones is huge, various kinds of these devices are available. The semiconductor houses, IC design industries, and software companies are coming together to get a share of this ever-growing market. At high-level, the smartphones can be grouped into various types as presented in Fig. 2.48 [35]. Many hardware and software combinations build different smartphones with diverse capabilities [120]. The primary processors in the smartphone include different types of ARM processors, Apple custom SoC processors, and Qualcomm processors. The main operating systems include Apple iOS, Android OS, Symbian OS, and Windows Phone.

Figure 2.48 Different types of smart phones.



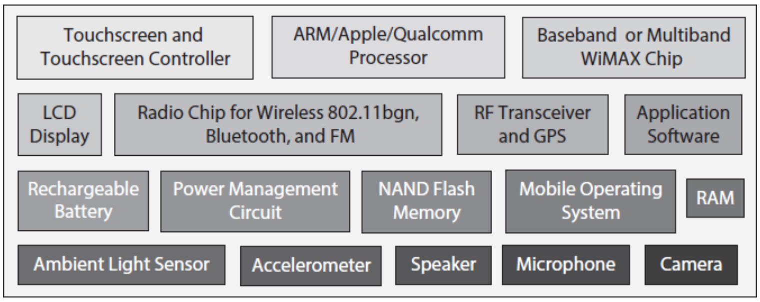
2.17.2. Background

Invention of the telephone by Alexander Graham Bell in 1876 started the age of long-distance speech communication. In 1973, Martin Cooper of Motorola presented the first mobile phone. A mobile phone, which is also called mobile, cellular telephone, or cell phone, is used to make mobile telephone calls across a wide geographic area unlike regular corded or cordless phones. Since then the development of mobile phones is in progress on a competitive basis. The current generation of mobile phones are smartphones that have more advanced computing ability, applications, and connectivity than a regular mobile phone.

2.17.3. What Is Inside?

The different components of a typical smartphone are shown in Fig. 2.49. The touchscreen and the LCD display are essentially the typical user input/output interface of the smart phone. The touchscreen uses the similar technology as in the case of the slate PC. The processors are variants of ARM core. Other processors that are either custom built or built on the basis of an ARM core can be present. The WiMAX chip that supports mobile WiMAX baseband and three frequency bands—2.3–2.4 GHz, 2.5–2.7 GHz, and 3.3–3.8 GHz—is an important component of the smartphone. The radio chip has functionality like 802.11n WiFi, Bluetooth, and FM. An RF transceiver with GPS is an integral part of smartphones. The Li-ion rechargeable battery with a power management unit provides power to the components. The smartphone system has NAND Flash for permanent storage of data and volatile RAM to be used by the processors. The ambient light sensor adjusts the brightness of the display based on the environment and disables the touchscreen when it is held close to the ear. The accelerometer aligns the smartphone in a portrait or a landscape orientation based on the direction of the device. A speaker and microphone are built-in audio devices in a smartphone. There are two cameras, comprising low-power-consuming CMOS sensors, in a smartphone, one in front and one in back, to facilitate video conferencing. The mobile operating systems coordinate the processing of the different components. Application software is available in large numbers depending on the OS of the smartphone.

Figure 2.49 The typical components of a smart phone.

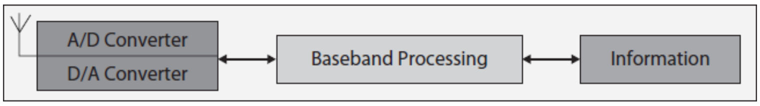


2.18. Software-Defined Radio

2.18.1. What Is It?

A software-defined radio (SDR) system, or simply SDR, is a set of hardware and software components that constitute a reconfigurable system for wireless communication [36, 38, 65, 68, 89, 156]. In an ideal scenario, the SDR consists of a wideband antenna, wideband ADC, wideband DAC, and a programmable processor (Fig. 2.50) [148]. SDR is an efficient multimode, multiband, multifunctional communications system that can be enhanced using software upgrades. The SDR essentially leads to universal radio terminals (URTs) while allocating as many hardware functions as possible to software.

Figure 2.50 The system architecture of an ideal SDR.



2.18.2. Background

In 1984, the term "software radio" was coined by the Garland Texas Division of E-Systems Inc. that is now known as Raytheon Company [8, 87]. This "software radio" consisted of a digital baseband receiver of thousands of adaptive filter taps using multiple array processors accessing shared memory that provided programmable interference cancellation and demodulation for broadband signals. In 1991, the term "Software Defined Radio" was coined [101, 102]. By performing as many large portions as possible of radio functions in a software, the SDR presents many advantages over specialized hardware approaches:

1. SDR has the ability to receive and transmit different modulation schemes using a common set of hardware.
2. SDR has the possibility of adaptively choosing an operating frequency and a mode best suited for prevailing conditions.
3. SDR is fully field upgradeable and extensible as better controlling software becomes available.
4. SDR provides the opportunity to recognize and avoid interference with other communications channels.
5. SDR becomes the basis of the next generation of mobile communications, replacing a multitude of incompatible standards, thus providing true universality.
6. SDR users realize significant time and cost savings as the same device replaces a number of competing technologies and protocols.
7. SDR makes the world roaming of wireless devices become a reality.
8. SDR eliminates analog hardware and its cost that results in simplification of radio architectures and improved performance.

2.18.3. What Is Inside?

In order to give a detailed and comparative perspective of the SDR, this section starts discussions from the traditional radio. The schematic representation of the structure of a traditional and hardware-based radio system is shown in Fig. 2.51 [68]. In the traditional radio schematic, the AFE consists of a significant portion of the system and it performs the reception using an antenna and down-conversion of RF signals to intermediate frequency (IF) and then to baseband. Once the signal has been down-converted, the special-purpose hardware processes the signal. The software involved in this case is minimal. In an SDR system, a significant portion of the processing is transferred from specialized hardware to general hardware under software control. The schematic representation of the SDR is provided in Fig. 2.52. In the SDR, the entire baseband processing and even the conversion from IF to baseband is performed in the software. In a pure software radio, the majority of functions are performed by a software that has moved as close to the antenna as possible. This SDR is shown in Fig. 2.53. In this system, direct conversion from RF to baseband is performed by using software.

Figure 2.51 The structure of a conventional hardware-based radio system.

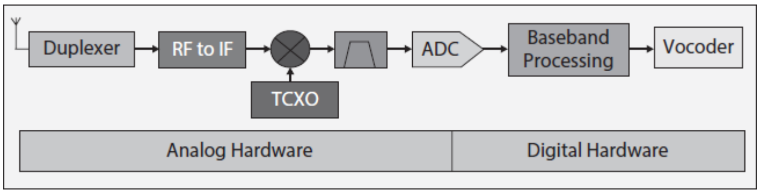


Figure 2.52 The structure of an SDR system showing a significant portion of processing is performed in general hardware under software control.

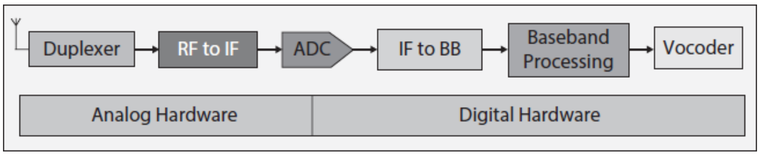
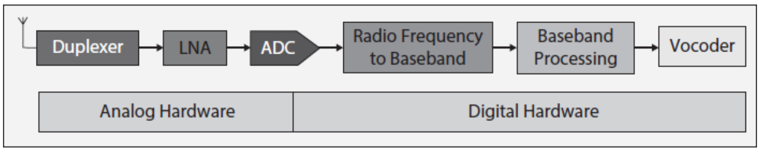


Figure 2.53 The pure software radio in which the majority of functions are performed by software.

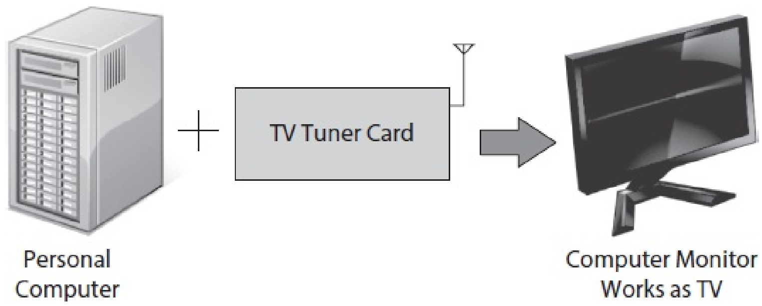


2.19. TV Tuner Card for PCs

2.19.1. What Is It?

A TV tuner card is a component that allows the personal computers to receive, capture, process, and record TV signals [51, 121, 131]. It is similar to the TV tuner of a digital TV. Most TV tuners also function as video capture cards, allowing them to record TV programs onto a hard disk. The schematic representation of a PC with TV tuner card is shown in Fig. 2.54. In essence, the monitor becomes a regular TV that displays a TV signal [18]. The advantage of using a TV tuner card to watch TV in a PC is the removal of the actual geographical hurdle that would generally obstruct a typical TV.

Figure 2.54 TV tuner card once installed in PC allows viewing TV in a monitor.



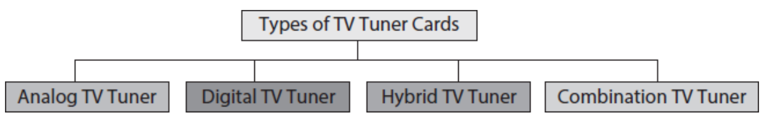
2.19.2. Background

In the early 1990s, the NEC laptop TV with a built-in television tuner and an antenna marked the beginning of watching TV signals in a digital computer [10]. The NEC laptop TV did not record and was only for watching TV. In 1992, the Mac TV was introduced primarily for watching TV and not for video recording. In 1992, the TV tuner card was introduced to watch TV signals in a PC by Animation Technologies Inc. [13]. In the same year, Hauppauge introduced the TV tuner cards for the PC [24]. In 1996, ATI Technologies Inc. introduced its TV tuner cards [14].

The existing varieties of TV tuner cards can be classified into the following types (seeFig. 2.55) [18]:

1. *Analog TV Tuner:* Analog TV tuners generate a raw video stream on receiving a signal from the antenna. They typically need a data integrated compression strategy for further recording.
2. *Digital TV Tuner:* Digital TV tuners generate compressed video (e.g. MPEG2) that displays high-quality videos and audio. These cards do not need additional encoding chips.
3. *Hybrid TV Tuner:* Hybrid TV tuners are the cards that can be reconfigured to operate as either an analog TV tuner or a digital TV tuner.
4. *Combination TV Tuner:* The combination TV tuner cards are the cards that simultaneously operate as an analog TV tuner and a digital TV tuner.

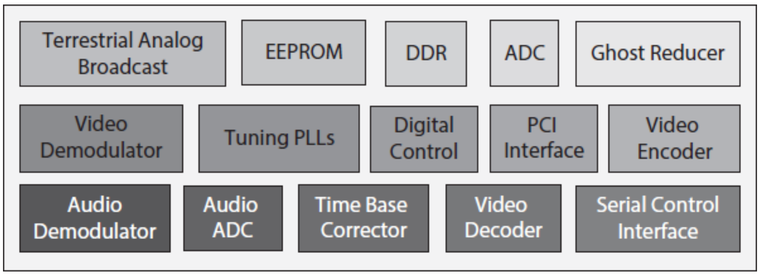
Figure 2.55 Different types of TV tuner cards.



2.19.3. What Is Inside?

The schematic representation of a typical TV tuner card is shown in Fig. 2.56. The antenna that is external to (not a part of) the TV tuner card receives terrestrial signals from the air. The signal may also come from a cable TV or other video-generating devices when the TV tuner is used for capturing and digitization purposes. The tuner is essentially PLLs. The RF signal is demodulated to an IF signal using the demodulators. The ADCs then convert the signals to digital forms for further processing using digital processors. The video is then processed and MPEG2 compressed video is sent to the PC through an interface. A ghost reducer is responsible for reducing ghost pictures. EEPROM nonvolatile memory is used to store data that must be saved when power is OFF. DDR volatile memory is used for intermediate storage.

***Figure 2.56** Different components of a TV tuner card.*



2.20. Universal Remote Control

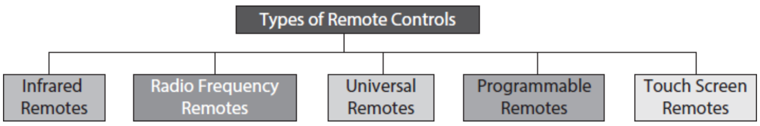
2.20.1. What Is It?

A universal remote control is a remote control that can be programmed to communicate with various brands of one consumer electronics device or various types of consumer electronics devices. The low-end universal remote controls can only communicate with a few consumer electronics devices. The high-end universal remote controls can communicate with large number of consumer electronics devices and can learn from new remote controls as they become available.

2.20.2. Background

In 1898, the earliest remote control was conceptualized by Nikola Tesla and described in his patent [145]. In 1939, the battery-operated LF radio transmitter called "Philco Mystery Control" became the first wireless remote control for a consumer electronics device [40]. In 1995, "Flashmatic" became the first wireless TV remote [23]. A large variety of remote controls have been designed since then. The different types of remote controls are presented in Fig. 2.57. In the early 1980s, the IR technology-based remote controls became popular. By the early 2000s, the proliferation of remote controls happened with an increasing number and variety of remote controls to communicate with the ever-increasing number of consumer electronics appliances. The RF remote controls provide longer and wider range as compared to the IR remote. The RF remote was first used in World War II. However, IR remote became a household name because of the cheaper price. The universal remote controls can communicate with various brands of one or more types of consumer electronic appliances. The programmable remote controls can be programmed to accommodate any system configuration to provide the control as if the systems are fully integrated. The universal and programmable remote controls are becoming immensely popular these days. The touchscreen remote controls have an LCD screen in which the buttons are actually images on the screen that send signals to the electronic appliance when touched.

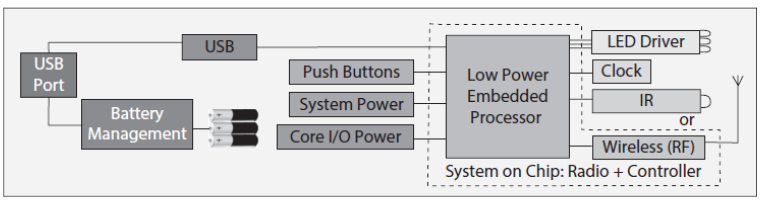
Figure 2.57 ***Different types of remote control.***



2.20.3. What Is Inside?

The different components of a universal programmable touchscreen remote control is shown inFig. 2.58 [32]. The main workhorse of the remote control is a low-power-embedded processor. This processor is designed using SoC technology. The processor is powered by a battery and battery management unit. Of note, the battery for this kind of remote is rechargeable. The signal communication component is RF or IR. The RF portions contain RF circuits and RF antenna. The signal from the IR is sent through the LED and its drivers. The remote control's display is an LCD touchscreen. The touchscreen has different control buttons as pictures. In addition, different physical keyboard buttons may be provided. The remote may contain a limited amount of permanent storage. The high-end versions of the remote may include a voice-control mechanism.

Figure 2.58 ***Different components of a universal programmable touchscreen remote control.***



2.21. Questions

2.1 Pick a consumer electronics media player system of your choice. Identify its hardware and software components. Briefly describe their functionalities.

2.2 Pick a consumer electronics system of your choice. Identify the different types of chips presented in the system and discuss their functionalities.

2.3 Pick a human health-monitoring system of your choice. Identify its hardware and software components. Briefly describe their functionalities.

2.4 Pick a security system of your choice. Identify its hardware and software components. Briefly describe their functionalities.

2.5 Describe the working principle of a touchscreen in an electronic system.

2.6 Identify different types of analog chips present in a smartphone.

2.7 Identify different types of digital chips present in a smartphone.

2.8 Briefly discuss different pixel sensors used in present-day cameras.

2.9 Identify a system that has multiple cores. Discuss what software and hardware components constitute such a multicore system.

2.10 Discuss the differences between a sensor and actuator. Give three examples of each.

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