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CECS 346 Embedded Systems I

Prof. Gevik Sardarbegians

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Lab 3 - SysTick Timer

In this lab we will be implementing a SysTick to our previous Lab #2, which will generate a more accurate timing of our embedded system. Our SysTick Timer will be replacing the original delay function that we created. We will also be introduced to a tool on Keil named "logic analyzer" which will allow us to view the bit state (0/1) of our ports.

Lab Photos

