Analysis of Various Approximate Multipliers

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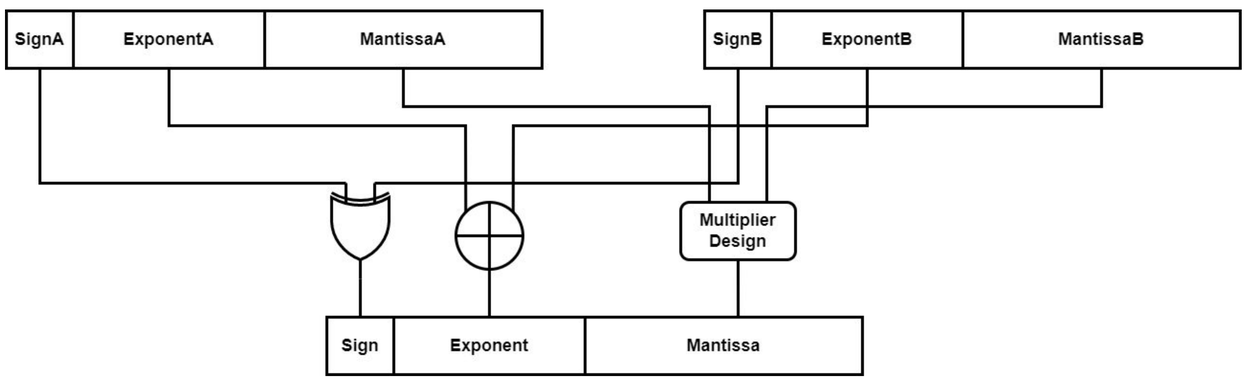
INTRODUCTION

The IEEE 754 standard has been used in various applications over the years. We used two techniques (the newly developed quantisation based on POSIT number system, and approximation) that could lead to a reduction in the hardware, power, and area requirements of the multiplier, while maintaining the accuracy for several Neural Networks, mainly focussing on LeNet5 and ResNet18. We have implemented various multipliers: Fixed-POSIT multiplier, approximate integer, approximate floating-point multipliers (Compressor-based, FPCAM, RMAC, CFPU), along with various approximate multipliers proposed over the years.

METHODOLOGY

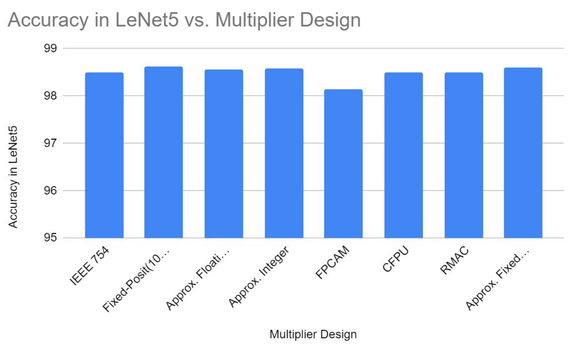
The general flow of the setup is as follows:

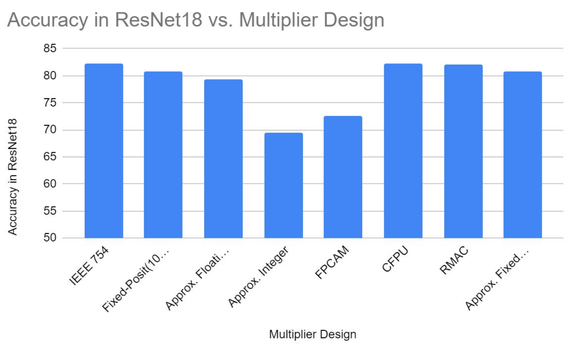


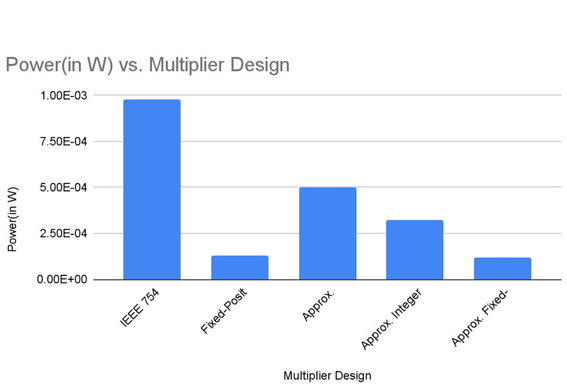
The multiplier design is replaced by one of the various multipliers we have tested.

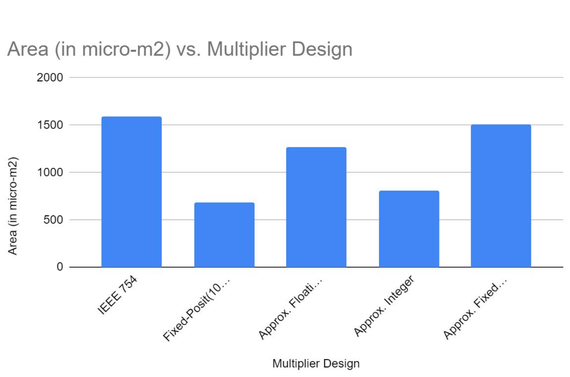
RESULTS

The following results for two Neural Networks have been obtained:









Note that:

1. For compressor-based approximate design, we have plotted the accuracy, power and area, when using the Yang2 [1] compressor.

2. For power and area comparison, the IEEE 754 standard, the approximate fixed-posit, and approximate floating-point multipliers use a total length of 16 bits.

CONCLUSIONS

- As could be observed from the plots in the Results section, it is evident that the approximate integer multiplier can be used only for smaller networks, but it accuracy drops as we go on to larger networks.

- Similarly, the compressor-based approximate floating-point multiplier works well for 32 bits, but as we decrease the number of bits of mantissa, accuracy would degrade.

- FPCAM (Floating Point Configurable Approximate Multiplier), as observed, consumes very less area and power, but we have to trade accuracy in larger networks.

- Similarly, CFPU (Configurable Floating-Point) and RMAC (Runtime Configurable) multiplier both have quite less drop in the accuracy as compared to the base accuracy.

- An another important observation is the difference in the accuracies on changing the operand sequence in the multiplier.
  That is, multiplying *a with b* and multiplying *b with a* would give us different accuracies in case of approximate multipliers.[6]

- For the compressor-based approximate multipliers (approximate integer, approximate floating-point, and approximate fixed-posit multipliers), it is observed that the power and area consumption is much less than the standard IEEE 754 multiplier.

  Amongst the compressor designs [1], Yang2 is observed to be the most accurate design (although consuming more area and power as compared to other compressor designs). Similarly, the Sabetz multiplier is observed to have the least accuracy, but is quite efficient in terms of area and power. Note that for the results, best case accuracy is reported (accuracy of Yang2).

- A final observation that was made is that when the number of mantissa bits are eight or more, we could use the compressor-based approximation technique for hardware reduction. Else, we could use the techniques used in other approximate multipliers, such as FPCAM, RMAC, or CFPU.

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