ATF-54143

High Intercept Low Noise Amplifier for the 1850–1910 MHz PCS Band using the Enhancement Mode PHEMT

Application Note 1222

Introduction

Avago Technologies' ATF-54143 is a low noise enhancement mode PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. Avago Technologies' new enhancement mode technology provides superior performance while allowing a DC grounded source amplifier with a single polarity power supply to be easily designed and built. Unlike a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. Instead of a 0.7 V base to emitter voltage, the enhancement mode PHEMT requires about a 0.6 V potential between the gate and source for nominal drain current.

The ATF-54143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The 800 micron gate width of the ATF-54143 makes it ideal for applications in the VHF and lower GHz frequency range by providing low noise figure coincident with high intercept point. The wide gate width also provides low impedances that are easy to match.

This application note describes the use of the ATF-54143 in a low noise amplifier optimized for the 1850 to 1910 MHz band for PCS base station applications. The amplifier design combines low noise figure and good third order intercept point (IP3), while maintaining moderate input and output return loss. The amplifier makes use of surface mount miniature multi-layer chip inductors for a compact layout.

When biased at a bias point of $V_{ds} = 3$ V and I_d of 60 mA, the ATF-54143 is specified as having a nominal noise figure of 0.5 dB with a typical gain of 16.5 dB. The output intercept point (OIP3) is specified at +36 dBm, making the device capable of an input intercept point (IIP3) of nearly +20 dBm.

LNA Demo Board

For applications in the VHF through 2.4 GHz frequency range, a generic demonstration board was developed. The board, as shown in Figure 1, is etched on 0.031" FR-4 for low cost. The board utilizes small surface mount components. Input and output are via E.F. Johnson SMA connectors, part number 142-0701-881.

PCS Amplifier Design

The schematic diagram describing the PCS low noise amplifier is shown in Figure 2. Circuit topology is very similar to the typical depletion mode circuit except for the method of biasing the device. A parts placement drawing is shown in Figure 3. The parts list for the amplifier is shown in Table 1. A photograph of a completed demonstration board is shown in Figure 4.

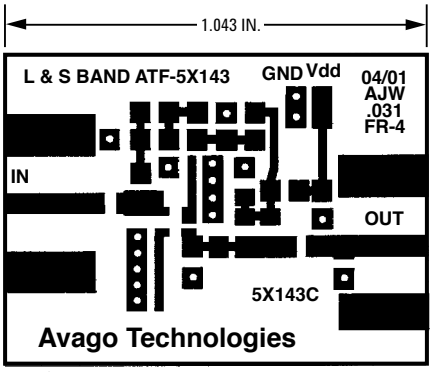

Figure 1. 1X Artwork for the Avago Technologies' ATF-54143 Low Noise Amplifier Demonstration Board. Actual dimensions: 1.043 inch by 0.755 inch.

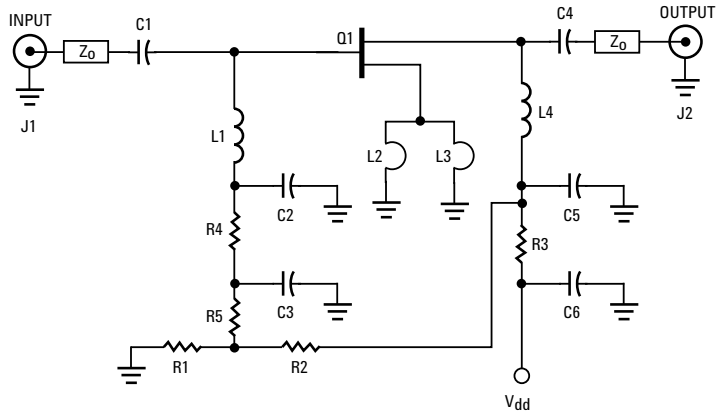

Figure 2. Avago Technologies' ATF-54143 low noise PCS amplifier using passive biasing.

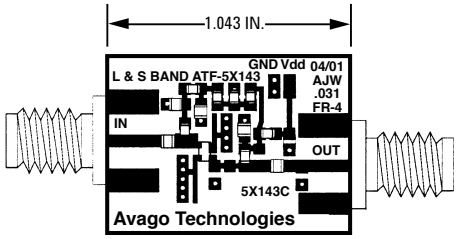

Figure 3. Component Placement Drawing for the Avago Technologies' ATF-54143 Low Noise Amplifier.

Table 1. Component Parts List for the ATF-54143 Amplifier.

C1, C2, C4, C5	8.2 pF chip capacitor Rohm MCH185A8R2DK
C3, C6	10,000 pF chip capacitor Murata GRM188R71H103KA01D
J1, J2	SMA Connector, EF Johnson p.n. 142-0701-881
L1	2.7 nH inductor (Toko LL1608-FH2N7S)
L2, L3	Strap each source pad to the ground pad with 0.040" wide etch. The jumpered etch is placed a distance of 0.025" away from the point where each source lead contacts the source pad. Cut off unused source pad. See text.
L4	5.6 nH inductor (Toko LL1608-FH5N6K)
Q1	Avago Technologies' ATF-54143 PHEMT
R1	300 Ω chip resistor
R2	1200 Ω chip resistor
R3	10 Ω chip resistor
R4	50 Ω chip resistor
R5	10K Ω chip resistor (see text)
Zo	50 Ω Microstripline

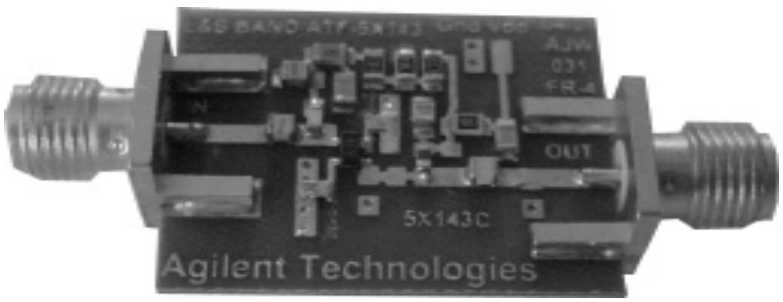

Figure 4. Photograph of completed Avago Technologies' ATF-54143 Demonstration Amplifier.

One of the advantages of the enhancement mode PHEMT is the ability to DC ground the source leads and still require only a single positive polarity power supply. Whereas a depletion mode PHEMT pulls maximum drain current when $V_{gs} = 0$ V, an enhancement mode PHEMT pulls nearly zero drain current when $V_{gs} = 0$ V. The gate must be made positive with respect to the source for the enhancement mode PHEMT to begin pulling drain current. It is also important to note that if the gate terminal is left open-circuited, the device will pull some amount of drain current due to leakage current, creating a voltage differential between the gate and source terminals.

Biasing the ATF-54143 is accomplished by the use of a voltage divider consisting of R1 and R2. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback to help keep drain current constant. The purpose of R4 is to enhance the low frequency stability of the device by providing a resistive termination at low frequencies. Capacitor C3 provides a low frequency bypass for R4. Additional resistance in the form of R5 (approximately 10KΩ) is added to provide current limiting for the gate of enhancement mode devices such as the ATF-54143. This is especially important when the device is driven to P1dB or Psat. The effect of R5 will be discussed in the results section of this application note. R5 can be eliminated if the values of resistors R1 and R2 are appropriately chosen. There is more information regarding this subject in a later section.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor (C1) and a shunt inductor (L1). The high-pass topology is especially well-suited for PCS and WLAN applications as it offers good low frequency gain reduction which can minimize the amplifier's susceptibility to cellular and pager transmitter overload. L1 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. C1 also doubles as a DC block. The Q of L1 is extremely important from the standpoint of circuit loss which directly relates to noise figure. The Toko LL1608-F2N7S is a small multilayer chip inductor with a rated Q of 32 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. This network has been optimized primarily for noise figure with secondary emphasis on input return loss. A modest amount of source inductance in the form of L2 and L3 is used to improve input return loss with minimal effect on noise figure.

The amplifier uses a similar high-pass structure for the output impedance matching network. L4 and C4 provide the proper match for best output return loss and maximum gain. L4 also doubles as a means of inserting voltage to the drain. Resistor R3 and capacitor C6 provide a low frequency resistive termination for the device which helps stability. C6 was chosen to be 10000 pF or 0.01 μF over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the low frequency (F2-F1) difference component of the two test signals used to measure IP3. This can be especially important for the typical 1.25 MHz spacing used in CDMA IP3 evaluation.

The demonstration board is designed for use with any of the SOT-343 packaged family of Avago Technologies' enhancement mode PHEMT devices. The demonstration board was also designed so that the designer has several circuit options with which to optimize performance for a particular application. Component mounting pads are provided near L4 to allow a resistor to be paralleled with L4 to lower gain and increase stability. A space is also provided for a resistor in series with the device drain lead. The space has already been jumpered on the demo board and can be easily removed with a sharp knife if a series resistance is desired. Neither of these resistors is required for this LNA design. It is important to remember that any amount of resistive loading in the drain circuit will effect gain and, more importantly, P1dB and OIP3.

Inductors L2 and L3 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback to the device. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability, and input and output return loss. The amplifier demonstration board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstripline which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad would be connected to the ground pad with a very short piece of etch at the point closest to the device source lead.

A moderate amount of source inductance is used in the amplifier described in this application note. The optimum length for each source lead is 0.025". The 0.025" is measured from the edge of the source lead to the closest edge of the ground strap. See Figure 5. The ground straps are made from copper strap approximately 0.020" in width.

The straps are used to bridge the 0.020" gap from the source lead etch to the ground pad. In the actual conversion of the design to a board layout, each source lead can be made approximately .045" in length from the edge of the device source lead to the ground pad. The ground pad should have at least two plated-through holes connecting the ground pad to the bottom ground plane.

Performance of the Avago Technologies' ATF-54143 Amplifier

The amplifier is tested at a bias point of $V_{ds} = 3\,V$ @ $I_d = 65$ mA. The measured noise figure and gain of the completed amplifier are shown in Figures 6 and 7. Noise figure is under 0.8 dB from 1800 to 2000 MHz. Gain is a nominal 16 dB at 1900 MHz. Matching circuit losses have been measured on similar printed circuit boards using similar discrete matching components and have been found to exhibit several tenths of a dB of loss. Subtracting this loss from the measured noise figure of the complete amplifier results in a nominal 0.5 dB noise figure for the device by itself.

Measured input and output return loss is shown in Figure 8. The input return loss measures a nominal -6.4 dB at 1900 MHz, while the output return loss measures -12.5 dB.

Most PCS base station low noise amplifiers are used in a balanced configuration. The usual balanced configuration consists of the antenna feeding the input port of a 90 degree hybrid coupler which feeds two similar ATF-54143 amplifiers with an equal amplitude power division with a 90 degree phase offset between the two amplifiers. An additional 90 degree hybrid coupler combines the outputs from the ATF-54143 amplifiers into a single output. The primary advantage of the balanced configuration is up to a 3 dB improvement in P1dB and OIP3 with only a slight degradation in gain and noise figure due to coupler losses. Another important advantage of the balanced configuration is very good input return loss. As long as the amplitude and phase of the reflected signal from each ATF-54143 amplifier are reasonably matched, the resultant reflection from the input 90 degree hybrid will be very low, resulting in very good input return loss. Any reflected power is dissipated in the isolated port load resistor on the fourth port of the input 90 degree hybrid coupler.

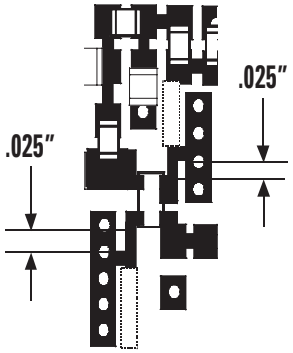

Figure 5. Source Grounding for the ATF-54143.

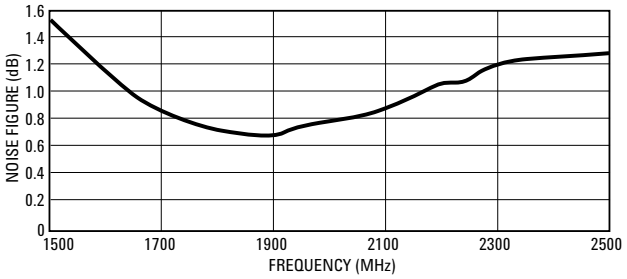

Figure 6. Avago Technologies' ATF-54143 Amplifier Noise Figure vs. Frequency.

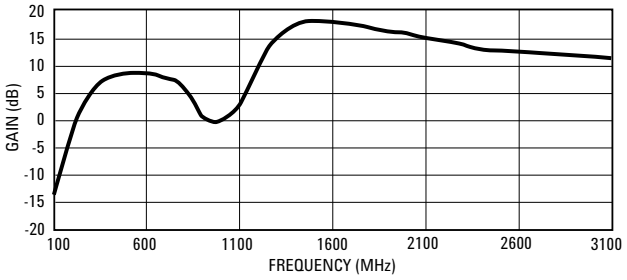

Figure 7. Avago Technologies' ATF-54143 Amplifier Gain vs. Frequency.

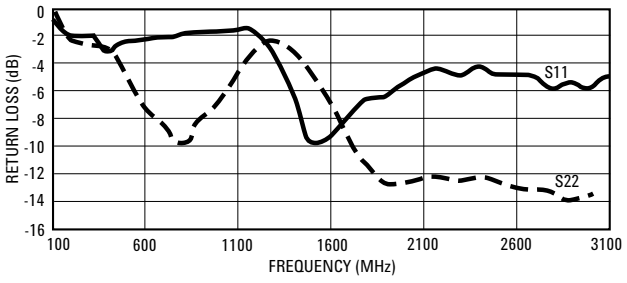

Figure 8. Avago Technologies' ATF-54143 Amplifier Input and Output Return Loss vs. Frequency.

Further improvement in LNA S11 is possible by lengthening L2 and L3. Lengthening L2 and L3 also reduces in-band gain and improves in-band stability. The limit on how much source inductance can be tolerated by the device is based on out-of-band gain peaking and resultant instabilities. Consult Appendix 1 for additional information regarding source inductance and its resultant effect on amplifier performance.

The output third order output intercept point (OIP3) was measured to be +36.5 dBm at 1.9 GHz. This calculates out to be an input intercept point (IIP3) of +20 dBm.

Passive Biasing versus Active Biasing and its effect on P1dB and Gate Current

The P1dB of the low noise amplifier is dependent on the type of bias supply used as well as the DC impedance presented to the gate terminal. The output P1dB of the amplifier as biased in Figure 2 measured +19.6 dBm. As the amplifier is driven to P1dB and beyond, the device is being driven out of Class A and into Class AB. As a result of driving the amplifier into Class AB, the drain current can either increase or decrease in value. This is very much frequency and load impedance dependent. An added effect is that gate current will increase with increased RF drive.

Both depletion mode and enhancement mode PHEMTs manufactured by Avago Technologies use Schottky-barrier metal for the source and drain contacts. A simplified schematic diagram showing these contacts as two Schottky diodes connected back-to-back is shown in Figure 9.

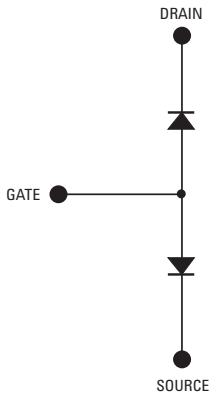

Figure 9. DC representation of PHEMT showing back-to-back Schottky barrier contacts.

In the case of a depletion mode PHEMT, the normal negative gate-to-source voltage will reverse bias the gate-to-source Schottky diode junction resulting in very low gate current. In the case of an enhancement mode PHEMT such as the ATF-54143, the positive gate-to-source voltage will forward bias the gate-to-source Schottky diode junction. At low values of forward conduction, the resultant I_{gs} will be very low (in the μA region), increasing to 100s of μA as V_{gs} approaches approximately 0.7 V. Normal gate current under standard bias conditions and operation in the linear region will be very low. However, as the RF input is increased to the level approaching P1dB, the average rectified gate current increases. The degree of increase in gate current under high RF drive is bias circuit dependent. Several different bias schemes were evaluated and the results are presented in this section. The amplifier is tested with both passive and active bias and with various amounts of gate current limiting.

The configuration for passive biasing is shown previously in Figure 2. Resistor R5 in Figure 2 provides gate current limiting by presenting a high impedance to the device. The circuit is analyzed with resistor R5 equal to 10K Ω and R5 equal to 0 Ω.

The amplifier circuit was also analyzed with active biasing as shown in Figure 10. The active biasing scheme uses the typical textbook bias circuit using a PNP transistor and several resistors connected as a regulator. Resistors R1 and R2 provide a constant voltage at the base of Q2. The voltage is increased by the 0.7 volt V_{BE} drop of Q2 and presented to the drain circuit. Resistor R3 sets the drain current based on a constant supply voltage V_{dd} and a constant voltage at the emitter of Q2. Capacitor C7 provides an AC bypass at the collector of Q2. This capacitor helps suppress any noise and/or oscillations that may be caused by Q2. Resistor R6 provides similar gate current limiting as did R5 in the passive bias circuit. The active biasing circuit is tested with resistor R6 set at 0 Ω, 1K Ω, and 10K Ω.

The parts list for the components used in the active biasing circuit is shown in Table 2. The RF circuitry uses the same components as shown in Figure 2 and Table 1.

Table 2. Component values used in the Active Biasing Circuit

C3,C6,C7	0.01 μF
Q2	2N2907 PNP BJT or equivalent
R1	1450 Ω
R2	1050 Ω
R3	23 Ω
R4	10 Ω
R5	50 Ω
R6	10K Ω
R7	1K Ω

In order to evaluate the performance of each of the various passive and active biasing circuits, RF input power was swept from -14 dBm up to +8 dBm at 1880 MHz. The graph in Figure 11 shows RF power output versus RF power input for the various passive and active biasing configurations. The graph in Figure 12 relates RF power input to average rectified gate current for the various bias configurations.

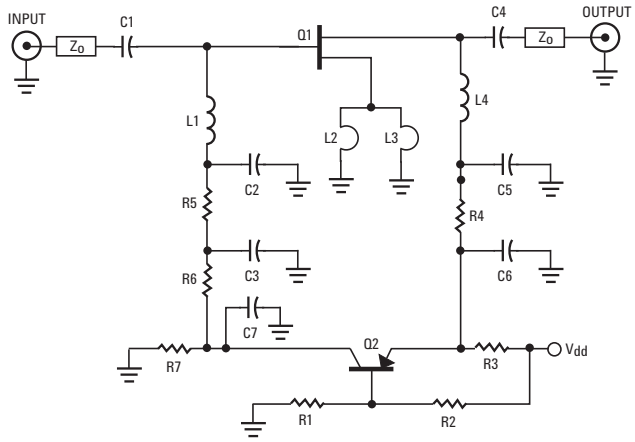

Figure 10. Avago Technologies' ATF-54143 LNA with Active Biasing.

Analysis of the Passive Biasing Network

As shown in Figure 11, the passive biasing supply with R5 = 10KΩ provides a slightly higher P1dB, but then quickly compresses. The high impedance gate supply with R5 = 10KΩ actually allows the amplifier to have gain expansion just prior to P1dB. With R5 = 0Ω, the amplifier has higher saturated output power due to the stiffer bias supply. The equivalent impedance of the gate supply is 300Ω in parallel with 1250Ω or approximately 242Ω, which is then in series with R4 (50Ω) = 292Ω. The stiffer gate supply actually allows greater gate current to flow under hard drive conditions.

The graph in Figure 12 shows that the average rectified gate current at P1dB is less than 50 μA for R6 = 10KΩ and 0Ω. However, at P3dB, the rectified gate current for R6 = 0Ω, is 850 μA which corresponds to an input power level of +6 dBm. Increasing the input power level to +8 dBm causes the gate current to approach 2.3 mA. Increasing R5 to 10,000Ω limits the gate current to 100 μA even at an input power level of +8 dBm.

Analysis of the Active Biasing Circuits

In general, active biasing does not offer any advantage over passive biasing with regards to improving P1dB. However, saturated power output is best with R6 = 10KΩ. As noted with the passive biasing circuits, increasing the value of R6 does limit gate current under hard drive conditions and is highly recommended. As shown in Figure 12, even 1000Ω for R6 is not high enough to minimize the draw of gate current under hard drive conditions. Using 10KΩ for R6 limits the gate current to 500 μA, even with an input power of +8 dBm.

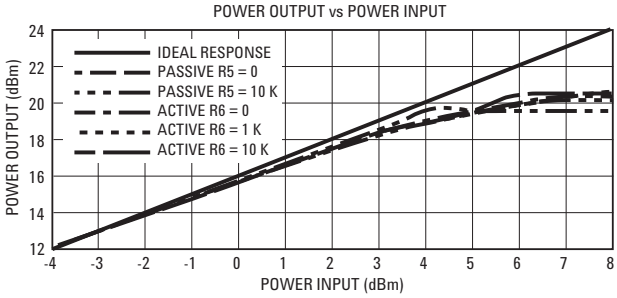

Figure 11. Power Output vs. Power Input for Passive and Active Biasing.

Maximum Suggested Gate Current

The maximum suggested gate current for the ATF-54143 is 2 mA. Incorporating resistor R5 in the passive bias network, or resistor R6 in the active bias network, safely limits gate current to 500 μA at P1dB drive levels. In order to minimize component count in the passive biased amplifier circuit, the 3 resistor bias circuit consisting of R1, R2, and R5 can be simplified, if desired. R5 can be removed if R1 is replaced with a 4.7KΩ resistor and if R2 is replaced with a 27KΩ resistor. This combination should limit gate current to a safe level.

P1dB and Drain Efficiency

The data in Table 3 compares the P1dB and relative drain efficiency of each bias circuit. The passive bias circuit with R5 equal to 10 KΩ provides superior P1dB and superior drain efficiency. The higher impedance passive circuit allows the drain current to decrease at P1dB with the side effect of improved drain efficiency.

Conclusion

The Avago Technologies' ATF-54143 low noise PHEMT has been designed into a low noise amplifier application for the 1850 to 1910 MHz PCS market. The amplifier provides low noise figure (0.75 dB) and very good IIP3 (+20 dBm) coincident with moderate input return loss, good output return loss, and moderate gain at a bias point of V_{ds} = 3 V and I_d = 60 – 65 mA. The enhancement mode technology also eliminates the need for a negative power supply, making biasing significantly easier as compared to biasing depletion mode devices.

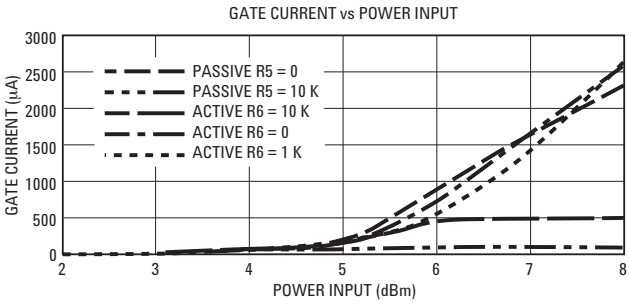

Figure 12. Gate Current vs. Power Input for Passive and Active Biasing.

Table 3. P1dB and Drain Efficiency for Various Bias Networks.

Circuit	Vd (V)	Idq (mA)	Id @ P1dB (mA)	DC input (mW)	P1dB (dBm)	Eff. (%)
Passive R5 = 0	3	60	61.0	183	+18.3	36.90
Passive R5 = 10K	3	60	43.0	129	+19.6	70.70
Active R6 = 0	3	60	57.7	173	+18.8	43.80
Active R6 = 1K	3	60	58.7	176	+18.6	41.10
Active R6 = 10K	3	60	58.9	177	+18.7	41.90

Appendix 1.
Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential downside is reduced low frequency gain. However, decreased gain also correlates to higher input intercept point. The question then becomes one of how much source inductance can be added before going too far.

For an amplifier operating in the 2 GHz frequency range, excessive source inductance usually manifests itself in the form of a gain peak above 6 GHz, and even sometimes above 12 GHz. Normally the high frequency amplifier gain roll-off is gradual and smooth. Adding source inductance begins to add bumps or gain peaks to the once smooth gain roll-off. The source inductance, while having a degenerative effect at low frequencies, has a regenerative effect at higher frequencies. This shows up as a very high frequency gain peak (S21) and input return loss (S11) becoming more positive. Some shift in upper frequency performance is acceptable as long as the amount of source inductance is fixed and has some margin in the design to account for S21 variations in the device.

A wide-band gain plot of S21 for an amplifier using the 400 micron gate width ATF-55143 device is shown in Figure 13. The plot shown in Figure 13 represents an amplifier that uses minimal source inductance and has a relatively flat gain response at the higher frequencies. The amplifier has relatively high gain at 2 GHz, but less than 0 dB gain above 6 GHz.

The wide-band gain plot shown in Figure 14 is for the same amplifier that uses additional source inductance. Increased source inductance improves low frequency stability by lowering gain at 2 GHz by 1 to 2 dB. Input return loss will also be improved while noise figure will stay relatively constant. The effect of adding additional source inductance can be seen as some gain peaking above 6 GHz. This level of gain peaking shown in Figure 14 is not considered a problem because of its relatively low level compared to the in-band gain.

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak in the 12 to 13 GHz frequency range which could approach several dB. Its effect can be seen in Figure 15. The end result is poor amplifier stability, especially when the amplifier is placed in a housing with walls and a cover.

Larger gate width devices such as the 800 micron ATF-54143 will be less sensitive to source inductance than the smaller gate width devices and can therefore tolerate more source inductance before instabilities occur. The only drawback of the wider gate width ATF-54143 is slightly reduced gain. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance on overall amplifier performance.

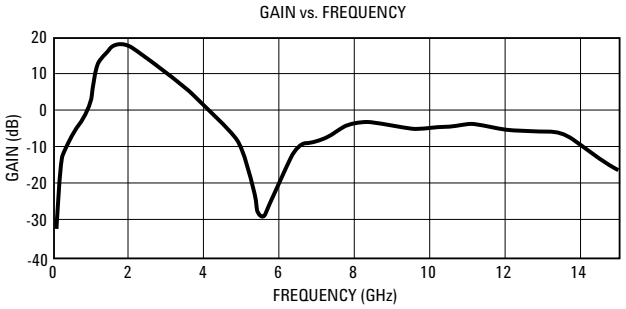

Figure 13. Wide-band gain plot of 2 GHz ATF-55143 amplifier using minimal source inductance.

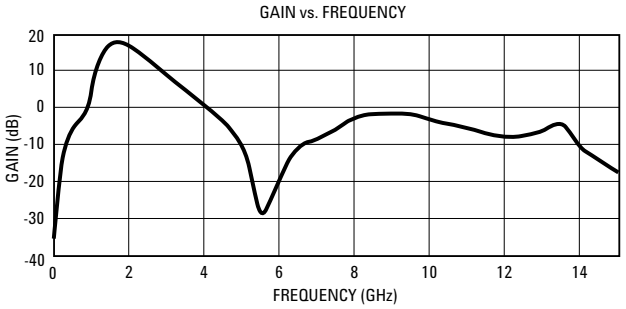

Figure 14. Wide-band gain plot of 2 GHz ATF-55143 amplifier with an acceptable amount of source inductance.

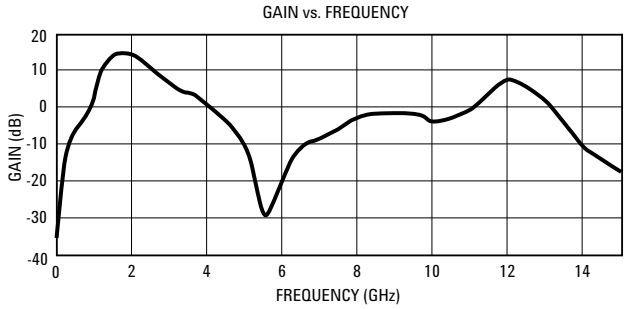

Figure 15. Wide-band gain plot of 2 GHz ATF-55143 amplifier with an unacceptable amount of source inductance producing undesirable gain peaking in the 12 to 13 GHz frequency range.

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

Obsoletes 5988-4290EN
5989-2273EN May 13, 2010