AMD

Chapter 17

# DDR Memory Controller

## Introduction

Figure 17-1 shows the AMD Zynq™ UltraScale+™ MPSoC DDR subsystem placement. It connects to rest of the MPSoC through six AXI data interfaces and one AXI control interface. One of the data paths is connected to the real-time processing unit (RPU) and two to the cache coherent interconnect (CCI-400). Others are multiplexed across the DisplayPort controller, FPD DMA, and the programming logic (PL). Of the six interfaces, five are 128-bits wide and the sixth interface (tied to the RPU) is 64-bits wide.

The DDR subsystem supports DDR3, DDR3L, LPDDR3, DDR4, and LPDDR4. It can accept read and write requests from six application host ports that are connected to the controller using AXI bus interfaces. These requests are queued internally and scheduled for access to DRAM devices. The memory controller issues commands on the DDR PHY interface (DFI) interface to the PHY module that reads and writes data from DRAM.

### System Memories

The processor-addressable memories are shown in Figure 17-1 and include the following:

- External DDR DRAM memory.
- Internal OCM memory (LPD), see Chapter 18, On-chip Memory.
- RPU tightly-coupled memory (TCM), see Chapter 4, Real-time Processing Unit.
- PL block UltraRAM memories, see *UltraScale Architecture Memory Resources User Guide* (UG573) [Ref 10].

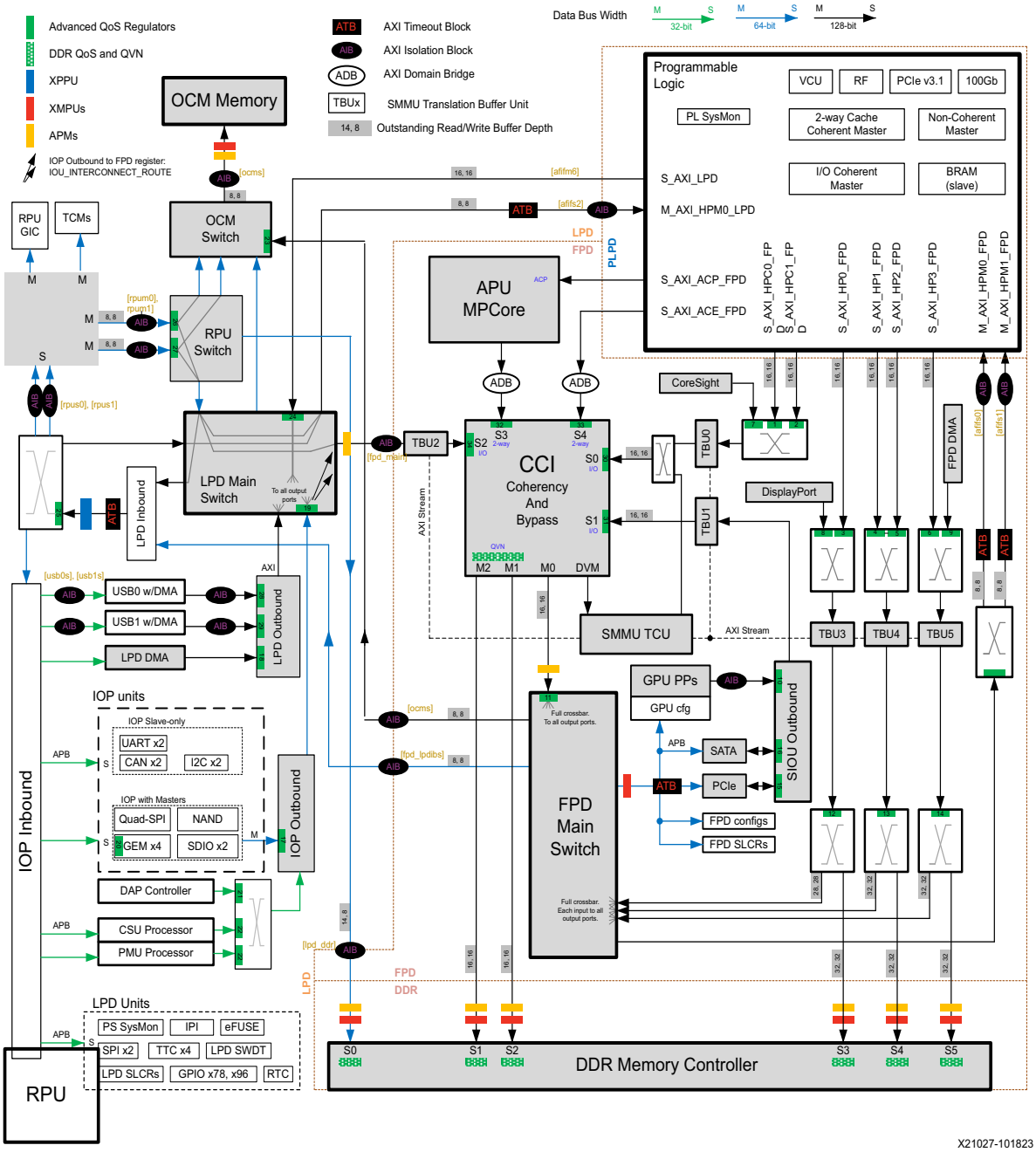


*Figure 17-1:* **System Memories**

## Features

- DDR3, DDR3L, LPDDR3, DDR4, and LPDDR4.
- Support Dynamic DDR configuration of key timings parameter values by reading the SPD on SODIMM/UDIMM/RDIMM parts.
- Dual-rank configurations.
- Dynamic scheduling to optimize bandwidth and latency.
- 64 read and 64 write buffers in fully associative content addressable memories (CAMs).
- Error correction code (ECC) support in 32-bit and 64-bit mode, 2-bit error detection and 1-bit error correction. No ECC support for LPDDR3.
- Programmable quality of service (QoS):
  - Video, isochronous: reads and writes.
  - Low latency: reads.
  - Best effort: reads and writes.
- Delayed writes for optimum performance on SDRAM data bus.
- Out-of-order execution of commands for enhanced SDRAM efficiency.
- Automatic DRAM low-power modes:
  - Entry and exit events based on memory traffic.
  - Power-down, clock-stop, and self-refresh.
  - Clock-stop not supported with RDIMMs.
  - No automatic low-power support for LPDDR3 and LPDDR4.
- Explicit SDRAM mode register updates under software control.
- Highly efficient read-modify-write transactions when byte enables are used with ECC enabled.
- Automatic logging of both correctable and uncorrectable errors.
- Ability to poison the write data by adding uncorrectable errors, for use in testing ECC error handling (ECC poison).
- Responsive to XMPU poisoned AXI transaction.
- Enable 2tCK command timing (2T timing) on the DDR3/DDR4 command/address/control bus signals. This feature can be used as a workaround to address signal quality problems on the CAC bus caused by sub-optimal board layout or power quality issues.

## DDR PHY Features

- Complete PHY initialization, training, and control.
- Automatic differential data strobe (DQS) gate training.
- Delay line calibration and voltage threshold (VT) compensation.
- Automatic write leveling.
- Automatic read and write data bit deskew and eye centering.
- Automatic address/command bit deskew and eye centering for LPDDR3.
- Automatic bit deskew and eye centering for LPDDR4.
- Enhanced power saving support.
- PHY control and configuration registers.
- Compatible with the DFI 4.0 PHY interface standard.

## DDR Memory Types, Densities, and Data Widths

The DDR memory controller is able to connect to devices under the conditions listed in Table 17-1.

*Table 17-1:* **DDR Memory Controller Conditions**

| Parameter | Value | Notes |
|---|---|---|
| Maximum total memory density (GB) | 34 | This is the maximum supported density. |
| Total data width (bits) | 16, 32, 64 | 16 and 64-bit LPDDR4 are not supported. 16-bit is supported for DDR4 only. |
| Component memory density (Gb per die) | 0.5, 1, 2, 4, 6, 8, 12, 16 | 3, 6, 12 and 16Gb single-channel LPDDR4 are not supported.<br>6, 12, 24 and 32Gb dual-channel LPDDR4 are not supported. |
| Component data width (bits) | 8, 16, 32 | 4-bit devices not supported. Byte-mode LPDDR4 devices not supported. |
| Number of ranks | 2 | |
| Number of row address bits | 17(2) | Limited by the memory controller. |
| Number of bank address bits | 3 | |
| Bank group | 2 | |
| MEMC_FREQ_RATIO | 2 | DDR PHY to controller clock ratio (2:1). |

**Notes:**
1. 3DS DDR4 is not supported in PS.
2. LPDD4 support is limited to 16 row bits. DDR4 support is limited to 17 row bits. DDR3, DDR3L, and LPDDR3 are limited by their DRAM specifications.

Table 17-2 lists some memory configuration examples. The memory configuration speeds are listed in the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) [Ref 2].

*Table 17-2:* **Example Memory Configurations**

| Technology | Configuration | Number of Components | Total Width | Component Density | Capacity | Rank |
|---|---|---|---|---|---|---|
| DDR3 (with ECC) | x8 | 9 | 72 | 4 Gb/8 Gb | 4 GB/8 GB | 1 and 2 |
| DDR3 (with ECC) | x16 | 5 | 72 | 2 Gb | | 1 |
| DDR3L (with ECC) | x8 | 9 | 72 | 4 Gb/8 Gb | 4 GB/8 GB | 1 and 2 |
| DDR3L (with ECC) | x16 | 5 | 72 | 2 Gb | | 1 |
| LPDDR3 | x32 | 2 | 64 | 4Gb | | 1 |
| DDR4 | x8 | 8 | 64 | 8 Gb/16 Gb | 8 GB/16 GB | 1 and 2 |
| DDR4 (with ECC) | x16 | 5 | 72 | 8 Gb | | 1 |
| LPDDR4 | x32 | 1 | 32 | 8 Gb | | 1 |
| LPDDR4 | x32 with DDP | 1 | 32 | 16 Gb | | 2 |
| LPDDR4 (with ECC) | x32 | 2 | 40 | 8 Gb | | 1 |

***Note:*** Table 17-2 lists just some of the possible memory configurations. Other configurations are possible.

## DDR DRAM Pins

The DDR I/O pins are located on bank 504 and can have a 16-bit, 32-bit or 64-bit data path to the DRAMs depending on the device type. Bytes 0 to 1 correspond to 16-bit data, bytes 0 to 3 correspond to 32-bit data, and bytes 0 to 7 correspond to 64-bit data. Byte 8 refers to the ECC bits. The pins are summarized in Table 17-3. See *Zynq UltraScale+ MPSoC Packaging and Pinout User Guide (*UG1075) [Ref 7] for pin assignments. The pin swap guidelines are described in Answer Record 67330. See *UltraScale Architecture PCB Design User Guide* (UG583)[Ref 15] for clamshell functionality.

*Table 17-3:* **DDR Pins**

| Pin Name | Direction | Description |
|---|---|---|
| PS_DDR_DQ | Input/Output | DRAM data. |
| PS_DDR_DQS_P | Input/Output | DRAM differential data strobe positive. |
| PS_DDR_DQS_N | Input/Output | DRAM differential data strobe negative. |
| PS_DDR_ALERT_N | Input | DRAM alert signal. |
| PS_DDR_ACT_N | Output | DRAM activation command. |
| PS_DDR_A | Output | DRAM row and column address. |
| PS_DDR_BA | Output | DRAM bank address. |
| PS_DDR_BG | Output | DRAM bank group. |

*Table 17-3:* **DDR Pins *(Cont'd)***

| Pin Name | Direction | Description |
|---|---|---|
| PS_DDR_CK_N | Output | DRAM differential clock negative. |
| PS_DDR_CK | Output | DRAM differential clock positive. |
| PS_DDR_CKE | Output | DRAM clock enable. |
| PS_DDR_CS | Output | DRAM chip select. |
| PS_DDR_DM | Output | DRAM data mask. |
| PS_DDR_ODT | Output | DRAM termination control. |
| PS_DDR_PARITY | Output | DRAM parity signal. |
| PS_DDR_RAM_RST_N | Output | DRAM reset signal, active Low. |
| PS_DDR_ZQ | Input/Output | ZQ calibration signal. |

### Power and Reset

The DDR memory controller is powered by the VCC_PSINTFP_DDR pins. These pins must be connected to the VCC_PSINTFP power pins and the FPD power supply. The DDR memory controller can only be reset along with the FPD using the PMU_GLOBAL.GLOBAL_RESET [FPD_RST] reset bit.

***Note:*** Once the initial calibration sequence in psu_init.c is completed AMD does not recommend using RST_DDR_SS to reset the DDR subsystem.

## System Block Diagram

The DDR subsystem (Figure 17-2) consists of six instances of the AMD memory protection unit (DDR_XMPU), AXI to APB bridge, AXI performance monitor, DDR controller and DDR PHY.

The XMPU protection unit prevents unauthorized access to restricted areas of the DDR. Both read and write accesses are restricted. The AXI performance monitor provides AXI throughput and latency for all six input ports of the DDR controller. The AXI performance monitor can be accessed by software.

After the request goes through the performance monitors and protection units, the DDR controller establishes a priority for each read, write, and high priority read request based on many factors. The requests are arbitrated and presented to the DDR PHY, and several stages of buffering occurs.

The PHY processes read/write requests from the controller and translates them into specific signals within the timing constraints of the target DDR memory. Signals from the controller are used by the PHY to produce internal signals that connect to the pins through the digital

PHYs. The DDR pins connect directly to the DDR device or devices through the PCB signal traces.

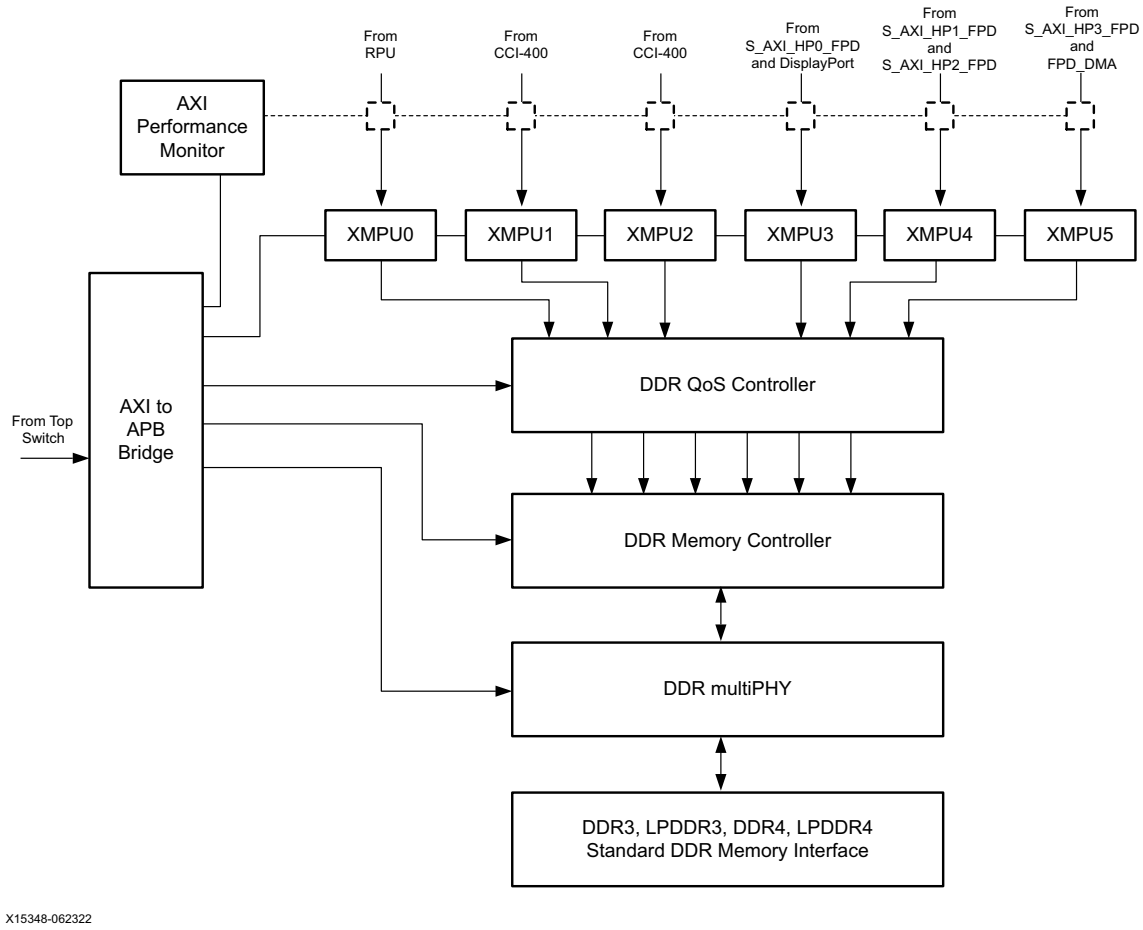


*Figure 17-2:* **DDR Subsystem Block Diagram**

## AMD Memory Protection Unit

The XMPU is a region-based memory protection unit. In this chapter, an AXI port interface is referred to as an AXI port. An incoming read or write request on an AXI port in one of the XMPUs is checked against each XMPU region. Any read or write transactions to the DDR regions undergo predefined checks and only when they pass these checks are the transactions allowed. Read and write permissions are independently checked. If the check fails, then the transaction is handled as described in the *XMPU Error Handling* section in the System Protection Units in Chapter 16.

The addresses and master IDs are used for checks. If the address and ID range checks are true, and if the memory region is configured as secure, then only a secure request can access this region. If the transaction is non-secure and the region is configured as secure,