Zynq UltraScale + Device

Technical Reference Manual

UG1085 (v2.4) December 21, 2023

AMD Adaptive Computing is creating an environment where employees, customers, and partners feel welcome and included. To that end, we're removing non-inclusive language from our products and related collateral. We've launched an internal initiative to remove language that could exclude people or reinforce historical biases, including terms embedded in our software and IPs. You may still find examples of non-inclusive language in our older products as we work to make these changes and align with evolving industry standards. Follow this link for more information.



AMDA

Table of Contents

Chapter 1: Introduction Functional Units and Peripherals 20 **Chapter 2: Signals, Interfaces, and Pins Chapter 3: Application Processing Unit** System Registers 62

System Memory Virtualization Using SMMU Address Translation	63
Chapter 4: Real-time Processing Unit	
Introduction	68
Cortex-R5F Processor Functional Description	
Error Correction and Detection	
Level2 AXI Interfaces	74
Memory Protection Unit	74
Events and Performance Monitor	75
Power Management	75
Exception Vector Pointers	75
System Register Overview	76
Tightly Coupled Memory	77
Chapter 5: Graphics Processing Unit	
Introduction	84
Graphics Processing Unit Functional Description	
Graphics Processing Unit Level 2 Cache Controller	94
Graphics Processing Unit Memory Management Unit	95
Graphics Processing Unit Programming Model	98
Graphics Processing Unit Register Overview	.00
Chapter 6: Platform Management Unit	
Introduction	.05
Functional Description	
Operation	
Programming Model	
Register Overview 1	44
MIO Signals	.49
Chapter 7: Real Time Clock	
Introduction	51
Functional Description 1	.52
Calibration	56
External Clock Crystal and Circuitry 1	58
Battery Selection	L 5 9
RTC Register List	l61
Programming Model 1	.62
Programming Example – Periodic Alarm 1	.64

Chapter 8: Functional Safety	
Introduction	165
Safety Features overview	166
Chapter 9: System Monitors	
Introduction	170
Functional Description	
Operating Modes	
Programming Examples	
Register Sets	
System Interfaces	
Chapter 10: System Addresses	
• •	
Introduction	
System Address Register Overview	215
Chapter 11: Boot and Configuration	
Introduction	219
Boot Image Format	228
Functional Units	231
CSU BootROM Error Codes	233
PL Bitstream	239
Register Overview	242
Configuration Programming Model	244
Chapter 12: Security	
Introduction	248
Device and Data Security	249
Secure Boot	273
Chapter 13: Interrupts	
Introduction	298
System Interrupts	
GIC Interrupt System Architecture	
RPU GIC Interrupt Controller.	
APU GIC Interrupt Controller	
IPI Interrupts and Message Buffers	
GIC Proxy Interrupts	
CPU Private Peripheral Interrupts	
Register Overview	
-	

Programming Examples	324
Chapter 14: Timers and Counters	
Introduction	327
APU MPCore System Counter	329
APU Core Private Physical and Virtual Timers	331
Triple-timer Counters	335
System Watchdog Timers	343
MIO - EMIO Signals	356
Chapter 15: PS Interconnect	
Introduction	357
Block Diagram	358
ATB Timeout Description	363
AXI Performance Monitor	365
Programming Example – Metric Counter	369
Quality of Service	369
Interconnect Register Overview	376
Chapter 16: System Protection Units	
Introduction	378
TrustZone	383
SMMU Protection on CCI Slave Ports	391
XMPU Protection of Slaves	392
XMPU Register Set Overview	400
XPPU Protection of Slaves	401
Master IDs List	411
XPPU Register Set Overview	414
Programming Example	415
Write-Protected Registers Table	419
Security and Safety Errors	421
AIB Isolation Functionality	422
Chapter 17: DDR Memory Controller	
Introduction	424
System Block Diagram	429
DDR Subsystem Overview	434
Functional Description	447
Controller Initialization	449
Programming Toxics	453

Register Overview	483
Programming Model	495
Reading DRAM Configuration Mode Registers	512
Chapter 18: On-chip Memory	
Introduction	517
On-chip Memory Functional Description	518
On-chip Memory Register Overview	520
On-chip Memory Programming Model	521
Chapter 19: DMA Controller	
Introduction	523
DMA Controller Functional Description	
DMA Data Flow	
DMA Performance Requirements	
DMA Interrupt Accounting	
DMA Over Fetch	
DMA Transaction Control	
DMA Controller Register Overview	
DMA Programming for Data Transfer	
DMA Programming Model for FCI	
Chapter 20: CAN Controller	
·	
Introduction	
Functional Description	
Register Overview	
Programming Model	581
Chapter 21: UART Controller	
Introduction	590
UART Controller Functional Description	591
UART Controller Register Overview	604
MIO – EMIO Signals	605
UART Controller Programming Model	606
Chapter 22: I2C Controllers	
Introduction	610
Functional Description	
I/O Signals	
Pagistar Overview	615

Programming Model	616
Chapter 23: SPI Controller	
Introduction	633
Functional Description	
MIO-EMIO Signals	639
Register Overview	641
Programming Model	642
Chapter 24: Quad-SPI Controllers	
Introduction	640
System Control	
Generic Quad-SPI Controller	
Legacy Quad-SPI Controller	
Register Overview	
Programming and Usage Considerations	
Generic Quad-SPI Controller Programming	
Legacy Quad-SPI Controller Programming	
MIO Signals.	
Chapter 25: NAND Memory Controller	
Introduction	704
Functional Description	705
Register Overview	707
Clocks and Resets	709
I/O Signal Pins	709
Programming Model	712
Chapter 26: SD/SDIO/eMMC Controller	
Introduction	729
Functional Description	732
Clocks and Resets	736
I/O Signals	
Register Overview	752
Programming Examples	756
Chapter 27: General Purpose I/O	
Introduction	
	774
Functional Description	

MIO Signals	783
Programming Model	784
Chapter 28: Multiplexed I/O	
Introduction	789
MIO Pin Assignment Considerations	
MIO Table at a Glance	
Register Overview	
Programming Model	
Chapter 29: PS-GTR Transceivers	
Introduction	811
Functional Description	
Register Overview	
Configuration Program	
Comparation Togram	0_0
Chapter 30: PCI Express Controller	
Introduction	829
Functional Description	831
I/O Signals	860
Register Overview	861
Programming Topics	866
Chapter 31: USB Controller	
Introduction	881
Data Flow	885
Data Structure Network	886
Programming Guide	899
Device Programming	902
Register Overview	904
Chapter 32: SATA Controller	
Introduction	924
Functional Description	925
Register Overview	934
Programming Considerations	
Basic Steps When Building a Command	940
Command FIS (CFIS)	

Chapter 33: DisplayPort Controller
Introduction
Functional Description
Register Overview 98
Programming Considerations
MIO-EMIO Signals
Chapter 34: GEM Ethernet
Introduction
Functional Description
I/O Signals
Programming Model
Register Overview
Chapter 35: PS-PL AXI Interfaces
Introduction
Functional Description
Choosing a Programmable Logic Interface
Signal Overview
Register Overview
Chapter 36: PL Peripherals
Introduction
PCI Express Integrated
100G Ethernet
DisplayPort Video and Audio Interfaces
Interlaken
GTH and GTY Transceivers
PL System Monitor
Video Codec Unit
RFSoC
Chapter 37: PS Clock Subsystem
Introduction
System PLL Units
Basic Clock Generators
Special Clock Generators
Programming Examples
PLL Integer Divide Helper Data Table
Poristor Overview 114

napter 38: Reset System	
Introduction	1154
Functional Description	1155
Register Overview	1163
Programming Model	1163
napter 39: System Test and Debug	
Introduction	1166
JTAG Functional Description	1168
Arm DAP Controller	1178
CoreSight Functional Description	1181
CoreSight Address Map	1198
Clocks, Reset, and Power Domains	1201
I/O Signals	1203
MBIST, LBIST, and Scan Clear (Zeroization)	1205
ppendix A: Additional Resources and Legal Notices	
Finding Additional Documentation	1212
Support Resources	1213
References	1213
Arm References	1214
Revision History	1216
Please Read: Important Legal Notices	1235