FPGA Example Design: Xilinx Zynq Board

JITX Team

July 31, 2024

1 Project Goals and Future Prospects

1.1 Primary Objectives

- Develop an FPGA design of moderate complexity using JITX, serving as a comprehensive overview of the tool's capabilities.

- Utilize this design as a stress test to identify and resolve bugs in the JITX toolchain, while ensuring adequate performance.

- Create a compelling marketing asset: A Zynq-based board represents a significant engineering challenge. Successfully implementing this design demonstrates JITX's ability to handle complex projects, appealing to professionals already working with the Zynq platform and those engaged in projects of similar complexity.

1.2 Future Enhancements

- Refactor the codebase to improve reusability and parameterization, with the ultimate goal of integrating it into the JSL library.

- Expand the design to interface with a VPX backplane, contingent upon the development of a VPX backplane generator. This addition would transform the project into a highly attractive example for specific industry players, such as Lockheed-Martin.

- Potential to evolve into a world-class VPX backplane solution, further enhancing JITX's market position in specialized, high-performance computing applications.
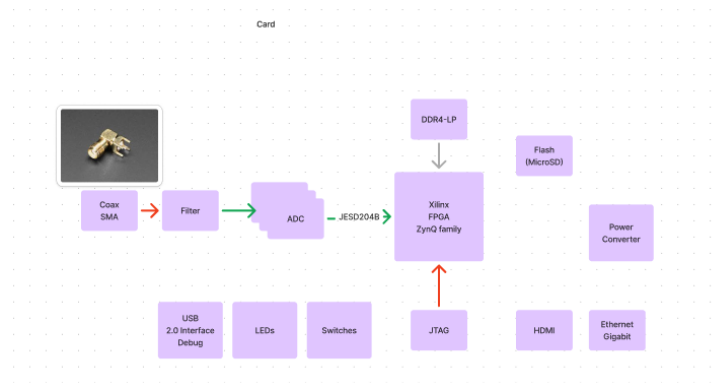
Figure 1: Block diagram of the Zynq FPGA-based Design