AMD

Chapter 2

Signals, Interfaces, and Pins

Introduction

The dedicated device pins and the major signals and interfaces that cross between Programmable Logic (PL) and Processing System (PS) power domains are listed in this chapter. Figure 2-1 shows the dedicated device pins, and the signals and interfaces between power domains.

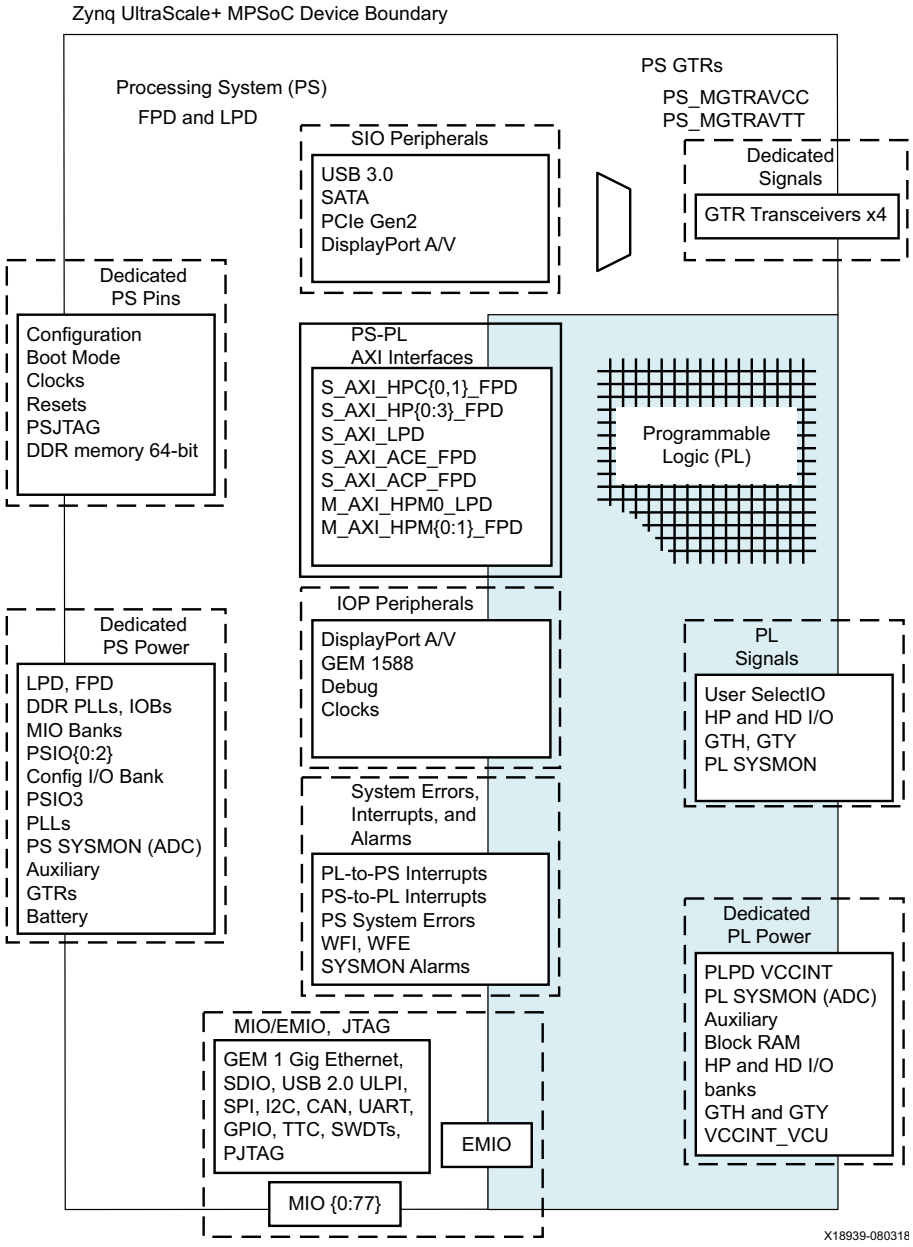

Figure 2-1: **PS Pins and Interfaces Diagram**

Dedicated Device Pins

The dedicated device pins are divided into these groups:

- Power.
- Clock, reset, and configuration.
- JTAG interfaces.
- Multiplexed I/O (MIO).
- PS GTR serial channels.
- DDR I/O (see Table 17-3 in DDR PHY Features in Chapter 17).

Power Pins

The dedicated power pins for the PS and internal logic of the PL are listed in Table 2-1. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) [Ref 2] for specifications.

Table 2-1: **Power Pins**

Pin Name	Description
VCC_PSINTLP	PS low-power domain (LPD) supply voltage.
VCC_PSINTFP	PS full-power domain (FPD) supply voltage.
VCC_PSAUX	PS auxiliary voltage.
VCC_PSBATT	PS battery operated voltage.
VCC_PSPLL	LPD PLLs: RPLL (RPU), IOPLL (I/O). FPD PLLs: APLL (APU), VPLL (video), DPLL (DDR controller).
VCC_PSDDR_PLL	DDR PLLs supply voltage for DDRIOB. When PS DDR is not used, tie to ground.
VCC_PSINTFP_DDR	DDR memory controller supply voltage. Tie to VCC_PSINTFP.
VCCO_PSDDR	PS DDR I/O supply voltage. When PS DDR is not used, tie to ground.
VCCO_PSIO[0:3]	Power supply voltage for the PS I/O banks. • VCCO_PSIO[0] is bank 500. MIO pins 0 to 25. • VCCO_PSIO[1] is bank 501. MIO pins 26 to 51. • VCCO_PSIO[2] is bank 502. MIO pins 52 to 77. • VCCO_PSIO[3] is bank 503. Mode, config, PSJTAG, error, SRST, POR, PS_REF_CLK.
VCCINT	PL power domain (PLPD) supply voltage.
VCCINT_VCU	Video codec unit supply voltage.
VCCAUX	PL auxiliary voltage.
VCCBRAM	PL block RAM supply voltage.
PS_MGTRAVCC	PS-GTR $V_{MGTAVCC}$ supply voltage.

Table 2-1: **Power Pins *(Cont'd)***

Pin Name	Description
PS_MGTRAVTT	PS GTR $V_{MGTAVTT}$ termination voltage.
VCC_PSADC	PS System Monitor analog voltage.
VCCADC	PL System Monitor analog voltage.

Clock, Reset, and Configuration Pins

The clock pins include the main PS reference clock input and the clock crystal connections to the real-time clock (RTC) in the battery power domain. The reset and configuration pins control the device and provide status information.

Table 2-2: **Clock, Reset, and Configuration Pins**

Pin Name	Direction	Type	Description
PS_REF_CLK	Input	Dedicated	System reference clock.
PS_PADI	Input	Dedicated	Crystal pad input (RTC).
PS_PADO	Output	Dedicated	Crystal pad output (RTC).
PS_POR_B	Input	Dedicated	Power-on reset signal.
POR_OVERRIDE	Input	Dedicated	POR delay override. 0 = Standard PL power-on delay time(1) (recommended default). 1= Faster PL power-on delay time.(1) Do not allow this pin to float before and during configuration. This pin must be tied to VCCINT or GND.
PS_SRST_B	Input	Dedicated	System reset commonly used during debug.
PS_MODE	Input/Output	Dedicated	4-bit boot mode pins sampled on POR deassertion.
PS_INIT_B	Input/Output	Dedicated	Indicates the PL is initialized after a power-on reset (POR). This signal should not be held Low externally to delay the PL configuration sequence because the signal level is not visible to software. However, if there is a CRC error detected when the PL bitstream is loaded PS_INIT_B will be driven low.
PS_DONE	Output	Dedicated	Indicates the PL configuration is completed. Requires an external pull-up resistor.
PS_PROG_B	Input/Output	Dedicated	PL configuration reset signal.
PS_ERROR_OUT	Output	Dedicated	Asserted for accidental loss of power, a hardware error, or an exception in the PMU.
PS_ERROR_STATUS	Output	Dedicated	Indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.

Table 2-2: **Clock, Reset, and Configuration Pins *(Cont'd)***

Pin Name	Direction	Type	Description
PS_MGTREFCLK[3:0]	Input	Dedicated	Reference clock for the PS-GTR transceivers.
PUDC_B	Input	Dedicated	Pull-Up During Configuration (bar) Dedicated input pin. Active-Low input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. Caution! Do not allow this pin to float before and during configuration. Must be tied High or Low. PUDC_B must be tied either directly or via a ≤ 1 k Ω resistor to VCCAUX or GND.

Notes:

1. The T_{POR} specification begins when the last of the monitored supplies (VCCINT, VCCAUX, VCCBRAM) reaches 95% of its recommended operating condition voltage.

JTAG Interfaces

There are two JTAG port interfaces: PSJTAG and PJTAG. The PSJTAG port can reach all TAP controllers on the chain. The signals are on the device pins listed in Table 2-3.

The PJTAG interface port provides exclusive access to the Arm DAP controller. The PJTAG interface signals on MIO are listed in Table 28-2.

PSJTAG is discussed in Chapter 39, System Test and Debug.

Table 2-3: **PS JTAG Interface Pins**

Pin Name	Direction	Description
PS_JTAG_TCK	Input	JTAG data clock.
PS_JTAG_TDI	Input	JTAG data input.
PS_JTAG_TDO	Output	JTAG data output.
PS_JTAG_TMS	Input	JTAG mode select.

MIO Pins

The PS uses the MIOs as described in Chapter 28, Multiplexed I/O. The MIO pins are configured by accessing registers located in the IOU_SLCR register set. The default routing for the peripheral I/O signals is through the EMIO interface to the PL fabric. The pin availability for the I/O controller is often different between routing to the MIO pins versus the EMIO interface to the PL.

Table 2-4: **MIO Pins**

Pin Name	Type	Direction	Description
PS_MIO[0:77]	Configurable pins, see Table 28-2	Input/Output	Multiplexed I/Os are configured for the IOP controllers and other interfaces: SPI, QSPI, NAND, USB 2.0 ULPI, GEM Ethernet RGMII, SDIO, UART, GPIO, MDIO, SWDT, TTC, TPIU, PJTAG.

DDR Memory Controller I/O

The DDR memory controller pins are described in Table 17-3 in Chapter 17, DDR Memory Controller.

PS GTR Serial Channel Device Pins

There are four pairs of gigabit serial device pins. These connect to the PCIe, SATA, and USB 3.0 signals from the controllers in the PS. The GTR serial channels are described in Chapter 29, PS-GTR Transceivers.

PS-PL Signals and Interfaces

The PS and PL can be tightly coupled in a heterogeneous processing system using the many signals and interfaces between the LPD and FPD in the PS and the functionality configured in the PL. The PL can also be independently isolated from the LPD and FPD regions using isolation walls. The PS-PL signals and interfaces also include other functions to configure and control the device. The PS-PL signals and interfaces include these groups:

- PS-PL Voltage Level Shifters
- Processor communications
- System error signals
- MIO-EMIO signals and interfaces
- Miscellaneous signals and interfaces
- Dedicated stream interfaces
- DisplayPort media interfaces
- Clock signals
- Timer signals
- System debug signals and interfaces

The PS-PL signal and interface names are listed in the *Zynq UltraScale+ MPSoC Processing System LogiCORE IP Product Guide* (PG201) [Ref 27].

PS-PL Voltage Level Shifters

The PS communicates with the PL using voltage level shifters. All of the signals (input and output) and interfaces between the PS and PL traverse a voltage boundary and are routed through voltage-level shifters. Some of the voltage-level shifter enables are controlled by the PL power state including the signals for the PL, the EMIO JTAGs, the PCAP interface, and other modules. The PL is treated as a separate power domain (PLPD). The AXI interfaces are isolated using isolation blocks. To enable an PS-PL AXI interface, the PS-PL isolation must be disabled by making a PMU service request using the PMU_GLOBAL[REQ_PWRUP_INT_EN] bit.

Processor Communications

Table 2-5 lists the processor communications signals. See Table 35-7 in Chapter 35, PS-PL AXI Interfaces for additional information.

Table 2-5: **Processor Communications**

Signal Name	Count	Source	Destination	Description
P2F PMU signal	32 signals	LPD	PL	GPO3 register signals to PL.(1)
F2P PMU signal	32 signals	PL	LPD	GPI3 register signals from PL.(1)
APU wake up	2 signals	PL	FPD	APU WFE and WFI event and interrupt status.
IRQ_P2F_PL_IPIx	4 channels	LPD	PL	IPI interrupts to PL targets.
IRQ_F2P_PL_IPIx	7 channels	PL	LPD	IPI interrupts to PS targets.
PL IRQs	16 signals	PL	LPD, FPD	IRQ signals from PL to GICs.
RPU CPU IRQs	4 signals	PL	LPD	FIQ, IRQ interrupts for each core.
APU CPU IRQs	8 signals	PL	FPD	FIQ, IRQ interrupts for each core.
PS System IRQs	>100 signals	PS	PL	PS generated interrupts to GICs and PL.
LPD IOP interrupts	100	LPD	PL	From peripherals to GICs and PL. See Table 13-1.
FPD IOP interrupts	64	FPD	PL	From peripherals to GICs and PL. See Table 13-1.
Events	~	LPD, FPD	PL	Events from RPU and APU.

Notes:
1. Software environments might assign meaning to the GPI and GPO signals of the PMU.

System Error Signals

Table 2-6 lists the system error signals.

Table 2-6: **System Error Signals**

Name	Count	Source	Destination	Description
System errors	49	PS	PL (and PS)	System error signals.
P2F PMU error	4	PMU	PL (and PS)	PMU output error signal.
F2P PMU error	4	PL	PMU	PMU input error signal.

MIO-EMIO Signals and Interfaces

The MIO device pins are fundamental to the I/O connections for the LPD IOP controllers. Software routes the controllers I/O signals to the MIO pins using IOU_SLCR registers. When there are not enough MIO pins for the peripheral I/O, then the EMIO can be used to connect signals to PL I/O device pins and logic within the PL. Table 2-7 lists the MIO-EMIO signals and interfaces.

RECOMMENDED: *The routing of the IOP interface I/O signals must be configured as a group. That is, the signals within an interface must not be split and routed to different MIO pin groups. For example, if the SPI 0 CLK is routed to MIO pin 40, then the other signals of the SPI 0 interface must be routed to MIO pins 41 to 45. Similarly, the signals within an IOP interface must not be split between MIO and EMIO. However, unused signals within an IOP interface do not necessarily need to be routed. Each unused MIO pin can be configured as a GPIO.*

Table 2-7: **MIO-EMIO Signals and Interfaces**

Interface	MIO Access	EMIO Access	Notes
GEM{0:3}	RGMII	GMII	MIO: 4-bit RGMII v2.0, external PHY, 250 MHz data rate. EMIO: 8-bit GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, 1000BASE-SX, and 1000BASE-LX in PL, 125 MHz data rate.
SDIO{0, 1}	Yes	Yes	The SDIO interface performance is reduced when using the EMIO interface.
USB{0, 1}	USB 2.0 to external ULPI PHY.	No	The USB 3.0 interface is routed to a GTR channel
I2C{0, 1}	Yes	Yes	
SPI{0, 1}	Yes	Yes	The SPI interface performance is reduced when using the EMIO interface.
UART{0, 1}	Yes (RX, TX)	Yes (RX, TX, modem signals).	
CAN{0, 1}	Yes	Yes	External PHY.
GPIO Banks {0:2}	Yes (up to 78)	No	
GPIO Banks {3:5}	No	Yes (up to 96)	Input, output, and 3-state control.
Quad-SPI	Yes	No	
NAND	Yes	No	
LPD_SWDT, FPD_SWDT	Yes	Yes	Reset and output pulse.
CSU_SWDT	No	No	
TPIU Trace	Up to 16 bits	Up to 32 bits	

Miscellaneous Signals and Interfaces

Table 2-8 lists the miscellaneous signals and interfaces. For details, see Table 34-1, Table 34-2, and Table 34-3.

Table 2-8: **Miscellaneous Signals and Interfaces**

Name	Count	Source	Destination	Description
GEM FIFO	87 (x4)	GEM, PL	GEM, PL	Ethernet RX and TX FIFO packet streams.
GEM 1588	136	GEM, PL	GEM, PL	Ethernet 94-bit IEEE 1588 timestamp read by PL interface, PTP event frame interface, and timestamp clock interface.
DDR Refresh Req	2	PL	FPD	DDR memory controller external refresh request signals.
DDR Refresh Clk	1	PL	FPD	DDR memory controller refresh clock.
SEU error alarm	1	PL	CSU	Single event upset error alarm from the PL.
LPD DMA flow control	5	PL	LPD, PL clock, valids, acknowledges	See Figure 19-4.
FPD DMA flow control	5	PL	FPD, PL clock, valids, acknowledges	See Figure 19-4.

Dedicated Stream Interfaces

The GEM provides packet interface and support for the IEEE Std 1588 in the PL. The packet streaming interface (FIFO interface) from the GEM (bypassing the DMA) is available to the PL for implementation of additional functionality like packet inspection or audio-video broadcast (AVB). Additional signals for supporting the IEEE Std 1588 are also available to the PL. For details on this interface, refer to Chapter 34, GEM Ethernet.

The DisplayPort streaming interface for video and audio to/from the PL provides video and audio interfaces to the PL. It can take video/audio input from the PL and direct video/audio output to the PL. For details on this interface, refer to Chapter 33, DisplayPort Controller.

DisplayPort Media Interfaces

The DisplayPort streaming interface for video and audio to or from the PL provides video and audio interfaces to the PL. It can take video or audio input from the PL and direct video or audio output to the PL. For details on this interface, see Chapter 33, DisplayPort Controller. Table 2-9 lists the PS-PL DisplayPort media interfaces.

Table 2-9: **DisplayPort Media Interfaces**

Name	Count	Source	Destination	Description
Audio	77	PS, PL	PS, PL	One 32-bit audio input interface. One 32-bit audio output interface.
Video	154	PS, PL	PS, PL	Two 36-bit video streams to PS for overlay. One 36-bit video stream to PL display controller (e.g, HDMI, VGA, MIPI).

Clock Signals

Table 2-10 lists the clock signals.

Table 2-10: **Clock Signals**

Name	Count	Source	Destination	Description
PL_CLK{0:3}	4	LPD	PL	PS clock subsystem to PL fabric.
F2P clocks	2	PL	LPD	PS to PL auxiliary reference clocks.
RTC clock	1	LPD	LPD	RTC clock oscillator signal.

Timer Signals

Table 2-11 lists the timer signals.

Table 2-11: **Timer Signals**

Name	Count	Source	Destination	Description
TTC{0:3}_CLK	4	EMIO, MIO	LPD	Triple time counter optional clock sources.
TTC{0:3}_WAVE	4	LPD	EMIO, MIO	Triple timer counter waveform signal destinations.
WDT0_CLK	1	EMIO, MIO	LPD	LPD SWDT optional clock sources.
WDT1_CLK	1	EMIO, MIO	FPD	FPD SWDT optional clock sources.
WDT0_RST	1	LPD	GICs, EMIO, MIO	LPD SWDT reset signal destinations.
WDT1_RST	1	FPD	GICs, EMIO, MIO	FPD SWDT reset signal destinations.

System Debug Signals and Interfaces

Table 2-12 lists the system debug signals and interfaces.

Table 2-12: **System Debug Signals and Interfaces**

Name	Count	Description
CTI	48	CoreSight cross-trigger Interface.
TPIU	36	CoreSight trace-port interface.
FTM	118	Fabric trace module.
STM event		CoreSight system trace macrocell.

PS-PL AXI Interfaces

The PS-PL AXI interfaces are summarized in Table 2-13. These interfaces are described in Chapter 35, PS-PL AXI Interfaces.

Table 2-13: **PS-PL AXI Interfaces Summary**

Interface Name	Abbreviation	FIFO Interface	Master	Usage Description
S_AXI_HP{0:3}_FPD	HP{0:3}	AFI_{2:5}	PL	Non-coherent paths from PL to FPD main switch and DDR. No L2 cache allocation.
S_AXI_LPD	PL_LPD	AFI_6	PL	Non-coherent path from PL to IOP in LPD.
S_AXI_ACE_FPD	ACE	None	PL	Two-way coherent path between memory in PL and CCI.
S_AXI_ACP_FPD	ACP	None	PL	Legacy coherency. I/O coherent with L2 cache allocation.
S_AXI_HPC{0, 1}_FPD	HPC{0, 1}	AFI_{0:1}	PL	I/O coherent with CCI. No L2 cache allocation.
M_AXI_HPM{0, 1}_FPD	HPM{0, 1}	None	PS	FPD masters to PL slaves.
M_AXI_HPM0_LPD	LPD_PL	None	PS	LPD masters to PL slaves.