EC311/Introduction to Logic Design
Fall 2025

Class: Mon and Wed 12:20 pm to 2:05 pm in PHO 203
Labs: Mon 10:10 am to 11:55 am, Tue 9 am to 10:45 am, Wed 4:30 pm to 6:15 pm,
Thu 3:30 pm to 5:15 pm, and Fri 12:20 pm to 2:05 pm in PHO 115.

Course Objective

The class covers the theory and practice of digital hardware design. Students will learn to formulate real-world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they will also learn fundamental logic design and verification skills using Verilog HDL and FPGAs.

Staff Information

Instructor:
Ajay Joshi
Email: joshi@bu.edu (Include EC311 in the subject line).
Office Hours: Friday 9 am to 10 am or by appointment in PHO 334.

GTFs:
Lohit Daksha
Email: tihol@bu.edu (Include EC311 in the subject line).
Office Hours: Tuesday and Thursday 6:30 pm to 7:30 pm or by appointment in PHO 115.

UTFs
Alice Badareen badareen@bu.edu
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Textbooks and Class Material

– Digital Design, 6th Edition, Mano and Ciletti, Pearson (5th edition is also acceptable).
– Starter's Guide to Verilog 2001, Ciletti. Pearson.

Class Websites

- Blackboard (http://learn.bu.edu) for lecture notes, homeworks, labs, exams, etc.
- Piazza (https://piazza.com/) for asking questions.
- Gradescope (https://www.gradescope.com/) for quizzes, homeworks, and exams.

Course Goals

To provide students with:

- An experience with digital logic design and implementation.
- An understanding of the CAD tools used for logic design.
- An understanding of sound logic design methodologies.

Course Outcomes

As an outcome of completing this course, students should be able to:

- Understand the applications of logic design.
- Understand abstraction and hierarchy in digital design.
- Understand what components are available for logic design.
- Understand the use of Boolean algebra in logic analysis and design.
- Understand logic minimization criteria and methods for use in design.
- Understand the concept of state in digital systems.
- Design combinational digital logic systems given specifications.
- Design sequential digital logic systems (finite state machines) given specifications.
- Implement logic designs in hardware and with CAD tools.
- Discover component availability and data using the Internet or other resources.

Evaluation

Grading

Two mid-term exams: 20% each, Final exam: 30%, Project: 10%, Labs: 15%, In-class quizzes: 5%.

Exams

The two mid-term exams will be during class time. Final exam will be on Dec 17 from 12 noon to 2 pm.

Project

We will do a group project at the end of the semester. Each group will consist of 4-5 students. Details of the project will be provided at a later date.

Labs

Lab assignments will be posted on the Blackboard website. Grades will be assigned to completed labs. Students are expected to attend their scheduled lab section every week. No credit will be given for late submission of lab assignments.

Homeworks

Homework assignments will be posted on the Blackboard website.

Course Policies

Exam/Lab Grade discussion:

Grade discussion/corrections should be done within one week after the graded exam or lab is distributed. No grade changes will be made after one week.

Collaboration Policy:

In this class, you may use any textbooks or web sources and/or human collaborators (from class) for your work, subject to the following strictly enforced conditions:

- You must clearly acknowledge all your sources (including your collaborator).
- You must write all answers in your own words.
- You must be able to fully explain your answers upon demand (and I will demand it!).

- You may not use any human resource outside of class in doing your work. Obviously, you may not collaborate with anyone on exams.

Failure to meet any of the above conditions could constitute plagiarism and will be considered cheating in this class. If you are not sure whether something is permitted by the course policy, ASK ME! (it's much more awkward to explain your actions after the fact to the College Disciplinary Committee).

Academic integrity:

- Boston University's academic code of conduct will be strictly applied.
- Boston University's computing ethics will be strictly applied.

Course Schedule (tentative)

Lecture Number	**Date**	**Lecture Topic & Reading Chapters**	**In-class Quiz**	**Homework Out**	**Lab Out**
1	Sep 3	Introduction (1.1-1.6)			
2	Sep 8	Binary arithmetic (1.6-1.9)		Hw1	Pre-Lab A
3	Sep 10	Boolean algebra, canonical forms (2.1-2.8)			
4	Sep 15	K-Maps, logic minimization (3.1-3.8)	Q1	Hw 2	Pre-Lab B
5	Sep 17	Verilog			
6	Sep 22	Combinational logic (4.1-4.5)	Q2	Hw 3	Lab 1
7	Sep 24	Adders, multipliers, (4.5-4.8)			
8	Sep 29	Decoder, encoders (4.9-4.10)	Q3	Hw 4	
9	Oct 1	Comparators (4.9-4.10)			
10	Oct 6	MUXes, tri-state (4.10-4.12)	Q4		
11	Oct 8	Synchronous sequential logic: latches and FFs (5.1-5.4)			
12	Oct 14	**Exam 1**			

Lecture Number	Date	Lecture Topic	Reading Chapters (Mano)	Homework Out	Lab Out
13	Oct 15	Synchronous sequential logic: latches and FFs (5.1-5.4)			Lab 2
14	Oct 20	State machines (5.5-5.8)	Q5	Hw5	
15	Oct 22	State machines (5.5-5.8)			
16	Oct 27	State machines (5.5-5.8)	Q6	Hw 6	
17	Oct 29	Registers (6.1-6.3)			
18	Nov 3	Counters (6.4-6.6)	Q7	Hw 7	
19	Nov 5	Memory (7.1-7.2)			
20	Nov 10	Error codes (7.3-7.4)	Q8	Hw 8	
21	Nov 12	ROM, PLD, PLA, PAL (7.5-7.8)			
22	Nov 17	Processor basics	Q9		
23	Nov 19	Processor basics			
24	Nov 24	**Exam 2**			
25	Dec 1	Miscellaneous Topics			
26	Dec 3	Miscellaneous Topics	Q10		
27	Dec 8	Project presentations			
28	Dec 10	Project presentations			
	Dec 17	Final Exam			