COEN 313
Speculative Execution HW

3.15

1. Not pipelined

Iteration	Instruction	Issues	Completes	Commits	Mem access (loads)	Write CDB
1	fld	3	4	5	6	7
1	fmul.d	4	19	20		21
1	fld	5	6	21	22	23
1	fadd.d	6	16	22		23
1	fsd	7	19	23		24
1	addi	8	9	24		25
1	addi	9	10	25		26
1	sltu	10	11	26		27
1	bnez	11	12	27		28
2	fld	12	13	28	29	30
2	fmul.d	20	35	36		37
2	fld	21	36	37	38	39
2	fadd.d	22	32	38		39
2	fsd	23	35	39		40
2	addi	24	25	40		41
2	addi	25	26	41		42
2	sltu	26	27	42		43
2	bnez	27	28	43		44
3	fld	28	29	30	31	32
3	fmul.d	36	51	52		53

3	fld	37	38	53	54	55
3	fadd.d	38	48	54		55
3	fsd	39	51	55		56
3	addi	40	41	56		57
3	addi	41	42	57		58
3	sltu	42	43	58		59
3	bnez	43	44	59		60

ROB:

Entry	Instruction	Destination	Value
1	fld	F2	Mem[0+Regs[x1]]
2	fmul.d	F4	#1 * Regs[F0]
3	fld	F6	Mem[0+Regs[x2]]
4	fadd.d	F6	#2 + #3
5	fsd	0 + Regs[x2]	#4
6	addi	x1	Regs[x1] + 8
7	addi	x2	Regs[x2] + 8
8	sltu		
9	bnez		
10	fld	F2	Mem[#6]
11	fmul.d	F4	#10 * Regs[F0]
12	fld	F6	Mem[#7]
13	fadd.d	F6	#11 + #12
14	fsd	0 + #7	#13
15	addi	x1	#6 + 8
16	addi	x2	#7 + 8

17	sltu		
18	bnez		
19	fld	F2	Mem[#15]
20	fmul.d	F4	#19 * Regs[F0]
21	fld	F6	Mem[#16]
22	fadd.d	F6	#20 + #21
23	fsd	0 + #7	#22
24	addi	x1	#15 + 8
25	addi	x2	#16 + 8
26	sltu		
27	bnez		

Reservation Tables:
1st iteration:

	Integer		FP adder		FP multiplier		Load		Store
~~I0~~	~~x1 8 R6~~	A0	F4 F6 R4	M0	F2 F0 R2	~~L0~~	~~x1 0 R1~~	S0	x2 A0 R5
~~I0~~	~~x2 8 R7~~	A1		M1		~~L0~~	~~x2 0 R3~~	S1	
I0		A2				L0		S2	
I1						L1		S3	
I2						L2		S4	

2nd iteration:

	Integer		FP adder		FP multiplier		Load		Store
~~I0~~	~~x1 8 R15~~	~~A0~~	~~F4 F6 R4~~	~~M0~~	~~F2 F0 R2~~	~~L0~~	~~x1 0 R10~~	~~S0~~	~~x2 A0 R5~~

~~I0~~	~~x2 8 R16~~	A1	F4 F6 R13	M1	F2 F0 R11	~~L0~~	~~x2 0 R12~~	S1	x2 A1 R14
I0		A2				L0		S2	
I1						L1		S3	
I2						L2		S4	

3rd iteration:

	Integer		FP adder		FP multiplier		Load		Store
~~I0~~	~~x1 8 R24~~	A0	F4 F6 R22	M0	F2 F0 R20	~~L0~~	~~x1 0 R19~~	S0	x2 A0 R23
~~I0~~	~~x2 8 R25~~	~~A1~~	~~F4 F6 R13~~	~~M1~~	~~F2 F0 R11~~	~~L0~~	~~x2 0 R21~~	~~S1~~	~~x2 A1 R14~~
I0		A1				L0		S1	
I1						L1		S2	
I2						L2		S4	

2. Pipelined

Iteration	Instruction	Issues	Completes	Commits	Mem access (loads)	Write CDB
1	fld	3	4	5	6	7
1	fmul.d	4	19	20		21
1	fld	5	6	21	22	23
1	fadd.d	6	16	22		23
1	fsd	7	19	23		24
1	addi	8	9	24		25
1	addi	9	10	25		26

1	sltu	10	11	26		27
1	bnez	11	12	27		28
2	fld	12	13	28	29	30
2	fmul.d	13	28	29		30
2	fld	21	29	30	31	32
2	fadd.d	22	32	33		34
2	fsd	23	35	36		37
2	addi	24	25	37		38
2	addi	25	26	38		39
2	sltu	26	27	39		40
2	bnez	27	28	40		41
3	fld	28	29	41	42	43
3	fmul.d	29	44	45		46
3	fld	37	45	46	47	48
3	fadd.d	38	48	49		50
3	fsd	39	51	52		53
3	addi	40	41	53		54
3	addi	41	42	54		55
3	sltu	42	43	55		56
3	bnez	43	44	56		57

ROB (same as above)

Entry	Instruction	Destination	Value
1	fld	F2	Mem[0+Regs[x1]]
2	fmul.d	F4	#1 * Regs[F0]
3	fld	F6	Mem[0+Regs[x2]]

4	fadd.d	F6	#2 + #3
5	fsd	0 + Regs[x2]	#4
6	addi	x1	Regs[x1] + 8
7	addi	x2	Regs[x2] + 8
8	sltu		
9	bnez		
10	fld	F2	Mem[#6]
11	fmul.d	F4	#10 * Regs[F0]
12	fld	F6	Mem[#7]
13	fadd.d	F6	#11 + #12
14	fsd	0 + #7	#13
15	addi	x1	#6 + 8
16	addi	x2	#7 + 8
17	sltu		
18	bnez		
19	fld	F2	Mem[#15]
20	fmul.d	F4	#19 * Regs[F0]
21	fld	F6	Mem[#16]
22	fadd.d	F6	#20 + #21
23	fsd	0 + #7	#22
24	addi	x1	#15 + 8
25	addi	x2	#16 + 8
26	sltu		
27	bnez		

Reservation Tables:
1st iteration:

	Integer		FP adder		FP multiplier		Load		Store
~~I0~~	~~x1 8 R6~~	A0	F4 F6 R4	M0	F2 F0 R2	~~L0~~	~~x1 0 R1~~	S0	x2 A0 R5
~~I0~~	~~x2 8 R7~~	A1		M1		~~L0~~	~~x2 0 R3~~	S1	
I0		A2				L0		S2	
I1						L1		S3	
I2						L2		S4	

2nd iteration:

	Integer		FP adder		FP multiplier		Load		Store
~~I0~~	~~x1 8 R15~~	~~A0~~	~~F4 F6 R4~~	~~M0~~	~~F2 F0 R2~~	~~L0~~	~~x1 0 R10~~	~~S0~~	~~x2 A0 R5~~
~~I0~~	~~x2 8 R16~~	A1	F4 F6 R13	M1	F2 F0 R11	~~L0~~	~~x2 0 R12~~	S1	x2 A1 R14
I0		A2				L0		S2	
I1						L1		S3	
I2						L2		S4	

3rd iteration:

	Integer		FP adder		FP multiplier		Load		Store
~~I0~~	~~x1 8 R24~~	A0	F4 F6 R22	M0	F2 F0 R20	~~L0~~	~~x1 0 R19~~	S0	x2 A0 R23
~~I0~~	~~x2 8 R25~~	~~A1~~	~~F4 F6 R13~~	~~M1~~	~~F2 F0 R11~~	~~L0~~	~~x2 0 R21~~	~~S1~~	~~x2 A1 R14~~
I0		A1				L0		S1	
I1						L1		S2	

I2		[redacted]	L2		S4	