31	27	26	25	24	20	19	1.	5 14	12	11		7	6	0	
	funct7				rs2		rs1	fur	ct3		$\operatorname{rd}$		opo	$\operatorname{ode}$	R-type
	ir	nm[]	11:0	)]			rs1	fur	$\cot 3$		$\operatorname{rd}$		opo	$\operatorname{ode}$	I-type
i	mm[11:	5]			rs2		rs1	fur	$\cot 3$	in	$\mathrm{nm}[4:0]$	0]	ope	$\operatorname{code}$	S-type
im	m[12 10]	0:5]			rs2		rs1	fur	$\cot 3$	imı	n[4:1]	11]	opo	ode	B-type
imm[31:12]											$\operatorname{rd}$		opo	ode	U-type
			imn	n[20	10:1 11	[9:12]					$\operatorname{rd}$		opo	$\operatorname{ode}$	J-type

# RV32I Base Instruction Set

	imm[31:12]			rd	0110111	LUI
	imm[31:12]			rd	0010111	AUIPC
im	m[20 10:1 11 1]	9:12]	000	rd	110 <mark>11111</mark>	$ brack  ext{JAL}$
imm[11:	imm[11:0]			rd	1100111	JALR
imm[12 10:5]	rs2	rs1	000	imm[4:1 11]	1100011	$\overline{\mathrm{BEQ}}$
imm[12 10:5]	rs2	rs1	001	imm[4:1 11]	1100011	BNE
imm[12 10:5]	rs2	rs1	100	imm[4:1 11]	1100011	BLT
imm[12 10:5]	rs2	rs1	101	imm[4:1 11]	1100011	$\overline{\text{BGE}}$
imm[12 10:5]	rs2	rs1	110	imm[4:1 11]	1100011	BLTU
imm[12 10:5]	rs2	rs1	111	imm[4:1 11]	1100011	BGEU
imm[11:	0]	rs1	000	rd	0000011	LB
imm[11:	[0]	rs1	001	rd	0000011	LH
imm[11:		rs1	010	rd	0000011	LW
imm[11:	[0]	rs1	100	rd	0000011	LBU
imm[11:	[0]	rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	ceil SB
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:	imm[11:0]		000	rd	0010011	ADDI
imm[11:	[0]	rs1	010	rd	0010011	SLTI
imm[11:	[0]	rs1	011	rd	0010011	SLTIU
imm[11:	[0]	rs1	100	rd	0010011	XORI
imm[11:	[0]	rs1	110	rd	0010011	ORI
imm[11:	[0]	rs1	111	rd	0010011	ANDI
0000000	shamt	rs1	001	rd	0010011	SLLI
0000000	shamt	rs1	101	rd	0010011	SRLI
0100000	shamt	rs1	101	rd	0010011	$\overline{SRAI}$
0000000	rs2	rs1	000	$\operatorname{rd}$	0110011	ADD
0100000	rs2	rs1	000	$\operatorname{rd}$	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rs1	010	rd	0110011	SLT
0000000	rs2	rs1	011	rd	0110011	SLTU
0000000	rs2	rs1	100	rd	0110011	XOR
0000000         rs2           0100000         rs2           0000000         rs2           0000000         rs2           fm         pred         succ		rs1	101	rd	0110011	SRL
		rs1	101	$\operatorname{rd}$	0110011	SRA
		rs1	110	$\operatorname{rd}$	0110011	OR
		rs1	111	rd	0110011	AND
		rs1	000	$\operatorname{rd}$	0001111	FENCE
000000000		00000	000	00000	1110011	ECALL
000000000	00000	000	00000	1110011	BREAK	

31	27	26	25	24	:	20	19	15	14	12	11	7	6	0	
	funct7				rs2		rs1		func	et3	re	d	ope	code	R-type
	ir	nm[	11:0	)]			rs1		func	et3	r	l	ope	code	I-type
i	mm[11:	5]			rs2		rs1		func	et3	imm	[4:0]	ope	code	S-type

#### RV64I Base Instruction Set (in addition to RV32I)

	`			,	
imm[11:0]			rd	0000011	LWU
1:0]	rs1	011	rd	0000011	LD
rs2	rs1	011	imm[4:0]	0100011	SD
shamt	rs1	001	rd	0010011	SLLI
$\operatorname{shamt}$	rs1	101	rd	0010011	SRLI
shamt	rs1	101	rd	0010011	SRAI
1:0]	rs1	000	rd	0011011	ADDIW
shamt	rs1	001	rd	0011011	SLLIW
shamt	rs1	101	rd	0011011	SRLIW
shamt	rs1	101	rd	0011011	SRAIW
rs2	rs1	000	rd	0111011	ADDW
rs2	rs1	000	rd	0111011	SUBW
rs2	rs1	001	rd	0111011	SLLW
rs2	rs1	101	rd	0111011	SRLW
rs2	rs1	101	$\operatorname{rd}$	0111011	SRAW
	1:0]    rs2     shamt     shamt     shamt     shamt     shamt     shamt     shamt     rs2     rs2     rs2     rs2     rs2	1:0]         rs1           rs2         rs1           shamt         rs1           shamt         rs1           shamt         rs1           1:0]         rs1           shamt         rs1           shamt         rs1           shamt         rs1           rs2         rs1           rs2         rs1           rs2         rs1           rs2         rs1           rs2         rs1           rs2         rs1	1:0]         rs1         011           shamt         rs1         001           shamt         rs1         101           shamt         rs1         101           shamt         rs1         000           shamt         rs1         001           shamt         rs1         101           shamt         rs1         101           rs2         rs1         000           rs2         rs1         000           rs2         rs1         001           rs2         rs1         101           rs2         rs1         101	1:0]         rs1         011         rd           rs2         rs1         011         imm[4:0]           shamt         rs1         001         rd           shamt         rs1         101         rd           shamt         rs1         101         rd           1:0]         rs1         000         rd           shamt         rs1         101         rd           shamt         rs1         101         rd           rs2         rs1         000         rd           rs2         rs1         000         rd           rs2         rs1         001         rd           rs2         rs1         001         rd           rs2         rs1         101         rd	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

## RV32/RV64 Zifencei Standard Extension

imm[11:0]	rs1	001	$\operatorname{rd}$	0001111	FENCE.I

#### RV32/RV64 Zicsr Standard Extension

10.02/10.01 200. Standard Entonsion									
csr	rs1	001	rd	1110011	CSRRW				
csr	rs1	010	rd	1110011	CSRRS				
csr	rs1	011	rd	1110011	CSRRC				
csr	uimm	101	rd	1110011	CSRRWI				
csr	uimm	110	rd	1110011	CSRRSI				
csr	uimm	111	$\operatorname{rd}$	1110011	CSRRCI				

### RV32M Standard Extension

0000001	rs2	rs1	000	$^{\mathrm{rd}}$	0110011	MUL					
0000001	rs2	rs1	001	$\operatorname{rd}$	0110011	MULH					
0000001	rs2	rs1	010	$\operatorname{rd}$	0110011	MULHSU					
0000001	rs2	rs1	011	$\operatorname{rd}$	0110011	MULHU					
0000001	rs2	rs1	100	rd	0110011	DIV					
0000001	rs2	rs1	101	$\operatorname{rd}$	0110011	DIVU					
0000001	rs2	rs1	110	rd	0110011	REM					
0000001	rs2	rs1	111	rd	0110011	REMU					

#### RV64M Standard Extension (in addition to RV32M)

10101111	Dunidana 112	1001151511 (11	i additio	11 00 100 021	· <del>·</del> ·	
0000001	rs2	rs1	000	$\operatorname{rd}$	0111011	MULW
0000001	rs2	rs1	100	$^{\mathrm{rd}}$	0111011	DIVW
0000001	rs2	rs1	101	$\operatorname{rd}$	0111011	DIVUW
0000001	rs2	rs1	110	$\operatorname{rd}$	0111011	REMW
0000001	rs2	rs1	111	$\operatorname{rd}$	0111011	REMUW