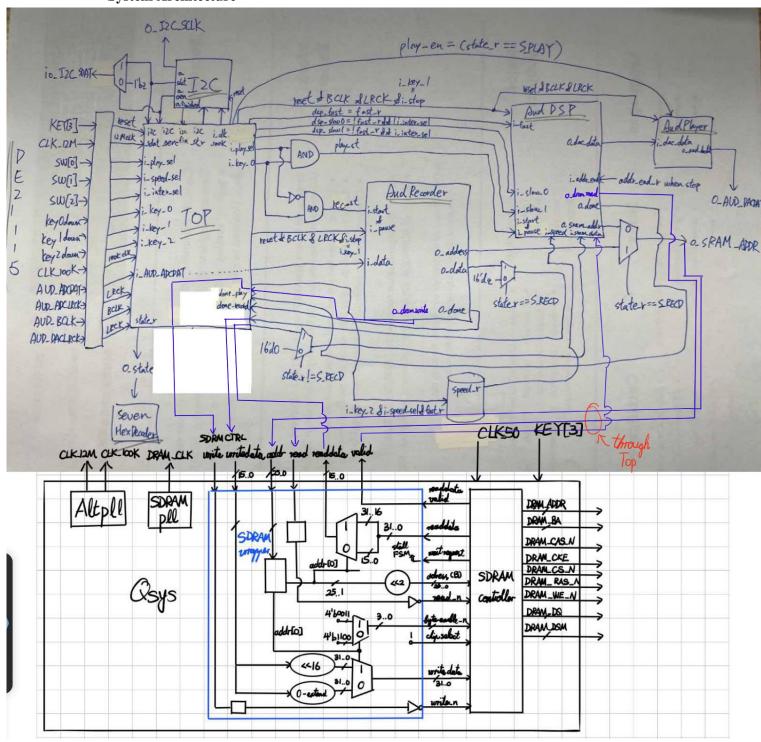
Team09_Lab3_Report

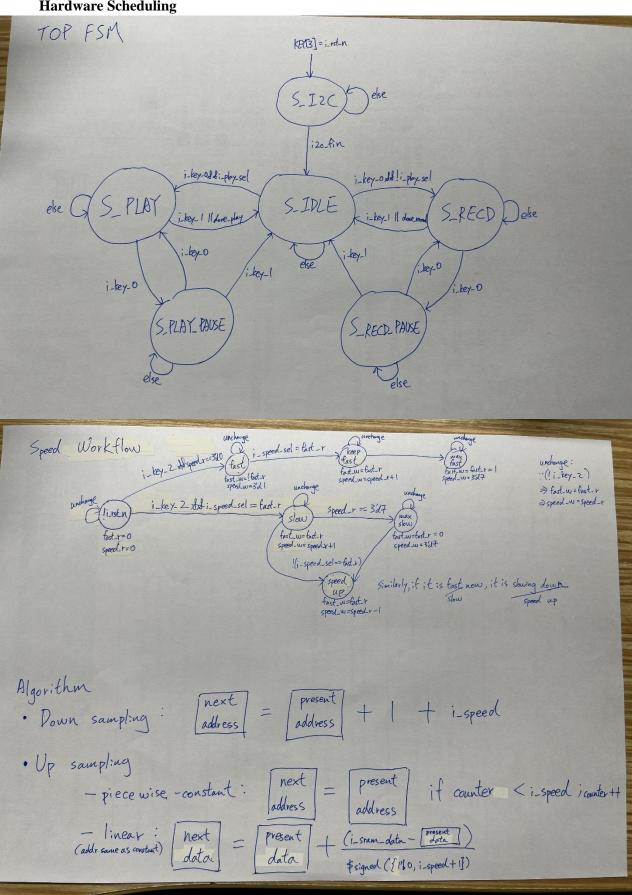
File Structure

- team09_lab3/team09_lab3_report: This file contains information about the source code in the directory and the instructions of lab3.
- team09_lab3/src : The files at this level are modules that implement the digital recorder.
- team09_lab3/src/DE2_115: The files in this folder are the DE2_115 related files.
- team09_lab3/src/Lab3_qsys/synthesis: The files in this folder are the Qsys generated HDL .qip and .v files.

System Architecture



Hardware Scheduling



Bonus

We have implemented storing and loading recorded audio with the onboard SDRAM chip. This is done by utilizing the Qsys components *System and SDRAM Clocks for DE-series Boards* and *SDRAM Controller*.

We have also written our own Avalon Memory Mapped Master component *sdram_wrapper* to better fit the pre-existing codes written for storing and loading with SRAM. In the end, we have successfully stored and played more than 32 seconds of audio in the SDRAM, with only a few signals and conditions added to the original codebase.

Fitter Summary

Fitter Summary	
Fitter Status	Successful - Tue Nov 07 22:16:58 2023
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,530 / 114,480 (1 %)
Total combinational functions	1,298 / 114,480 (1 %)
Dedicated logic registers	724 / 114,480 (< 1 %)
Total registers	843
Total pins	518 / 529 (98 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	2 / 4 (50 %)

Timing Analyzer

Timing Closure Recommendations

Summary [hide details]

This design contains failing setup paths with a worst-case slack of -73.658 ns. Run Report Timing Closure Recomme

Top Failing Paths [hide details]

	Slack	From	То	Recommendations
1	-73.658	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	Report recommendations for this path
2	-73.654	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	Report recommendations for this path
3	-73.652	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	Report recommendations for this path
4	-73.652	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	Report recommendations for this path
5	-73.648	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	Report recommendations for this path

Slo	Slow 1200mV 85C Model Setup Summary							
	Clock	Slack	End Point TNS					
1	AUD_BCLK	-73.658	-1808.155					
2	qsys0 altpll_0 sd1 pll7 clk[0]	-6.194	-155.253					
3	CLOCK_50	-2.595	-104.802					
4	qsys0 altpll_0 sd1 pll7 dk[1]	78.622	0.000					

Slo	Slow 1200mV 85C Model Minimum Pulse Width Summary							
	Clock	Slack	End Point TNS					
1	AUD_BCLK	-3.210	-215.235					
2	CLOCK_50	9.590	0.000					
3	qsys0 altpll_0 sd1 pll7 clk[0]	41.373	0.000					
4	qsys0 altpll_0 sd1 pll7 dk[1]	4999.706	0.000					

M TSOOIIIA	85C Model Setup: 'AUD_BCLK'						
Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Dela
-73.658	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.853
-73.513	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[13]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.708
-73.504	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.699
-73.341	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[15]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.392	76.642
-73.316	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[10]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.288	76.513
-73.264	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[7]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.459
-73.196	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[15]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.392	76.497
-73.187	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[15]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.392	76.488
-73.171	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[10]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.288	76.368
-73.162	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[10]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.288	76.359
-73.119	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[7]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.314
-73.110	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[7]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.305
-73.013	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[3]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	76.208
-72.979	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[14]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	76.311
-72.963	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[1]	gsys0 altpll 0 sd1 pll7 dk[0]	AUD BCLK	0.001	3.469	76.341
-72.872	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[11]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	76.204
-72.868	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del data r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD BCLK	0.001	3.286	76.063
-72.859	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.286	76.054
-72,848	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[12]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	76, 180
-72.834	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[14]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	76.166
-72.825	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del data r[14]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	76.157
-72.818	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[1]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.469	76,196
-72.809	Top:top0 speed r[0]	Top:top0 AudDSP:dsp0 del data r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD BCLK	0.001	3.286	76.004
-72.809	Top:top0 speed r[1]	Top:top0 AudDSP:dsp0 del data r[1]	qsys0 altpll 0 sd1 pll7 dk[0]	AUD BCLK	0.001	3,469	76.187
-72.753	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	76.085
-72,738	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del data r[9]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD BCLK	0.001	3,423	76.070
-72.727	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	76.059
-72.718	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del data r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD BCLK	0.001	3.423	76.050
-72.703	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	76.035
-72,694	Top:top0 speed r[1]	Top:top0 AudDSP:dsp0 del_data_r[12]	qsys0 altpl 0 sd1 pl 7 clk[0]	AUD BCLK	0.001	3.423	76.026
-72.664	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_[12]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.286	75.859
-72.655	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[2]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.286	75.850
-72.608	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[2]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	75.940
-72.599	Top:top0 speed_r[2] Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[8]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	75.931
-72.599		Top:top0 AudDSP:dsp0 del_data_r[8]		AUD_BCLK	0.001	3.423	75.931
-72.593	Top:top0 speed_r[2]		qsys0 altpll_0 sd1 pll7 clk[0]		0.001	3.423	75.925
-72.499	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001		75.831
-72.449	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK		3.423	
	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	75.781
-72.354 -72.345	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[5]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.423	75.686 75.677
-72.345	Top:top0[speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	75.636
	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK			
-72.295	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	75.627
-72.290	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	75.622
-72.186	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[0]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.392	75.487
-72.145	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	75.477
-72.136	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.423	75.468
-72.041	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[0]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.392	75.342
-72.032	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[0]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.392	75.333
-47.744	Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.898
-47.636	Top:top0 AudDSP:dsp0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.790
-47.620	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	49.108
-47.487	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	48.975
-47.426	Top:top0 AudDSP:dsp0 data_r[8]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	48.197
-47.423	Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del data r[15]	AUD BCLK	AUD BCLK	1.000	0.246	48.687

55 56	47.000										
56	-47.398	Top:top0 AudDSP:dsp0 data_r[0]			SP:dsp0 del_data_r					142	48.558
	-47.350	Top:top0 AudDSP:dsp0 data_r[0]			SP:dsp0 del_data_r					136	48.504
7	-47.315	Top:top0 AudDSP:dsp0 data_r[1]			SP:dsp0 del_data_r					246	48.579
8	-47.307	Top:top0 AudDSP:dsp0 data_r[5]			SP:dsp0 del_data_r					075	48.400
9	-47.305	Top:top0 AudDSP:dsp0 data_r[9]			SP:dsp0 del_data_r					.247	48.076
)	-47.303	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0) data_r[1]		SP:dsp0 del_data_r					606	48.897
	-47.290	Top:top0 AudDSP:dsp0 data_r[1]	Maria Pet		SP:dsp0 del_data_r					142	48.450
	-47.278	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					502	48.768
	-47.269	Top:top0 AudDSP:dsp0 data_r[2]			SP:dsp0 del_data_r					136	48.423
4	-47.259	Top:top0 AudDSP:dsp0 data_r[10]			SP:dsp0 del_data_r					.247	48.030
5	-47.242	Top:top0 AudDSP:dsp0 data_r[1]			SP:dsp0 del_data_r					136	48.396
6	-47.226	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					500	48.714
7	-47.220	Top:top0 AudDSP:dsp0 data_r[11]			SP:dsp0 del_data_r					.247	47.991
8	-47.186	Top:top0 AudDSP:dsp0 data_r[3]	NIdea - Fol		SP:dsp0 del_data_r					136	48.340
9	-47.170	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					606	48.764
70	-47.145	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					502	48.635
71	-47.138	Top:top0 AudDSP:dsp0 data_r[4]			SP:dsp0 del_data_r					136	48.292
72	-47.128	Top:top0 AudDSP:dsp0 data_r[12]			SP:dsp0 del_data_r	[]				.247	47.899
73 74	-47.120	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					500	48.608
	-47.099	Top:top0 AudDSP:dsp0 data_r[0]			SP:dsp0 del_data_r					136	48.253
75	-47.093	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0) data_r[0]		SP:dsp0 del_data_r					500	48.581
76	-47.090	Top:top0 AudDSP:dsp0 data_r[8]			SP:dsp0 del_data_r					.122	47.986
77	-47.088	Top:top0[AudDSP:dsp0]data_r[13]			SP:dsp0 del_data_r					.247	47.859
8	-47.061	Top:top0 AudDSP:dsp0 data_r[0]			SP:dsp0 del_data_r					277	48.356
9	-47.050	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					500	48.538
80	-47.048	Top:top0 AudDSP:dsp0 data_r[8]			SP:dsp0 del_data_r					.209	47.857
31	-47.045	Top:top0 AudDSP:dsp0 data_r[0]			SP:dsp0 del_data_r					323	48.386
32	-47.032	Top:top0 AudDSP:dsp0 data_r[8]			SP:dsp0 del_data_r					.247	47.803
33	-47.013 47.004	Top:top0 AudDSP:dsp0 data_r[14]			SP:dsp0 del_data_r					.247	47.784
34	-47.004	Top:top0 AudDSP:dsp0 data_r[6]			SP:dsp0 del_data_r					136	48.158
85	-46.999 -46.001	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 Top:top0 AudDSP:dsp0 data_r[1]			SP:dsp0 del_data_r					500	48.487
86 87	-46.991 -46.986				SP:dsp0 del_data_r SP:dsp0 del_data_r					136	48.145 48.189
87 88	-46.986 -46.975	Top:top0 AudDSP:dsp0 data_r[5]			SP:dsp0 del_data_r					185	48.189
38 39		Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					500	
	-46.969	Top:top0 AudDSP:dsp0 data_r[9] Top:top0 AudDSP:dsp0 data_r[5]			SP:dsp0 del_data_r					.122	47.865
90	-46.961 -46.954				SP:dsp0 del_data_r					081	48.060
91	-46.954 -46.953	Top:top0 AudDSP:dsp0 data_r[0]			SP:dsp0 del_data_r					277	48.249
92 93	-46.953 -46.948	Top:top0 AudDSP:dsp0 data_r[1] Top:top0 AudDSP:dsp0 data_r[2]			SP:dsp0 del_data_r SP:dsp0 del_data_r					277 246	48.248 48.212
93	-46.941										48.566
94 95	-46.941 -46.937	Lab3_gsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r					637	48.566
95 96	-46.937 -46.930	Top:top0[AudDSP:dsp0]data_r[1]			SP:dsp0 del_data_r SP:dsp0 del_data_r					323	
96 97	-46.930 -46.927	Top:top0 AudDSP:dsp0 data_r[0] Top:top0 AudDSP:dsp0 data_r[9]			SP:dsp0 del_data_r SP:dsp0 del_data_r					.209	48.225 47.736
98 99	-46.925 -46.923	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0			SP:dsp0 del_data_r SP:dsp0 del_data_r					683 .122	48.596 47.819
100	-46.923	Top:top0 AudDSP:dsp0 data_r[10] Top:top0 AudDSP:dsp0 data_r[2]			SP:dsp0 del_data_r					142	48.083
				Top:topu AudD	SP:dsp0 del_data_r	[10] AOD_BCLK	AUD_B	CLK 1.	000 0.	142	40.003
SIOW	1200mv	85C Model Setup: 'qsys0 altpll_0 sd1 pll7	[CIK[U]								
	Slack	From Node	To	o Node	Laund	th Clock	Latch Clock	Re	lationship Cl	lock Skew	Data Dela
	-6.194	Top:top0 AudDSP:dsp0 done_r	Top:top0 st	ate_r[0]	AUD_BCLK		qsys0 altpll_0 sd1 pll7 dk	[0] 0.001	-3.6	83	2.450
1											2.240
1 2	-6.026	Top:top0 AudRecorder:recorder0 done_r	Top:top0 st	ate_r[0]	AUD_BCLK		qsys0 altpll_0 sd1 pll7 clk	[0] 0.001	-3.6	46	2.319
2	-6.026 -5.997		Top:top0 st								2.319
	-5.997	Top:top0 AudRecorder:recorder0 done_r	Top:top0 st	ate_r[1]	AUD_BCLK		qsys0 altpll_0 sd1 pll7 dk	[0] 0.001	-3.6	41	2.295
2 3 4	-5.997 -5.904	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r	Top:top0 st	ate_r[1] ate_r[2]	AUD_BCLK AUD_BCLK		qsys0 altpll_0 sd1 pll7 dk qsys0 altpll_0 sd1 pll7 dk	[0] 0.001 [0] 0.001	-3.6 -3.6	41 78	2.295 2.165
2 3 4 5	-5.997 -5.904 -5.529	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20]	Top:top0 st Top:top0 st Top:top0 ac	cate_r[1] cate_r[2] ddr_end_r[20]	AUD_BCLK AUD_BCLK AUD_BCLK		qsys0 altpll_0 sd1 pll7 clk qsys0 altpll_0 sd1 pll7 clk qsys0 altpll_0 sd1 pll7 clk	[0] 0.001 [0] 0.001 [0] 0.001	-3.6· -3.6· -3.2·	41 78 41	2.295 2.165 2.227
2 3 4 5	-5.997 -5.904 -5.529 -5.515	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4]	Top:top0 st Top:top0 st Top:top0 ac Top:top0 ac	cate_r[1] cate_r[2] ddr_end_r[20] ddr_end_r[4]	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK		qsys0 altpll_0 sd1 pll7 dk qsys0 altpll_0 sd1 pll7 dk qsys0 altpll_0 sd1 pll7 dk qsys0 altpll_0 sd1 pll7 dk	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	-3.6 -3.6 -3.2 -3.2	41 78 41 71	2.295 2.165 2.227 2.183
2 3 4 5 6 7	-5.997 -5.904 -5.529 -5.515 -5.432	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11]	Top:top0 st Top:top0 st Top:top0 ac Top:top0 ac Top:top0 ac	ate_r[1] :ate_r[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[11]	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK		qsys0 altpll_0 sd1 pll7 dk qsys0 altpll_0 sd1 pll7 dk	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	-3.6 -3.6 -3.2 -3.2	41 78 41 71 71	2.295 2.165 2.227 2.183 2.100
2 3 4 5 6 7 8	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 ac Top:top0 ac Top:top0 ac Top:top0 ac	tate_r[1] tate_r[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[11] ddr_end_r[0]	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK		qsys0 altpll_0 sd1 pll7 dk qsys0 altpll_0 sd1 pll7 dk	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2	41 78 41 71 71 51	2.295 2.165 2.227 2.183 2.100 2.096
2 3 4 5 6 7 8	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 ac Top:top0 ac Top:top0 ac Top:top0 ac Top:top0 ac	tate_r[1] tate_r[2] ddr_end_r[20] ddr_end_r[11] ddr_end_r[11] ddr_end_r[0] ddr_end_r[1]	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK		qsys0 altpll_0 sd1 pll7 clk qsys0 altpll_0 sd1 pll7 clk	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	3.6 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 71 71 51	2.295 2.165 2.227 2.183 2.100 2.096 2.096
2 3 4 5 6 7 8 9	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 ac	tate_r[1] tate_r[2] ddr_end_r[20] ddr_end_r[11] ddr_end_r[11] ddr_end_r[0] ddr_end_r[1] ddr_end_r[1]	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK		qsys0 altpli_0 sd1 pli7 dk qsys0 altpli_0 sd1 pli7 dk	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	-3.6 -3.6 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2	41 78 41 71 71 51 51	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096
2 3 4 5 6 7 8 9 10	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 ador_r[11] Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r	Top:top0 st Top:top0 st Top:top0 ac	tate_r[1] tate_r[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[11] ddr_end_r[0] ddr_end_r[1] ddr_end_r[2] ddr_end_r[3]	AUD_BCLK		qsys0 altpli_0 sd 1 pli 7 clk qsys0 altpli_0 sd 1 pli 7 clk	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	-3.6 -3.6 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2	41 78 41 71 71 71 71 51 51 51 51 51	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096
2 3 4 5 6 7 8 9 10 11	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 ac	ate_[1] ate_[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[11] ddr_end_r[0] ddr_end_r[1] ddr_end_r[2] ddr_end_r[3] ddr_end_r[4]	AUD_BCLK		qsys0 altpli_0 sd 1 pl7 ck; qsys0 altpli_0 sd 1 pl7 ck;	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	-3.6 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2	41 78 41 71 71 71 71 71 71 71 71 71 71 71 71 71	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096
2 3 3 4 4 5 5 7 7 3 8 9 9 110 111 112 113	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 ac	ate_[1] ate_[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[1] ddr_end_r[0] ddr_end_r[0] ddr_end_r[2] ddr_end_r[3] ddr_end_r[4] ddr_end_r[5]	AUD_BCLK		qsys0 atpl _0 sd 1 pi17 ck, qsys0 atpl _0 sd 1 pi17	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	-3.6 -3.6 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2	41 78 41 71 71 51 51 51 51 51	2,295 2,165 2,227 2,183 2,100 2,096 2,096 2,096 2,096 2,096 2,096 2,096
2 3 3 4 5 5 5 7 7 8 8 9 9 10 11 11 12 13 14	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 ador_r[11] Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r	Top:top0 st Top:top0 st Top:top0 at	ate_[1] ate_[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[11] ddr_end_r[0] ddr_end_r[7] ddr_end_r[2] ddr_end_r[3] ddr_end_r[4] ddr_end_r[4] ddr_end_r[6]	AUD_BCLK		qsys0 latpl. 0 sd 1 pl/17cl. qsys0 atpl. 0 sd 1 pl/17cl. qsys0 sd 1	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 71 71 51 51 51 51 51 51	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096
2 3 4 5 5 7 7 3 8 9 110 111 112 113	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 at	ate_[1] ate_[2] ddr_end_r[20] ddr_end_r[4] ddr_end_r[1] ddr_end_r[0] ddr_end_r[0] ddr_end_r[2] ddr_end_r[3] ddr_end_r[4] ddr_end_r[5]	AUD_BCLK		qsys0 atpl _0 sd 1 pi17 ck, qsys0 atpl _0 sd 1 pi17	[0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 71 71 51 51 51 51 51 51	2,295 2,165 2,227 2,183 2,100 2,096 2,096 2,096 2,096 2,096 2,096 2,096
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2 3 4 5 6 7 8	-5,997 -5,904 -5,529 -5,515 -5,432 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 at	ate_[1] ate_[2] ddr_end_[20] ddr_end_[4] ddr_end_[11] ddr_end_[0] ddr_end_[0] ddr_end_[3] ddr_end_[4] ddr_end_[4] ddr_end_[4] ddr_end_[5] ddr_end_[5] ddr_end_[6]	AUD_BCLK		qsys0 atpl 0 sd 1 pl 1 cld qsys0 atpl 0 sd 1 pl 1 rld qsys0 sd 1 pl 1 qsys0 sd 1 pl 1 qsys0 sd 1 pl 1 qsys0 qs 1 pl 1 qsys0 qs 1 qs	[0] 0.001 [0] 0.001	-3.6 -3.6 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2 -3.2	41 78 41 71 71 51 51 51 51 51 51 51 51 51	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096
2 3 4 5 6 7 8 9 10 11 12 13 14 15	-5,997 -5,904 -5,529 -5,515 -5,432 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408 -5,408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dsp0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st Top:top0 st Top:top0 ac	ate_[1] ate_[2] ddr_end_[20] ddr_end_[4] ddr_end_[11] ddr_end_[0] ddr_end_[1] ddr_end_[2] ddr_end_[3] ddr_end_[4] ddr_end_[5] ddr_end_[5] ddr_end_[6]	AUD_BCLK		qsys0 atpl. 0 sd 1 pl17 ck, qsys0 atpl. 0 sd 1 pl17	[0] 0.001 [0] 0.	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 71 71 71 51 51 51 51 51 51 51 51 51 51 51	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096
2 3 4 5 5 6 7 8 9 9 10 11 12 13 14 15 16	-5.997 -5.904 -5.529 -5.515 -5.432 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 ador_r[4] Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 adone_r	Top:top0 st	ate_[1] ate_[2] dtc_end_[20] ddr_end_[4] ddr_end_[11] ddr_end_[0] ddr_end_[1] ddr_end_[2] ddr_end_[3] ddr_end_[4] ddr_end_[5] ddr_end_[6] ddr_end_[7] ddr_end_[6] ddr_end_[7]	AUD_BCLK		qsys0 latpl. 0 jet1 jell7-ide,	[0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 178 141 141 141 141 141 141 141 141 141 14	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096
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2 3 4 5 6 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	-5.997 -5.904 -5.529 -5.515 -5.402 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 adone_r	Top:top0 st	ate_[1] ate_[2] ate_[6] dtd_end_[4] dtd_end_[4] dtd_end_[14] dtd_end_[14] dtd_end_[15] dtd_end_[6] dtd_end_[6] dtd_end_[6] dtd_end_[6] dtd_end_[6] dtd_end_[6] dtd_end_[6] dtd_end_[7] dtd_end_[7] dtd_end_[7] dtd_end_[7] dtd_end_[16] dtd_end_[16] dtd_end_[16] dtd_end_[16] dtd_end_[16] dtd_end_[16] dtd_end_[16] dtd_end_[16]	AUD_BCLK		qsys0 latpl_0 sd1 pl17/ck qsys0 atpl_0 sd1 pl17/ck qsys0 sd1 pl1	[0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 41 77 78 41 41 77 71 71 71 71 71 71 71 71 71 71 71 71	2.295 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096
2 3 3 4 5 6 7 8 8 9 10 11 11 12 13 14 15 16 17 18 19 20 21	-5.997 -5.904 -5.529 -5.512 -5.408	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 done_r	Top:top0 st	ate_[1] ate_[2] ate_[2] dtr_end_[20] dtr_end_[4] dtr_end_[14] dtr_end_[15] dtr_end_[5] dtr_end_[6] dtr_end_[6] dtr_end_[7]	AUD_BCLK		qsys0 atps _0 sd 1 pi17 ck, qsys0 sd 1 pi17 ck,	[0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 41 77 78 78 79 79 79 79 79 79 79 79 79 79 79 79 79	2.295 2.165 2.165 2.127 2.183 2.100 2.096
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2 3 3 4 5 6 6 7 8 8 9 10 11 11 12 13 14 15 16 17 18 19 20 21 22 23 24	-5.997 -5.904 -5.5904 -5.591 -5.408 -	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudDSP:dop0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 dode_r[1] Top:top0 AudRecorder:recorder0 dode_r	Top:top0 st	ate [1] ate [2] ate [72] dth end [72] dth end [7]	AUD_BCLK		qsys0 atpl. 0 sd 1 pi17 ck, qsys0 ck, qsys0 ck, qsys0 ck, qsys0 ck, qsys0 ck, qsys0 ck	[0] 0.001 [0] 0.001	3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 78 441 441 477 77 77 77 77 77 77 77 77 77 77 77 77	2.295 2.165 2.165 2.165 2.127 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 1.973 1.902 1.1819
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2 3 4 4 5 5 6 6 6 7 7 8 8 9 9 10 10 12 12 13 13 14 14 15 15 16 6 17 18 18 19 19 10 10 11 12 12 13 13 14 14 15 16 16 17 18 18 19 19 10 10 10 10 10 10 10 10 10 10 10 10 10	5.997 -5.994 -5.515 -5.492 -5.515 -5.492 -5.5408 -5.509 -5.090 -5	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_f[20] Top:top0 AudRecorder:recorder0 addr_f[20] Top:top0 AudRecorder:recorder0 addr_f[11] Top:top0 AudRecorder:recorder0 addr_f[11] Top:top0 AudRecorder:recorder0 addr_f[11] Top:top0 AudRecorder:recorder0 addr_f[11] Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 addr_f[1] Top:top0 AudRecorder:recorder0 addr_f[2] Top:top0 AudRecorder:recorder0 addr_f[2] To	Top:topol st Top:topol st Top:topol st Top:topol sc Top:topol sc Topol	ate [1] ate [2] ate [2	AUD_BCLK		qsys0 altpl. 0 sd 1 pl/17ck qsys0 altpl. 0 sd 1 pl/1		3.6 3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 78 41 41 77 77 71 71 551 551 551 551 551 551 55	2.295 2.165 2.165 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 1.780 1.781 1.782 1.782 1.783 1.785 1.785 1.785 1.785 1.785 1.786 1.781 1.781 1.781 1.782 1.781 1.781 1.781 1.782 1.783 1.785 1.785 1.785 1.785 1.786 1.787 1.787 1.788 1.791
0 1 1 2 2 3 3 4 4 5 5 6 6 7 7 8 8 9 9 0 1 1 2 2 3 3 4 4 5 5 6 6 7 7 8 9 9 0 1 1 2 2 3 3 4 5 5 6 6 7 8 8 9 9 0 1 1 2 2 3 3 4 5	-5.997 -5.994 -5.529 -5.515 -5.408 -5.509 -5.090 -5.000 -5	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_f[20] Top:top0 AudRecorder:recorder0 addr_f[20] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 adone_r Top:top0 AudRecorder:recorder0 addr_f[3] Top:top0 AudRecorder:recorder0 addr_f[3] Top:top0 AudRecorder:recorder0 addr_f[3] Top:top0 AudRecorder:recorder0 addr_f[3] Top:top0 AudRecorder:recorder0 addr_f[3	Top:topol ist Topol ist Topol ist Topol ist Topol ist Topol ist Topol is	ate [1] ate [1] ate [2] did end [20] did end [1] did end [2] did end [2] did end [3] did end [6] did end [7] did end [1]	AUD_BCLK		qsys0 altql. 0 jet1 jel7/ck qs		3.6 3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 78 78 78 78 78 78 78 78 78 78 78 78	2.295 2.165 2.165 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 1.780 1.781 1.780 1.780 1.780 1.780 1.780 1.780 1.780 1.780 1.780 1.781 1.780
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2 3 4 5 5 6 6 7 7 8 8 9 9 00 11 12 23 3 4 4 15 5 6 6 17 7 8 8 19 9 10 11 12 12 13 14 14 15 16 16 17 17 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 16 17 18 18 19 10 10 11 12 13 13 14 15 16 17 18 18 19 10 10 11 12 13 13 14 15 16 17 18 18 19 10 10 11 12 13 13 14 15 16 17 18 18 19 10 10 10 11 12 13 13 14 15 16 17 18 18 19 10 10 11 12 13 13 14 15 16 17 18 18 19 10 10 10 10 10 10 10 10 10 10 10 10 10	-5.997 -5.994 -5.515 -5.408 -6	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 ador_r Top:top0 AudRecorder:recorder0 addr_r Top:top0	Topitopolist	ate [1] ate [2] did end [20] did end [3] did end [4] did end [6] did end [7] did end [8] did end [9] did end [10]	AUD_BCIK		egyo altipl. 0 et 10 17/ck		3.6 3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 78 41 41 77 77 71 71 551 551 551 551 551 551 55	2.295 2.165 2.165 2.165 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 1.730
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2 3 4 5 6 7 8 9 9 10 11 12 23 3 44 15 15 16 17 7 18 18 19 19 10 11 12 13 14 14 15 15 16 17 18 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 16 17 18 19 10 11 12 13 14 15 15 15 15 15 15 15 15 15 15 15 15 15	-5.997 -5.994 -5.515 -5.408 -6	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 ador_r Top:top0 AudRecorder:recorder0 addr_r Top:top0	Top:topol ist To	ate [1] ate [2] did end [20] did end [3] did end [4] did end [6] did end [7] did end [8] did end [9] did end [10]	AUD_BCIK		egyo altipl. 0 et 10 17/ck		3.6 3.6 3.6 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2 3.2	41 78 78 78 41 41 77 71 71 71 71 71 71 71 71 71 71 71 71	2.295 2.165 2.165 2.165 2.227 2.183 2.100 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 2.096 1.780

55	-4.804	Top:top0 AudRecorder:recorder0 addr_r[6]	Top:top0 addr_end_r[6]	AUD_BCLK			0.001	-3.271	1.472
56	-4.770	Top:top0 AudRecorder:recorder0 addr_r[23]		AUD_BCLK	qsys0 altpll_0 sd1 qsys0 altpll_0 sd1		0.001	-3.241	1.468
57	77.875	Debounce:deb1 neg_r	Top:top0 state_r[1]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	-0.519	4.937
58	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
9	78,872	Debounce:deb1 neg_r	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
0	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
51	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
		Debounce:deb1 neg_r							
2	78.872		Top:top0 addr_end_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
3	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
4	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[6]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 dk[0]	83.333	-0.129	4.330
5	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[7]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	-0.129	4.330
6	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	-0.129	4.330
7	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[9]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	-0.129	4.330
8	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[10]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
9	78.872	Debounce:deb1 neg r	Top:top0 addr end r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
0	78.872	Debounce:deb1 neg_r	Top:top0 addr_end_r[12]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	-0.129	4.330
1	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 clk[0]			83.333		4.669
					qsys0 altpll_0 sd1			0.315	
2	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	0.315	4.669
3	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	0.315	4.669
4	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	0.315	4.669
5	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[4]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 dk[0]	83.333	0.315	4.669
5	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[5]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	0.315	4.669
,	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[6]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 dk[0]	83.333	0.315	4.669
3	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[7]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	0.315	4.669
,	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	0.315	4.669
	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[9]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	0.315	4.669
L	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[10]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	0.315	4.669
2	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	0.315	4.669
3	78.977	Top:top0 state_r[0]	Top:top0 addr_end_r[12]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	0.315	4.669
ŀ	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[13]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1	p 7 dk[0]	83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[14]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[15]	qsys0 altpll 0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg r	Top:top0 addr_end_r[16]	qsys0 altpll 0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[16]	qsys0 altpll 0 sd1 pll7 clk[0]					
					qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[18]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[19]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[20]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[21]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1	p 7 dk[0]	83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[22]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1	p 7 c k[0]	83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[23]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[24]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	-0.127	4.014
	79.190	Debounce:deb1 neg_r	Top:top0 addr_end_r[24]		qsys0 altpll_0 sd1				4.014
				qsys0 altpll_0 sd1 pll7 dk[0]			83.333	-0.127	
	79.229	Top:top0 state_r[2]	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1		83.333	0.309	4.411
	79.229	Top:top0 state_r[2]	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1		83.333	0.309	4.411
	79.229	Top:top0 state_r[2]	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1	pl17 clk[0]	83.333	0.309	4.411
0	79.229	Top:top0 state_r[2]	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1	p 7 dk[0]	83.333	0.309	4.411
	Slack	From Node		Node	Launch Clock	Latch Clock	Relationship	Clock Skew	
	-2.595 -2.595	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22]	AUD_BCLK C	OLOCK_50 OLOCK_50	1.000 1.000	-0.966 -0.966	2.617 2.617
	-2.595	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22]	AUD_BCLK C	CLOCK_50	1.000	-0.966	
	-2.595 -2.595	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22] r:sdram_wrapper_0 addr_r[20]	AUD_BCLK C AUD_BCLK C AUD_BCLK C	OLOCK_50 OLOCK_50	1.000 1.000	-0.966 -0.966	2.617 2.617
	-2.595 -2.595 -2.595	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22] r:sdram_wrapper_0 addr_r[20] r:sdram_wrapper_0 addr_r[1]	AUD_BCLK C AUD_BCLK C AUD_BCLK C AUD_BCLK C	CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000	-0.966 -0.966	2.617 2.617 2.617
	-2.595 -2.595 -2.595 -2.500	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[1]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22] r:sdram_wrapper_0 addr_r[20] r:sdram_wrapper_0 addr_r[1] r:sdram_wrapper_0 data_r[15]	AUD_BCLK C AUD_BCLK C AUD_BCLK C AUD_BCLK C AUD_BCLK C	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501	2.617 2.617 2.617 2.987
	-2.595 -2.595 -2.595 -2.500 -2.495	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22] r:sdram_wrapper_0 addr_r[20] r:sdram_wrapper_0 addr_r[1] r:sdram_wrapper_0 data_r[15] r:sdram_wrapper_0 data_r[14]	ALID_BCLK (ALID_B	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_f[25] r:sdram_wrapper_0 addr_f[22] r:sdram_wrapper_0 addr_f[20] r:sdram_wrapper_0 dadr_f[1] r:sdram_wrapper_0 data_f[15] r:sdram_wrapper_0 data_f[14]	AUD_BCLK (CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[20] r:sdram_wrapper_0 addr_r[13] r:sdram_wrapper_0 addr_r[15] r:sdram_wrapper_0 data_r[14] r:sdram_wrapper_0 data_r[14] r:sdram_wrapper_0 data_r[14]	AUD_BCLK (CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	r:sdram_wrapper_0 addr_r[25] r:sdram_wrapper_0 addr_r[22] r:sdram_wrapper_0 addr_r[20] r:sdram_wrapper_0 data_r[15] r:sdram_wrapper_0 data_r[14] r:sdram_wrapper_0 data_r[14] r:sdram_wrapper_0 data_r[12] r:sdram_wrapper_0 data_r[11]	AUD_BCLK C	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[20] risdram_wrapper_0 addr_r[10] risdram_wrapper_0 dadr_r[1] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[14] risdram_wrapper_0 data_r[12] risdram_wrapper_0 data_r[11] risdram_wrapper_0 data_r[11]	AUD_BCLK C	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0]AudRecorder:recorder0]write_r	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0 SDRAMWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[0] risdram_wrapper_0 addr_r[0] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[16] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[17]	AUD_BCLK C	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0[write_r Top:top0]AudRecorder:recorder0[write_r	Lab3_gsys:qsys0 SDRAMWirappe Lab3_gsys:qsys0 SDRAWWirappe Lab3_gsys:qsys0 SDRAWWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 data_r[14] risdram_wrapper_0 data_r[14] risdram_wrapper_0 data_r[14] risdram_wrapper_0 data_r[16] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[9]	AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_gysrqsys0 SDRAMWirappe Lab3_gysrqsys0 SDRAWwirappe Lab3_gysrqsys0 SDRAWwirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 daddr_r[1] risdram_wrapper_0 dada_r[4] risdram_wrapper_0 data_r[4] risdram_wrapper_0 data_r[4] risdram_wrapper_0 data_r[1] risdram_wrapper_0 data_r[1] risdram_wrapper_0 data_r[1] risdram_wrapper_0 data_r[6] risdram_wrapper_0 data_r[6] risdram_wrapper_0 data_r[6]	AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0[write_r Top:top0]AudRecorder:recorder0[write_r	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0 SDRAMWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 daddr_r[1] risdram_wrapper_0 dada_r[4] risdram_wrapper_0 data_r[4] risdram_wrapper_0 data_r[4] risdram_wrapper_0 data_r[1] risdram_wrapper_0 data_r[1] risdram_wrapper_0 data_r[1] risdram_wrapper_0 data_r[6] risdram_wrapper_0 data_r[6] risdram_wrapper_0 data_r[6]	AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	0.966 0.966 0.966 0.966 0.901 0.937 0.937 0.937 0.937 0.937 0.937 0.937 0.937 0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_gysrqsys0 SDRAMWirappe Lab3_gysrqsys0 SDRAWwirappe Lab3_gysrqsys0 SDRAWwirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[72] risdram_wrapper_0 addr_r[7] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[16] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[18] risdram_wrapper_0 datdr_r[8] risdram_wrapper_0 datdr_r[8]	AUD BOLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r	Lab3_geys:qeys0 SDRAMWirappe Lab3_geys:qeys0 SDRAMWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[0] risdram_wrapper_0 addr_r[0] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[16] risdram_wrapper_0 data_r[16] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[8] risdram_wrapper_0 datd_r[7] risdram_wrapper_0 datd_r[7] risdram_wrapper_0 datd_r[7] risdram_wrapper_0 datd_r[7]	AUD BOLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	0.966 -0.966 -0.966 -0.501 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.957 -0.957 -0.957	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0 SDRAWWirappe Lab3_qsys:qsys0 SDRAWWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 data_r[14] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 addr_r[19] risdram_wrapper_0 addr_r[19] risdram_wrapper_0 addr_r[19] risdram_wrapper_0 addr_r[24] risdram_wrapper_0 addr_r[24] risdram_wrapper_0 addr_r[25]	AUD BOLK AUD	0.00K_50 0.00K_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.966 -0.966 -0.966 -0.501 -0.937 -0	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
	-2.595 -2.595 -2.595 -2.500 -2.495 -2	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_gysrqsys0 SDRAMWirappe Lab3_gysrqsys0 SDRAMWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[72] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 data_r[15] risdram_wrapper_0 data_r[16] risdram_wrapper_0 data_r[17] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[18] risdram_wrapper_0 addr_r[9] risdram_wrapper_0 addr_r[9] risdram_wrapper_0 addr_r[24] risdram_wrapper_0 addr_r[24] risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[26]	AUD BOLK	0.00X_50 0.00X_	1.000 1.000	-0.966 -0.966 -0.966 -0.997 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.957 -0.957 -0.957 -0.957 -0.966 -0.966	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546
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	-2.595 -2.595 -2.595 -2.500 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.495 -2.390 -2.390 -2.390 -2.390	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0 SDRAWWirappe Lab3_qsys:qsys0 SDRAWWirappe	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[22] risdram_wrapper_0 addr_r[72] risdram_wrapper_0 addr_r[7] risdram_wrapper_0 addr_r[1] risdram_wrapper_0 data_r[14] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 addr_r[19] risdram_wrapper_0 addr_r[27] risdram_wrapper_0 addr_r[27] risdram_wrapper_0 addr_r[28] risdram_wrapper_0 addr_r[28] risdram_wrapper_0 addr_r[28] risdram_wrapper_0 addr_r[28]	AUD BOLK AUD	0.00K_50 0.00K_	1.000 1.000	-0.966 -0.966 -0.966 -0.906 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.957 -0.966 -0.966 -0.966 -0.557	2.617 2.617 2.617 2.987 2.546 2.547
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	2.595 2.595 2.595 2.595 2.595 2.495 2.390 2.300	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[2] Top:top0]AudRecorder:recorder0]addr_r[2] Top:top0]AudRecorder:recorder0]addr_r[2] Top:top0]AudDSP:ddp0]read_r Top:top0]AudDSP:ddp0]read_r Top:top0]AudDSP:ddp0]read_r Top:top0]AudDSP:ddp0]read_r Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]w	Lab3_qsys:qsys0 SDRAMWirappe	risidram_wrapper_0 addr_r[25] risidram_wrapper_0 addr_r[22] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[37] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[19] risidram_wrapper_0 data_r[19] risidram_wrapper_0 data_r[19] risidram_wrapper_0 data_r[19] risidram_wrapper_0 addr_r[19]	ALD BOLK ALD	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.940 -0.492 -0.492 -0.492 -0.492 -0.492 -0.460 -0.966 -0.557 -0.460 -0.460 -0.460 -0.460 -0.946	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.548 2.983 2.947 2.837 2.812 2.814 2.881 2.814 2.851 2.816
	2.595 2.595 2.595 2.590 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.390 2.300	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWirappe	risidram "wrapper_Oladdr_r[25] risidram "wrapper_Oladdr_r[27] risidram wapper_Oladdr_r[27] risidram wapper_Oladdr_r[27] risidram wapper_Oladdr_r[18] risidram wapper_Oladata_r[18] risidram wapper_Oladata_r[18] risidram wapper_Oladata_r[18] risidram wapper_Oladata_r[19] risidram wapper_Oladata_r[10] risidram wapper_Oladata_r[10] risidram wapper_Oladdr_r[10] risidram wapper_Oladdr_r[19] risidram wapper_Oladdr_r[27] risidram wapper_Oladdr_r[28] risidram wapper_Oladdr_r[3] risidram wapper_Oladdr_r[48] risidram wapper_Oladdr_r[48] risidram wapper_Oladdr_r[48] risidram wapper_Oladdr_r[48] risidram wapper_Oladdr_r[48] risidram wapper_Oladdr_r[58] risidram wapper_Oladata_r[78]	ALD BOLK ALD	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.906 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.940 -0.492 -0.492 -0.492 -0.492 -0.492 -0.492 -0.557 -0.460 -0.966 -0.966 -0.966 -0.946	2.617 2.617 2.617 2.987 2.546 2.547 2.817 2.817 2.817 2.817 2.817 2.817 2.818 2.348
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	2.595 2.595 2.595 2.595 2.595 2.495 2.390 2.290 2.200	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]write_r Top:top0]Au	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risidram_wrapper_0 addr_r[25] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[19] risidram_wrapper_0 data_r[19] risidram_wrapper_0 addr_r[19] risidram_wrapper_0 addr_r[19] risidram_wrapper_0 addr_r[28] risidram_wrapper_0 addr_r[18]	AUD BOLK AUD	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.940 -0.966 -0.966 -0.966 -0.557 -0.460 -0.946 -0.939 -0.939 -0.939 -0.939 -0.939	2.617 2.617 2.617 2.987 2.546 2.541 2.817 2.817 2.817 2.817 2.817 2.818 2.818 2.818 2.818 2.818 2.818 2.818 2.348
	2.595 2.595 2.595 2.595 2.590 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.390 2.390 2.390 2.390 2.390 2.390 2.306 2.206 2.206 2.206 2.206 2.206 2.206	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[3] Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r[1] Top:top0]AudRecorder:recorder0]addr_r[1] Top:top0]AudRecorder:recorder0]addr_r[1] Top:top0]AudRecorder:recorder0]addr_r[1] Top:top0]AudRecorder:recorder0]addr_r[1] Top:top0]AudRecorder:recorder0]write_r Top:top	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risdram_wrapper_0 addr_r[25] risdram_wrapper_0 addr_r[27] risdram_wrapper_0 addr_r[27] risdram_wrapper_0 addr_r[17] risdram_wrapper_0 addr_r[18] risdram_wrapper_0 addr_r[18] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[18] risdram_wrapper_0 data_r[19] risdram_wrapper_0 data_r[19] risdram_wrapper_0 addr_r[19] risdram_wrapper_0 addr_r[18]	AUD BOLK AUD	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.901 -0.937 -0.940 -0.492 -0.492 -0.557 -0.460 -0.966 -0.966 -0.966 -0.949 -0.946 -0.949 -0.949 -0.939 -0.939 -0.939 -0.939 -0.939 -0.939 -0.939 -0.939 -0.939	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.541 2.817 2.817 2.812 2.412 2.412 2.412 2.412 2.814 2.881 2.867 2.824 2.816
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	2.595 2.595 2.595 2.595 2.590 2.495 2.390 2.300 2.300 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.206 2.206 2.206 2.296 2.296 2.296 2.296 2.296 2.296	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[9] Top:top0]AudRecorder:recorder0]addr_r[10] Top:top0]AudRecorder:recorder0]addr_r[10] Top:top0]AudRecorder:recorder0]addr_r[10] Top:top0]AudRecorder:recorder0]addr_r[11] Top:top0]AudRecorder:recorder0]addr_r[11] Top:top0]AudRecorder:recorder0]addr_r[11] Top:top0]AudRecorder:recorder0]addr_r[11] Top:top0]AudRecorder:recorder0]addr_r[11] Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risidram "wrapper_Oladdr_[25] risidram wrapper_Oladdr_[124] risidram wrapper_Oladdr_[127] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[128] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[10] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[124] risidram wrapper_Oladdr_[124] risidram wrapper_Oladdr_[124] risidram wrapper_Oladdr_[126] risidram wrapper_Oladdr_[126] risidram wrapper_Oladdr_[127] risidram wrapper_Oladdr_[13] risidram wrapper_Oladdr_[14] risidram wrapper_Oladdr_[15] risidram wrapper_Oladdr_[16]	AUD BOLK AUD BO	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.906 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.940 -0.492 -0.557 -0.460 -0.557 -0.460 -0.557 -0.460 -0.501 -0.460 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.949 -0.939	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.947 2.837 2.412 2.412 2.412 2.412 2.814 2.888 2.857 2.824 2.816 2.807 2.348
	2.595 2.595 2.595 2.595 2.595 2.595 2.595 2.495 2.390 2.390 2.390 2.306 2.306 2.306 2.306 2.306 2.306 2.206 2.206 2.206 2.226 2.296 2.296 2.296 2.296 2.296 2.296 2.296 2.296	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risidram_wrapper_0 addr_r[25] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[28] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[18] risidram_wrapper_0 data_r[19] risidram_wrapper_0 data_r[19] risidram_wrapper_0 data_r[19] risidram_wrapper_0 addr_r[19] risidram_wrapper_0 addr_r[18]	ALD BOLK ALD	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.906 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.946 -0.966 -0.966 -0.557 -0.460 -0.460 -0.460 -0.460 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.990 -0.990 -0.993 -0.939	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.548 2.983 2.947 2.837 2.812 2.412 2.412 2.412 2.412 2.412 2.412 2.412 2.314 2.851 2.867 2.348
	2.595 2.595 2.595 2.595 2.590 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.495 2.390	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[9] Top:top0]AudRecorder:recorder0]addr_r[10] Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]addr_r Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risidram_wrapper_0 addr_r[25] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[28] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 addr_r[19] risidram_wrapper_0 addr_r[19] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 addr_r[19]	AUD BOLK AUD BO	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.940 -0.966 -0.966 -0.966 -0.966 -0.966 -0.946 -0.956 -0.555	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.548 2.947 2.837 2.412 2.412 2.412 2.412 2.412 2.412 2.814 2.881 2.867 2.824 2.815 2.816 2.816 2.848 2.348
	2.595 2.595 2.595 2.595 2.595 2.595 2.590 2.495 2.390 2.390 2.390 2.390 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.296	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[9] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[16] Top:top0]AudRecorder:recorder0]addr_r[16] Top:top0]AudRecorder:recorder0]addr_r[17] Top:top0]AudRecorder:recorder0]addr_r[18] Top:top0]AudRecorder:recorder0]addr_r[19] Top:top0]AudRecorder:recorder0]addr_r[19] Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]writ	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risidram_wrapper_0 addr_r[25] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[17] risidram_wrapper_0 addr_r[18] risidram_wrapper_0 data_r[18]	AUD BOLK AUD BO	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.9966 -0.991 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.9492 -0.557 -0.460 -0.966 -0.966 -0.966 -0.966 -0.966 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.946 -0.949 -0.939	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.983 2.947 2.837 2.412 2.412 2.412 2.412 2.412 2.412 2.412 2.412 2.412 2.412 2.413 2.851 2.851 2.851 2.851 2.867 2.348 2.345
	2.595 2.595 2.595 2.595 2.595 2.595 2.495 2.390 2.390 2.390 2.390 2.391 2.391 2.390 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.306 2.296	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]addr_r[13] Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0	risidram_wrapper_0 addr_r[25] risidram_wrapper_0 addr_r[27] risidram_wrapper_0 addr_r[28] risidram_wrapper_0 addr_r[18]	ALD BOLK ALD BO	200K_50	1.000 1.000	-0.966 -0.966 -0.966 -0.966 -0.906 -0.901 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.937 -0.940 -0.966 -0.966 -0.966 -0.966 -0.966 -0.946 -0.953 -0.939	2.617 2.617 2.617 2.987 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.546 2.548 2.947 2.837 2.812 2.412 2.412 2.412 2.412 2.814 2.888 2.345 2.345
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55	-2.289	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
56	-2.289	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
57	-2.279	Top:top0 AudRecorder:recorder0 addr_r[15]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.460	2.807
58	-2.274	Top:top0 AudDSP:dsp0 addr_r[4]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.565	2.697
59	-2.272	Top:top0 AudRecorder:recorder0 addr_r[8]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.768
60	-2.270	Top:top0 AudRecorder:recorder0 addr_r[2]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.501	2.757
61	-2.269	Top:top0 AudDSP:dsp0 addr_r[9]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.556	2.701
62	-2.265	Top:top0 AudRecorder:recorder0 addr_r[21]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.473	2.780
63	-2.255	Top:top0 AudDSP:dsp0 addr_r[8]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.556	2.687
64	-2.254	Top:top0 AudRecorder:recorder0 addr_r[23]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.778
65	-2.247	Top:top0 AudRecorder:recorder0 addr_r[22]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.491	2.744
66	-2.243	Top:top0 AudRecorder:recorder0 addr_r[17]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.767
67	-2.240	Top:top0 AudDSP:dsp0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.557	2.671
68	-2.235	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
69	-2.235	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
70	-2.235	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
71	-2.235	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
72	-2.235	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
73	-2.235	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
74	-2.222	Top:top0 AudRecorder:recorder0 addr_r[18]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.746
75	-2.220	Top:top0 AudDSP:dsp0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.486	2.722
76	-2.211	Top:top0 AudRecorder:recorder0 addr_r[24]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.735
77	-2.207	Top:top0 AudRecorder:recorder0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.488	2.707
78	-2.197	Top:top0 AudRecorder:recorder0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.721
79	-2.169	Top:top0 AudDSP:dsp0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.556	2.601
80	-2.151	Top:top0 AudRecorder:recorder0 addr_r[25]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.491	2.648
81	-2.145	Top:top0 AudDSP:dsp0 addr_r[6]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.483	2.650
82	-2.135	Top:top0 AudRecorder:recorder0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.631
83	-2.104	Top:top0 AudRecorder:recorder0 addr_r[20]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.491	2.601
84	-2.102	Top:top0 AudRecorder:recorder0 addr_r[4]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.501	2.589
85	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
86	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
87	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
88	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
89	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
90	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
91	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
92	-2.100	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
93	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
94	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
95	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
96	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
97	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
98	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
99	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
100	-2.091	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
Slow	1200m\	V 85C Model Minimum Pulse Width: 'AUD_	BCLK'					

	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.210	1.000	4.210	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[0]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[10]
4	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[11]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[12]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[13]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[14]
8	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[15]
9	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[16]
10	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[17]
11	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[18]
12	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[19]
13	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[1]
14	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[20]
15	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[21]
16	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[22]
17	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[23]
18	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[24]
19	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[25]
20	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[26]
21	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[2]
22	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[3]
23	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[4]
24	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[5]
25	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[6]
26	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[7]
27	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[8]
28	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[9]
29	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[0]
30	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[1]
31	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[2]
32	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 dadrck_p
33	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[0]
34	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[10]
35	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[11]
36	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[12]
37	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[13]
38	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[14]
39	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[15]
40	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[1]
41	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[2]
42	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[3]
43	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[4]
44	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[5]
45	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[6]
46	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[7]
47	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[8]
48	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[9]
49	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[0]
50	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[10]
51	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[11]
52	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[12]
53	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[13]
54	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[14]

55	-1.285	1.000	2.285	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[15]
56	-1.285	1.000	2,285	Min Period	AUD BCLK	Rise	Top:top0[AudDSP:dsp0[data_r[1]
57	-1.285	1.000	2.285	Min Period	AUD BCLK	Rise	Top:top0[AudDSP:dsp0[data_r[2]
58	-1.285	1.000	2.285	Min Period	AUD BCLK	Rise	Top:top0[AudDSP:dsp0[data r[3]
59	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[4]
60	-1.285	1.000	2.285	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[5]
61	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[6]
62	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[7]
63	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[8]
64	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[9]
65	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[0]
66	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[10]
67	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[11]
68	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[12]
69	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[13]
70	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[14]
71	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[15]
72	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[1]
73	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[2]
74	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[3]
75	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[4]
76	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[5]
77	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[6]
78	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[7]
79	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[8]
80	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[9]
81	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 done_r
82	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 read_r
83	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_CALC
84	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_IDLE
85	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_PAUSE
86	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_PLAY
87	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_
88	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_
89	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_
90	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_
91	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[0]
92	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[10]
93	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[11]
94	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[12]
95	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[13]
96	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[14]
97	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[15]
98	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[1]
99	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[2]
100	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[3]

Slov	Slow 1200mV 0C Model Setup Summary						
	Clock	Slack	End Point TNS				
1	AUD_BCLK	-66.398	-1640.870				
2	qsys0 altpll_0 sd1 pll7 clk[0]	-5.683	-141.183				
3	CLOCK_50	-2.383	-96.510				
4	qsys0 altpll_0 sd1 pll7 dk[1]	79.074	0.000				

Slov	Slow 1200mV 0C Model Minimum Pulse Width Summary							
	Clock	Slack	End Point TNS					
1	AUD_BCLK	-3.210	-215.235					
2	CLOCK_50	9.607	0.000					
3	qsys0 altpll_0 sd1 pll7 clk[0]	41.360	0.000					
4	qsys0 altpll_0 sd1 pll7 clk[1]	4999.709	0.000					

Slow	1200mV (OC Model Setup: 'AUD_BCLK'						
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-66.398	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	2.988	69.296
3	-66.275 -66.259	Top:top0[speed_r[2] Top:top0[speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13] Top:top0 AudDSP:dsp0 del_data_r[13]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	2.988	69.173 69.157
4	-66.079	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[15]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.087	69.076
6	-66.050 -66.043	Top:top0 speed_r[0] Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[7] Top:top0 AudDSP:dsp0 del_data_r[10]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	2.988	68.948 68.942
7	-65.956	Top:top0[speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[15]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.087	68.953
8	-65.940	Top:top0[speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[15]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.087	68.937
9 10	-65.927 -65.920	Top:top0 speed_r[2] Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[7] Top:top0 AudDSP:dsp0 del_data_r[10]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	2.988	68.825 68.819
11	-65.911	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[7]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	2.988	68.809
12	-65.904	Top:top0 speed_r[1] Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[10]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	2.989	68.803
13 14	-65.826 -65.777	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[3] Top:top0 AudDSP:dsp0 del_data_r[1]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	2.988 3.158	68.724 68.845
15	-65.735	Top:top0[speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[14]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.758
16	-65.703	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[3] Top:top0 AudDSP:dsp0 del_data_r[3]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	2.988	68.601
17 18	-65.687 -65.658	Top:top0 speed_r[1] Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[3]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	2.988 3.113	68.585 68.681
19	-65.654	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[1]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.158	68.722
20	-65.648 -65.638	Top:top0 speed_r[0] Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[2] Top:top0 AudDSP:dsp0 del_data_r[1]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	2.988 3.158	68.546 68.706
22	-65.620	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[12]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.643
23	-65.612	Top:top0[speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[14]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.635
24	-65.596 -65.539	Top:top0 speed_r[1] Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[14] Top:top0 AudDSP:dsp0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	3.113	68.619 68.562
26	-65.535	Top:top0[speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[11]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.558
27	-65.525	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[2]	qsys0 altpl _0 sd1 pl 7 dk[0]	AUD_BCLK	0.001	2.988	68.423
28 29	-65.519 -65.519	Top:top0 speed_r[0] Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[8] Top:top0 AudDSP:dsp0 del_data_r[11]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	3.113	68.542 68.542
30	-65.509	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[2]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	2.988	68.407
31	-65.497	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[12] Top:top0 AudDSP:dsp0 del_data_r[12]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.520
32	-65.481 -65.416	Top:top0 speed_r[1] Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[12] Top:top0 AudDSP:dsp0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	3.113	68.504 68.439
34	-65.400	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.423
35 36	-65.396 -65.380	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[8] Top:top0 AudDSP:dsp0 del_data_r[8]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK AUD_BCLK	0.001	3.113 3.113	68.419 68.403
37	-65.330	Top:top0 speed_r[1] Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[5]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.353
38	-65.270	Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	3.113	68.293
39 40	-65.207 -65.191	Top:top0 speed_r[2] Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[5] Top:top0 AudDSP:dsp0 del_data_r[5]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	3.113	68.230 68.214
41	-65.147	Top:top0[speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.170
42	-65.131	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.154
43	-65.129 -65.078	Top:top0 speed_r[0] Top:top0 speed_r[0]	Top:top0 AudDSP:dsp0 del_data_r[4] Top:top0 AudDSP:dsp0 del_data_r[0]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	3.113	68.152 68.075
45	-65.006	Top:top0 speed_r[2]	Top:top0 AudDSP:dsp0 del_data_r[4]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.029
46	-64.990	Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[4]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	3.113	68.013
47 48	-64.955 -64.939	Top:top0 speed_r[2] Top:top0 speed_r[1]	Top:top0 AudDSP:dsp0 del_data_r[0] Top:top0 AudDSP:dsp0 del_data_r[0]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK AUD_BCLK	0.001	3.087	67.952 67.936
49	-43.021	Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	44.168
50 51	-42.939 -42.805	Top:top0 AudDSP:dsp0 data_r[1] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13] Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK CLOCK_50	AUD_BCLK AUD_BCLK	1.000	0.128 0.559	44.086 44.353
52	-42.699	Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.230	43.948
53	-42.689	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.559	44.237
54 55	-42.673 -42.667	Top:top0 AudDSP:dsp0 data_r[0] Top:top0 AudDSP:dsp0 data_r[8]	Top:top0 AudDSP:dsp0 del_data_r[7] Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.128 -0.226	43.820 43.460
56	-42.663	Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.132	43.814
57	-42.637	Top:top0 AudDSP:dsp0 data_r[9]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.430 43.719
58 59	-42.629 -42.617	Top:top0[AudDSP:dsp0[data_r[5] Top:top0[AudDSP:dsp0[data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13] Top:top0 AudDSP:dsp0 del_data_r[15]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.071	43.866
60	-42.591	Top:top0 AudDSP:dsp0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.738
61 62	-42.581 -42.566	Top:top0 AudDSP:dsp0 data_r[1] Top:top0 AudDSP:dsp0 data_r[11]	Top:top0 AudDSP:dsp0 del_data_r[10] Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.132 -0.226	43.732 43.359
63	-42.520	Top:top0 AudDSP:dsp0 data_r[10]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.313
64	-42.518	Top:top0 AudDSP:dsp0 data_r[2]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.665
65 66	-42.497 -42.486	Top:top0 AudDSP:dsp0 data_r[3] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[13] Top:top0 AudDSP:dsp0 del_data_r[15]	AUD_BCLK CLOCK_50	AUD_BCLK AUD_BCLK	1.000	0.128 0.658	43.644 44.133
67	-42.457	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.559	44.005
68	-42.451	Top:top0[AudDSP:dsp0[data_r[13]	Top:top0[AudDSP:dsp0[del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.244
69 70	-42.450 -42.449	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1] Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[10] Top:top0 AudDSP:dsp0 del_data_r[3]	CLOCK_50 AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.560	43.999 43.596
71	-42.406	Top:top0 AudDSP:dsp0 data_r[12]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.199
72 73	-42.402 -42.397	Top:top0 AudDSP:dsp0 data_r[4] Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[13] Top:top0 AudDSP:dsp0 del_data_r[1]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.128	43.549 43.717
74	-42.370	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.658	44.017
75	-42.367	Top:top0 AudDSP:dsp0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.514
76 77	-42.355 -42.341	Top:top0 AudDSP:dsp0 data_r[0] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[14] Top:top0 AudDSP:dsp0 del_data_r[7]	AUD_BCLK CLOCK_50	AUD_BCLK AUD_BCLK	1.000	0.256	43.630 43.889
78	-42.334	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.560	43.883
79 80	-42.331 -42.332	Top:top0[AudDSP:dsp0[data_r[8]]	Top:top0 AudDSP:dsp0 del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.110 0.550	43.240
80 81	-42.322 -42.319	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[3] Top:top0 AudDSP:dsp0 data_r[8]	Top:top0 AudDSP:dsp0 del_data_r[13] Top:top0 AudDSP:dsp0 del_data_r[7]	CLOCK_50 AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.559 -0.226	43.870 43.112
82	-42.315	Top:top0 AudDSP:dsp0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[1]	AUD_BCLK	AUD_BCLK	1.000	0.301	43.635
83 84	-42.307 -42.307	Top:top0 AudDSP:dsp0 data_r[5] Top:top0 AudDSP:dsp0 data_r[14]	Top:top0 AudDSP:dsp0 del_data_r[15] Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.173 -0.226	43.499 43.100
85	-42.301	Top:top0[AudDSP:dsp0[data_r[9]	Top:top0 AudDSP:dsp0 del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.210
86	-42.299	Top:top0 AudDSP:dsp0 data_r[15]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.092
87 88	-42.289 -42.284	Top:top0 AudDSP:dsp0 data_r[9] Top:top0 AudDSP:dsp0 data_r[6]	Top:top0 AudDSP:dsp0 del_data_r[7] Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	-0.226 0.128	43.082 43.431
89	-42.281	Top:top0[AudDSP:dsp0[data_r[5]	Top:top0 AudDSP:dsp0 del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.071	43.371
90	-42.280	Top:top0 AudDSP:dsp0 data_r[8]	Top:top0 AudDSP:dsp0 del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	-0.193	43.106
91 92	-42.278 -42.273	Top:top0 AudDSP:dsp0 data_r[0] Top:top0 AudDSP:dsp0 data_r[1]	Top:top0 AudDSP:dsp0 del_data_r[11] Top:top0 AudDSP:dsp0 del_data_r[14]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.256	43.553 43.548
93	-42.271	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[2]	Top:top0 AudDSP:dsp0 del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.559	43.819
94	-42.271	Top:top0[AudDSP:dsp0[data_r[5]	Top:top0 AudDSP:dsp0 del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.075	43.365
95 96	-42.271 -42.250	Top:top0 AudDSP:dsp0 data_r[0] Top:top0 AudDSP:dsp0 data_r[9]	Top:top0 AudDSP:dsp0 del_data_r[2] Top:top0 AudDSP:dsp0 del_data_r[10]	AUD_BCLK AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.128 -0.193	43.418 43.076
97	-42.246	Top:top0 AudDSP:dsp0 data_r[7]	Top:top0 AudDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.393
98 99	-42.240 -42.233	Top:top0[AudDSP:dsp0[data_r[0]	Top:top0 AudDSP:dsp0 del_data_r[12] Top:top0 AudDSP:dsp0 del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.256	43.515
	-42.233 -42.230	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1] Top:top0 AudDSP:dsp0 data_r[11]	Top:top0 AudDSP:dsp0 del_data_r[3] Top:top0 AudDSP:dsp0 del_data_r[15]	CLOCK_50 AUD_BCLK	AUD_BCLK AUD_BCLK	1.000	0.559 -0.110	43.781 43.139

9	Slack	OC Model Setup: 'qsys0 altpll_0 sd1 pll7 From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Del
_	683	Top:top0 AudDSP:dsp0 done_r	Top:top0 state_r[0]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-3.333	2.290
-5.4	465	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r[1]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-3.289	2.116
-5.4		Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r[0]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-3.293	2.080
	332	Top:top0 AudDSP:dsp0 done_r	Top:top0 state_r[2]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-3.329	1.943
	067	Top:top0 AudRecorder:recorder0 addr_r[20]	Top:top0 addr_end_r[20]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 dk[0]	0.001	-2.926 -2.950	2.081
	051 936	Top:top0 AudRecorder:recorder0 addr_r[4] Top:top0 AudRecorder:recorder0 addr_r[11]	Top:top0 addr_end_r[4] Top:top0 addr_end_r[11]	AUD_BCLK AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950 -2.950	2.041 1.926
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[0]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
	920	Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[1]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[2]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9	920	Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[3]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[4]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[5]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[6]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[7]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9 -4.9		Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[8] Top:top0 addr_end_r[9]	AUD_BCLK AUD BCLK	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll 0 sd1 pll7 dk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[10]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932 -2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[11]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.9		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[12]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.932	1.928
-4.8	839	Top:top0 AudRecorder:recorder0 addr_r[7]	Top:top0 addr_end_r[7]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.829
-4.7	753	Top:top0 AudRecorder:recorder0 addr_r[16]	Top:top0 addr_end_r[16]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.767
-4.6	661	Top:top0 AudRecorder:recorder0 addr_r[10]	Top:top0 addr_end_r[10]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.651
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[13]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[14]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[15]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[16]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[17]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6 -4.6		Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[18] Top:top0 addr_end_r[19]	AUD_BCLK AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930 -2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[19]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[20]	AUD_BCLK	gsys0 altpl 0 sd1 pl 7 ck[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[22]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[23]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[24]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.6	616	Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[25]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.930	1.626
-4.5		Top:top0 AudRecorder:recorder0 addr_r[9]	Top:top0 addr_end_r[9]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.577
-4.5		Top:top0 AudRecorder:recorder0 addr_r[21]	Top:top0 addr_end_r[21]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.597
-4.5		Top:top0 AudRecorder:recorder0 addr_r[8]	Top:top0 addr_end_r[8]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.572
-4.		Top:top0 AudRecorder:recorder0 addr_r[2]	Top:top0 addr_end_r[2]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.570
-4.5		Top:top0 AudRecorder:recorder0 addr_r[0]	Top:top0 addr_end_r[0]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.555
-4.1	565	Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[24]	Top:top0 addr_end_r[5]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950 -2.926	1.555
-4.5		Top:top0 AudRecorder:recorder0 addr_r[19]	Top:top0 addr_end_r[24] Top:top0 addr_end_r[19]	AUD_BCLK AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.569
-4.5		Top:top0 AudRecorder:recorder0 addr_r[1]	Top:top0 addr_end_r[1]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.544
-4.5		Top:top0 AudRecorder:recorder0 addr_r[17]	Top:top0 addr_end_r[17]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.567
-4.5		Top:top0 AudRecorder:recorder0 addr_r[14]	Top:top0 addr_end_r[14]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.566
-4.5	539	Top:top0 AudRecorder:recorder0 addr_r[15]	Top:top0 addr_end_r[15]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.553
-4.5	535	Top:top0 AudRecorder:recorder0 addr_r[25]	Top:top0 addr_end_r[25]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.549
-4.5	526	Top:top0 AudRecorder:recorder0 addr_r[13]	Top:top0 addr_end_r[13]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.540
-4.5	523	Top:top0 AudRecorder:recorder0 addr_r[22]	Top:top0 addr_end_r[22]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.537
-4.3		Top:top0 AudRecorder:recorder0 addr_r[12]	Top:top0 addr_end_r[12]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.383
-4.3		Top:top0 AudRecorder:recorder0 addr_r[18]	Top:top0 addr_end_r[18]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.926	1.382
-4.3		Top:top0 AudRecorder:recorder0 addr_r[3]	Top:top0 addr_end_r[3]	AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.349
-4.3 -4.3		Top:top0 AudRecorder:recorder0 addr_r[6]	Top:top0 addr_end_r[6]	AUD_BCLK AUD_BCLK	qsys0 altpll_0 sd1 pll7 clk[0]	0.001	-2.950	1.333
78.		Top:top0 AudRecorder:recorder0 addr_r[23] Debounce:deb1 neg_r	Top:top0 addr_end_r[23] Top:top0 state_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	0.001 83.333	-2.926 -0.475	1.329 4.523
	227	Debounce:deb1 neg_r	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.118	3.987
	227	Debounce:deb1 neg_r	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
79.	227	Debounce:deb1 neg_r	Top:top0 addr_end_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[6]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[7]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
	227	Debounce:deb1 neg_r	Top:top0 addr_end_r[8]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
	227	Debounce:deb1 neg_r	Top:top0 addr_end_r[9]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
	227	Debounce:deb1 neg_r Debounce:deb1 neg_r	Top:top0 addr_end_r[10]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118	3.987
	227 227	Debounce:deb1 neg_r Debounce:deb1 neg_r	Top:top0 addr_end_r[11] Top:top0 addr_end_r[12]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.118 -0.118	3.987
79.		Top:top0 state_r[0]	Top:top0 addr_end_r[12]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[6]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[7]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0]	Top:top0 addr_end_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.289	4.300
79.	321	Top:top0 state_r[0]	Top:top0 addr_end_r[9] Top:top0 addr_end_r[10]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	321	Top:top0 state_r[0] Top:top0 state_r[0]	Top:top0 addr_end_r[10] Top:top0 addr end r[11]	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	83.333 83.333	0.289	4.300 4.300
	321	Top:top0 state_r[0]	Top:top0[addr_end_r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.289	4.300
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[13]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.116	3.685
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[14]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[15]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[16]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[17]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[18]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[19]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[20]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[21]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[22]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.116	3.685
	531	Debounce:deb1 neg_r	Top:top0 addr_end_r[23]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
79.		Debounce:deb1 neg_r	Top:top0 addr_end_r[24]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.116	3.685
	531 600	Debounce:deb1 neg_r	Top:top0 addr_end_r[25]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333 83.333	-0.116 0.285	3.685 4.017
		Top:top0 state_r[2] Top:top0 state_r[2]	Top:top0 addr_end_r[0] Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0] qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.285	4.017
		- op ropo paute_i[e]						
79.6		Top:top0 state_r[2]	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.285	4.017

Slow	1200mV	OC Model Setup: 'CLOCK_50'						
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
47	-2.105	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.967	2.127
48 49	-2.105 -2.103	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 addr_r[8]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_[0] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.967 -0.603	2.127
	-2.103	Top:top0 AudDSP:dsp0 addr_r[9]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.603	2.488
51	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
52 53	-2.101 -2.101	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK 50	1.000	-0.960 -0.960	2.130 2.130
53	-2.101	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
55	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
56	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
57	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
58 59	-2.101 -2.101	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[9] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.960 -0.960	2.130 2.130
60	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[5]	AUD BCLK	CLOCK_50	1.000	-0.960	2.130
61	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
62	-2.095	Top:top0 AudRecorder:recorder0 addr_r[17]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.569
63 64	-2.094 -2.089	Top:top0 AudDSP:dsp0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[2]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[5] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.545 -0.546	2.538
65	-2.089	Top:top0 AudDSP:dsp0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.604	2.467
66	-2.081	Top:top0 AudRecorder:recorder0 addr_r[24]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.555
67	-2.078	Top:top0 AudDSP:dsp0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.540	2.527
68 69	-2.070	Top:top0 AudRecorder:recorder0 addr_r[23]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.544
70	-2.065 -2.064	Top:top0 AudRecorder:recorder0 addr_r[14] Top:top0 AudRecorder:recorder0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.515 -0.532	2.539 2.521
71	-2.061	Top:top0 AudRecorder:recorder0 addr_r[22]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.507
72	-2.052	Top:top0 AudRecorder:recorder0 addr_r[18]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.526
73	-2.039	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
74 75	-2.039 -2.039	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[12] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.969 -0.969	2.059
76	-2.039	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
77	-2.039	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
78	-2.039	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
79	-2.025	Top:top0 AudRecorder:recorder0 addr_r[25]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.471
80 81	-2.000 -1.987	Top:top0 AudDSP:dsp0 addr_r[6] Top:top0 AudRecorder:recorder0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.543 -0.537	2.446 2.439
82	-1.986	Top:top0 AudRecorder:recorder0 addr_r[20]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.432
83	-1.970	Top:top0 AudDSP:dsp0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.603	2.356
84	-1.969	Top:top0 AudRecorder:recorder0 addr_r[4]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.546	2.412
85 86	-1.952 -1.952	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.960 -0.960	1.981 1.981
87	-1.952	Top:top0 AudDSP:tdsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
88	-1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
	-1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
90 91	-1.952 -1.952	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.960 -0.960	1.981
92	-1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
93	-1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
94	-1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
95	-1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
96 97	-1.949 -1.949	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[7] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[6]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.967 -0.967	1.971
98	-1.949	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
99	-1.949	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
100	-1.949	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
55 56	-2.101 -2.101	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[16] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.960 -0.960	2.130 2.130
57	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
58	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
59	-2.101	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
60 61	-2.101 -2.101	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[5] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[3]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK 50	1.000	-0.960 -0.960	2.130 2.130
62	-2.101	Top:top0 AudRecorder:recorder0 addr_r[17]	Lab3 gsys:gsys0 SDRAMWrapper:sdram wrapper 0 addr r[17]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.569
63	-2.094	Top:top0 AudDSP:dsp0 addr_r[5]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.545	2.538
64	-2.089	Top:top0 AudRecorder:recorder0 addr_r[2]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.546	2.532
65	-2.082	Top:top0 AudDSP:dsp0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.604	2.467
66 67	-2.081 -2.078	Top:top0 AudRecorder:recorder0 addr_r[24] Top:top0 AudDSP:dsp0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.515 -0.540	2.555
68	-2.070	Top:top0 AudRecorder:recorder0 addr_r[23]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.544
69	-2.065	Top:top0 AudRecorder:recorder0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.539
70	-2.064	Top:top0 AudRecorder:recorder0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.532	2.521
71 72	-2.061 -2.052	Top:top0 AudRecorder:recorder0 addr_r[22] Top:top0 AudRecorder:recorder0 addr_r[18]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[22] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.543 -0.515	2.507 2.526
73	-2.032	Top:top0 AudRecorder:recorder0 audr_r[18] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.059
74	-2.039	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
75	-2.039	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
76 77	-2.039	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
78	-2.039 -2.039	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[1]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.969 -0.969	2.059
79	-2.025	Top:top0 AudRecorder:recorder0 addr_r[25]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.471
80	-2.000	Top:top0 AudDSP:dsp0 addr_r[6]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.446
81	-1.987	Top:top0 AudRecorder:recorder0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.537	2.439
82 83	-1.986 -1.970	Top:top0 AudRecorder:recorder0 addr_r[20] Top:top0 AudDSP:dsp0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[20] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000	-0.543 -0.603	2.432 2.356
		and the property of the proper		AUD_BCLK	CLOCK_50	1.000	-0.546	2.412
	-1.969	Top:top0 AudRecorder:recorder0 addr_r[4]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]					1.981
84 85	-1.969 -1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.960	
84 85 86	-1.969 -1.952 -1.952	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
84 85 86 87	-1.969 -1.952 -1.952 -1.952	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000 1.000	-0.960 -0.960	1.981 1.981
84 85 86 87 88	-1.969 -1.952 -1.952 -1.952 -1.952	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[28] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000	-0.960 -0.960 -0.960	1.981 1.981 1.981
84 85 86 87 88 89	-1.969 -1.952 -1.952 -1.952	Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23] Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50	1.000 1.000	-0.960 -0.960	1.981 1.981
84 85 86 87 88 89 90	-1,969 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[24 Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[23 Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[3] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[16 Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[16 Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[14 Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[14	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981
84 85 86 87 88 89 90 91	-1,969 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952	Top:topO AudDSP:dopO read_r Top:topO AudDSP:dopO read_r	Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[24] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[23] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[17] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[17] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[14] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[14] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[14] Lab3_gsys:cgys0 SDRAMWrapper:sdram_wrapper_0 laddr_r[10]	AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981 1.981
84 85 86 87 88 89 90 91 92	-1,969 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952	TopttopO[AudDSP:dsp0] read_r	Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[24] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[128] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[18] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[18] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[16] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[10] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[10] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[9] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[9]	AUD_BCLK	CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981
84 85 86 87 88 89 90 91 92 93	-1.969 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[24] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[23] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[17] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[17] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[16] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[16] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[10] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[19] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[16] Lab3_qsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_r[16]	AUD_BCLK	CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981
84 85 86 87 88 89 90 91 92 93	-1,969 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952 -1,952	TopttopO[AudDSP:dsp0] read_r	Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[24] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[128] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[18] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[18] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[16] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[10] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[10] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[9] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_f[9]	AUD_BCLK	CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981
84 85 86 87 88 89 90 91 92 93 94 95 96	-1.969 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.9549 -1.949	Topstop0 (AudDSP:dsp0 (read_r	Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[24] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[23] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[123] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[16] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[16] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[16] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 addr_[17] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 daddr_[17] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 dadta_[17] Lab3_gsys:qsys0 SDRAMWirapper:sdram_wrapper_0 data_[16]	AUD_BCLK	CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50 CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981
84 85 86 87 88 89 90 91 92 93 94 95 96	-1.969 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952 -1.952	TopttopO (AudDSP:dsp0 read_r	Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[24] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[128] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[187] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[187] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[16] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[16] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[19] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[19] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[15] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[15] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[15] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[16] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[16] Lab3 _gsys::gsys0 SDRAMWrapper:sdram_wrapper_0 addr_[16]	AUD_BCLK	CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960 -0.960	1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981 1.981

			ım Pulse Width: 'AUI		cl :	d-4 = '	T- :
l	Slack	Actual Width	Required Width	Type Doct Date	Clock	Clock Edge	Target
	-3.210 -1.285	1.000	4.210 2.285	Port Rate Min Period	AUD_BCLK AUD_BCLK	Rise Rise	AUD_BCLK Top:top0 AudDSP:dsp0 addr_r[0]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0[AudDSP:dsp0[addr_r[10]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[11]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[12]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[13]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[14]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[15]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[16]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[17]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[18]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[19]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[1]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[20]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[21]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[22]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[23]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[24]
)	-1.285 -1.285	1.000	2.285	Min Period Min Period	AUD_BCLK AUD_BCLK	Rise Rise	Top:top0 AudDSP:dsp0 addr_r[25] Top:top0 AudDSP:dsp0 addr_r[26]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[2]
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[3]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[4]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[5]
;	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[6]
,	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[7]
,	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[8]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[9]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[0]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[1]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[2]
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 daclrck_p
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[0]
4	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[10]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[11]
,	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[12]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[13]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[14]
)	-1.285		2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[15]
1	-1.285 -1.285	1.000	2.285	Min Period Min Period	AUD_BCLK AUD_BCLK	Rise Rise	Top:top0 AudDSP:dsp0 data_nxt_r[1] Top:top0 AudDSP:dsp0 data_nxt_r[2]
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0[AudDSP:dsp0[data_nxt_r[3]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[4]
4	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[5]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[6]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[7]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[8]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[9]
9	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[0]
)	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[10]
1	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[11]
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[12]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[13]
4	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[14]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[15]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[1]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[2]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[3]
)	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[4]
)	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[5]
1	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[6]
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[7]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[8]
1	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[9]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[0]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[10]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[11]
8	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[12]
9	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[13]
)	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[14]
1	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[15]
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[1]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[2]
1	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[3]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[4]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[5]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[6]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[7]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[8]
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[9]
_	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 done_r
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 read_r
	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_CALC
	4 8		2.285	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_IDLE
	-1.285	1.000	2.205		AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 state_r.S_PAUSE
; ;	-1.285	1.000	2.285	Min Period		Rise	Top:top0 AudDSP:dsp0 state_r.S_PLAY
i i	-1.285 -1.285	1.000 1.000	2.285	Min Period	AUD_BCLK		
3 1 5 5	-1.285 -1.285 -1.285	1.000 1.000 1.000	2.285 2.285	Min Period Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_r[0
3 1 5 5 7	-1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000	2.285 2.285 2.285	Min Period Min Period Min Period	AUD_BCLK AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_r[0 Top:top0 AudPlayer:player0 bit_counter_r[1
3 4 5 7 3	-1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall	Top:top0 AudPlayer:player0 bit_counter_r[0 Top:top0 AudPlayer:player0 bit_counter_r[1 Top:top0 AudPlayer:player0 bit_counter_r[2
i i i i	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall	Top:top0 AudPlayer:player0 bit_counter_r[(Top:top0 AudPlayer:player0 bit_counter_r[: Top:top0 AudPlayer:player0 bit_counter_r[: Top:top0 AudPlayer:player0 bit_counter_r[:
	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall	Top:top0[AudPlayer:player0[bit_counter_r[c Top:top0[AudPlayer:player0[bit_counter_r[: Top:top0[AudPlayer:player0]bit_counter_r[: Top:top0[AudPlayer:player0[bit_counter_r[: Top:top0[AudPlayer:player0[data_r[0]
;	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall Fall	Top:top0 AudPlayer:player0 bit_counter_r[c Top:top0 AudPlayer:player0 bit_counter_r[: Top:top0 AudPlayer:player0 bit_counter_r[: Top:top0 AudPlayer:player0 bit_counter_r[: Top:top0 AudPlayer:player0 data_r[0] Top:top0 AudPlayer:player0 data_r[10]
3 3 5 7 7 8 9 9 1 1 1 2 2	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall Fall Fall Fall	Top:top0 [AudPlayer:player0 [bit_counter_r[0 Top:top0 [AudPlayer:player0]bit_counter_r[7 Top:top0 [AudPlayer:player0]bit_counter_r[7 Top:top0 [AudPlayer:player0 [bit_counter_r[7 Top:top0 [AudPlayer:player0 [data_r[0] Top:top0 [AudPlayer:player0 [data_r[10] Top:top0 [AudPlayer:player0 [data_r[11]
3 3 5 7 7 8 9 9 1 1 1 2 2	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall Fall	Top:top0 AudPlayer:player0 bit_counter_r[0 Top:top0 AudPlayer:player0 bit_counter_r[1 Top:top0 AudPlayer:player0 bit_counter_r[2 Top:top0 AudPlayer:player0 bit_counter_r[3 Top:top0 AudPlayer:player0 data_r[0] Top:top0 AudPlayer:player0 data_r[10]
3 1 5 5 7 7 3 8 9 9 1 1	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period Min Period Min Period Min Period Min Period Min Period Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall Fall Fall Fall	Top:top0 [AudPlayer:player0]bit_counter_r[0 Top:top0 [AudPlayer:player0]bit_counter_r[2 Top:top0 [AudPlayer:player0]bit_counter_r[2 Top:top0 [AudPlayer:player0]bit_counter_r[2 Top:top0 [AudPlayer:player0]data_r[0] Top:top0 [AudPlayer:player0]data_r[10] Top:top0 [AudPlayer:player0]data_r[11]
22 33 44 55 55 77 73 33 44 55 55	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period	AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	Fall Fall Fall Fall Fall Fall Fall	Top:top0 [AudPlayer:player0 [bit_counter_r[0 Top:top0 [AudPlayer:player0 [bit_counter_r[1 Top:top0 [AudPlayer:player0 [bit_counter_r[2 Top:top0 [AudPlayer:player0 [bit_counter_r[3 Top:top0 [AudPlayer:player0 [data_r[0] Top:top0 [AudPlayer:player0 [data_r[10] Top:top0 [AudPlayer:player0 [data_r[11] Top:top0 [AudPlayer:player0 [data_r[11]
	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period	AUD_BCLK	Fall Fall Fall Fall Fall Fall Fall Fall	Top:top0[AudPlayer:player0]bit_counter_f[0 Top:top0[AudPlayer:player0]bit_counter_f[0 Top:top0[AudPlayer:player0]bit_counter_f[3 Top:top0[AudPlayer:player0]bit_counter_f[3 Top:top0[AudPlayer:player0]data_f[0] Top:top0[AudPlayer:player0]data_f[10] Top:top0[AudPlayer:player0]data_f[11] Top:top0[AudPlayer:player0]data_f[12] Top:top0[AudPlayer:player0]data_f[12]
3 1 5 5 7 7 3 8 9 9 9 1 1 2 2	-1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285 -1.285	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285 2.285	Min Period Min Period	AUD_BCLK	Fall Fall Fall Fall Fall Fall Fall Fall	Top:top0 [AudPlayer:player0 [bit_counter_r[0 Top:top0 [AudPlayer:player0]bit_counter_r[1 Top:top0 [AudPlayer:player0]bit_counter_r[2 Top:top0 [AudPlayer:player0]bit_counter_r[2 Top:top0 [AudPlayer:player0]data_r[0] Top:top0 [AudPlayer:player0]data_r[10] Top:top0 [AudPlayer:player0]data_r[11] Top:top0 [AudPlayer:player0]data_r[12] Top:top0 [AudPlayer:player0]data_r[13] Top:top0 [AudPlayer:player0]data_r[13] Top:top0 [AudPlayer:player0]data_r[14]

Fast	Fast 1200mV 0C Model Setup Summary									
	Clock	Slack	End Point TNS							
1	AUD_BCLK	-35.334	-872.362							
2	qsys0 altpll_0 sd1 pll7 clk[0]	-3.227	-80.252							
3	CLOCK_50	-0.722	-25.743							
4	qsys0 altpll_0 sd1 pll7 clk[1]	80.867	0.000							

Fast	Fast 1200mV 0C Model Minimum Pulse Width Summary									
	Clock	Slack	End Point TNS							
1	AUD_BCLK	-3.000	-268.143							
2	CLOCK_50	9.234	0.000							
3	qsys0 altpll_0 sd1 pll7 dk[0]	41.446	0.000							
4	qsys0 altpll_0 sd1 pll7 dk[1]	4999.779	0.000							

7		, , , = , ,	4999.779	0.000					
asi	1200mV 0	C Model Setup: 'AUD_BCLK'							
	Slack	From Node	ToT	lode	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Dela
	-35.334	Top:top0 speed_r[0]	Top:top0 AudDSP:ds	pOldel data r[13]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.669	36.901
	-35.254	Top:top0 speed r[2]	Top:top0 AudDSP:ds		gsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.669	36.821
	-35.230	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.669	36.797
	-35.181	Top:top0 speed r[0]	Top:top0 AudDSP:ds		gsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.685	36.764
	-35.178	Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.730	36.806
	-35.134	Top:top0 speed r[0]	Top:top0 AudDSP:ds		gsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.669	36.701
	-35.101	Top:top0 speed r[2]	Top:top0 AudDSP:ds		qsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.685	36.684
	-35.098	Top:top0 speed r[2]	Top:top0 AudDSP:ds		gsys0 altpl 0 sd1 pl 7 clk[0]	AUD BCLK	0.001	1.730	36.726
	-35.077	Top:top0 speed r[1]	Top:top0 AudDSP:ds		qsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.685	36.660
)	-35.074	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.730	36.702
1	-35.054	Top:top0 speed r[2]	Top:top0 AudDSP:ds		gsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.669	36.621
2	-35.030	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD BCLK	0.001	1.669	36.597
3	-35.010	Top:top0 speed r[0]	Top:top0 AudDSP:ds		gsys0 altpll 0 sd1 pll7 dk[0]	AUD BCLK	0.001	1.746	36.654
4	-35.001	Top:top0 speed r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1,669	36.568
5	-34.958	Top:top0 speed r[0]	Top:top0 AudDSP:ds		gsys0 altpll 0 sd1 pll7 dk[0]	AUD BCLK	0.001	1.775	36.631
5	-34.942	Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll 0 sd1 pll7 dk[0]	AUD BCLK	0.001	1.746	36,586
7	-34.940	Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD BCLK	0.001	1.669	36.507
3	-34.930					AUD BCLK	0.001	1.746	36.574
,	-34.930	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK			
		Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]		0.001	1.746	36.573
)	-34.921	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.669	36.488
1	-34.906	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.550
	-34.897	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.669	36.464
3	-34.884	Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36.528
	-34.878	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.775	36.551
5	-34.862	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36.506
5	-34.860	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.669	36.427
7	-34.858	Top:top0 speed_r[0]	Top:top0 AudDSP:ds	p0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.502
3	-34.854	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.775	36.527
9	-34.849	Top:top0[speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.493
)	-34.838	Top:top0 speed_r[1]	Top:top0 AudDSP:ds	p0 del_data_r[12]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.482
1	-34.836	Top:top0[speed_r[1]	Top:top0 AudDSP:ds	p0 del_data_r[2]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.669	36.403
2	-34.825	Top:top0 speed_r[1]	Top:top0 AudDSP:ds	p0 del_data_r[11]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.469
3	-34.804	Top:top0 speed_r[2]	Top:top0 AudDSP:ds	p0 del_data_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.448
1	-34.780	Top:top0 speed_r[1]	Top:top0 AudDSP:ds	p0 del_data_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.424
5	-34.778	Top:top0 speed_r[2]	Top:top0 AudDSP:ds	p0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.422
5	-34.754	Top:top0 speed_r[1]	Top:top0 AudDSP:ds	p0 del_data_r[9]	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.398
7	-34.737	Top:top0 speed_r[0]	Top:top0 AudDSP:ds	p0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36.381
3	-34.734	Top:top0 speed_r[0]	Top:top0 AudDSP:ds	p0 del_data_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36.378
,	-34.657	Top:top0 speed_r[2]	Top:top0 AudDSP:ds	p0 del_data_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36.301
)	-34.656	Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD BCLK	0.001	1.746	36.300
ı	-34.654	Top:top0 speed_r[2]	Top:top0 AudDSP:ds	p0ldel data r[5]	gsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36,298
2	-34.633	Top:top0 speed_r[1]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 clk[0]	AUD_BCLK	0.001	1.746	36.277
3	-34.630	Top:top0 speed r[1]	Top:top0 AudDSP:ds		qsys0 altpll 0 sd1 pll7 clk[0]	AUD BCLK	0.001	1,746	36,274
	-34.590	Top:top0 speed_r[0]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.730	36.218
;	-34.576	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD BCLK	0.001	1,746	36,220
,	-34.552	Top:top0 speed_r[1]	Top:top0 AudDSP:ds	– –	qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.746	36.196
	-34.510	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD BCLK	0.001	1.730	36.138
3	-34.486	Top:top0 speed_r[2]	Top:top0 AudDSP:ds		qsys0 altpll_0 sd1 pll7 dk[0]	AUD_BCLK	0.001	1.730	36.114
	-22,482	Lab3 gsys:gsys0 SDRAMWrapper:sdram wrapper 0 data r[1			cLOCK 50	AUD_BCLK AUD_BCLK	1.000	0.123	23.582
,	-22.410	Lab3_qsys:qsysu SDRAMWrapper:sdram_wrapper_u data_r[i Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0			CLOCK_50	AUD_BCLK AUD_BCLK	1.000	0.123	23.582
	-22.410						1.000		23.510
		Top:top0 AudDSP:dsp0 data_r[0]	Top:top0 AudDSP:ds		AUD_BCLK	AUD_BCLK		0.051	
2	-22.344	Top:top0 AudDSP:dsp0 data_r[1]	Top:top0 AudDSP:ds		AUD_BCLK	AUD_BCLK	1.000	0.051	23.402
3	-22.329	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1			CLOCK_50	AUD_BCLK	1.000	0.139	23.445
4	-22.326	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1	Top:top0 AudDSP:ds	p0 del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.184	23.487

20.000 1.0	5 -22.301	Top:top0 AudDSP:dsp0 data_r[8]	Top:top0 Aur	dDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	23.166
20									23.382
20									23.362 23.373
1. 2.0.2.3 Transpoluture groups (1) Tran									23.415
Col.									23.322
2.2.2.1 Inchigation membring of process 100, 100, 100, 100, 100, 100, 100, 10									23.364
6. 22.22 Transacti Auction Continue, 1989 Transaction, 2019 Transaction, 2019 Continue, 2019 C									23.320
Fig. 20.20 The books but was a server and the process prices of the process of the books and					AUD_BCLK				23.077
20 20 10 10 10 10 10 10									23.310
20 20 Tennicol Accident design (1)									23.259
20 20 10 Temperal (Auch Control Contro									23.057
2. 23.13 Lab. Segregation Temperal Author depicted alexes Temperal Author depicted Author Lab. Co. 20.			Top:top0 Aud	dDSP:dsp0 del_data_r[10]					23.265
72 23.13 The temporal Confession of the Co									23.307
2									23.217
7. 20.00 1									23.211
2.1.14 TemporoliusComination TemporoliusComination App. 2007.									23.208
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Fig. 12.55									23.219
55 2.2.05 Leibgroup-processed_amprop_filest_file TempolsActified bedde filest_file Lough DEX Lough 0.00 0.45									23.225
2.200 Topicoplus/BDF projects Topicopl									23.312
2-200									23.267 22.966
99 22.007	7 -22.090	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0	0 data_r[1] Top:top0 Aud	dDSP:dsp0 del_data_r[12]	CLOCK_50	AUD_BCLK	1.000	0.200	23.267
20 20.05 Lab. 20.07 Lab. 20.07 Commonwealth 20.07									23.188
12 20.02 Leads, personage (DEAMWinger under un proper) (Select, 10) Topotopilus/Defended(ed. ptm.) (1) AU, DCK AUD, DCK 1.000 0.38									22.952 23.263
22 - 22.07									23.182
54 22.07 Lab 3_psycare(DCAMPS-Appel) Extraction (Lab Control) Ext	2 -22.082	Top:top0 AudDSP:dsp0 data_r[6]	Top:top0 Aud	dDSP:dsp0 del_data_r[13]					23.140
55 2.2.075 Topicop() AutoPrincip() and (1) Topicop() AutoPrincip() and (1) AD _DIX. AD									23.254
50 2.056 Totatop(AutOF-depolds) Totatop(AutOF-depolds) 4.05 AD_SCK AD_SCK L000 0.19 0.20 0.20 0.20 4.05 4.05 4.05 4.05 4.05 4.05 0.05 0.20 0.20 0.20 4.05 4.0									23.212
	6 -22.069	Top:top0 AudDSP:dsp0 data_r[13]	Top:top0 Aud	dDSP:dsp0 del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	22.934
20.2566 To the tool (Author) Appellation [7] To the tool (Author) Apple (all and p. 10] ALD, BLK ALD, BLK L000 0.09									23.126
To Note Lanch Clock Setury (approximation Setural (1917) Clot Clot Setural (1917) Clot									23.183
Sack From Nobe									23.225
2 - 3.09 Transpol Nuklescenier recorder (johne_f	ast 1200mV (0C Model Setup: 'qsys0 altpll_0 sd1 pll7 c	:lk[0]'						
2 3.059 Topropo/AuSRecorderrecorder/bloken_r Topr	Slack	From Node	To Node	Launch Clor	ck Late	n Clock	Relationship	Clock Skew	Data Delay
3									1.255
4 3.039 Topispo (Justice contract recorded plader y Topispo) (authority control plader y control plader) (princip) (Justice contract recorded plader y Topispo) (authority (princip) (Justice contract recorded plader y Topispo) (Justice contract recorded placer y									1.154
5 2.889 Top:toploubuleDecrete recorder loader [20] Top:toploubuleDecrete recorder loader [11] Top:toploubuleDecrete recorder loader [11] Top:toploubuleDecrete recorder loader [11] Top:toploubuleDecrete recorder loader [11] Top:toploubuleDecrete recorder loader [12] Top:toploubuleDecrete recorder loader [12] Top:toploubuleDecrete recorder loader [12] AD, DCK devoluteDecl olidation load labitive[0] 0.001 1.199 9 2.787 Top:toploubuleDecrete recorder loader [12] Top:toploubuleDecrete recorder loader [13] AD, DCK devoluteDecl olidation load labitive[0] 0.001 1.1690 10 2.787 Top:toploubuleDecrete recorder loader [13] AD, DCK devoluteDecl olidation load labitive[0] 0.001 1.1690 11 2.787 Top:toploubuleDecrete recorder loader [14] AD, DCK devoluteDecl olidation labitive[0] 0.001 1.1690 13 2.787 Top:toploubuleDecrete recorder loader [14] AD, DCK devoluteDecl olidation labitive[16] 0.001 1.1690 14 2.797 Top:toploubuleDecrete recorder loader [16] Top:toploubuleDecrete recorder loader [17] Top:toploubuleDecrete recorder loader [18] AD, DCK devoluteDecl olidation labitive[18] <td< th=""><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>1.092</th></td<>									1.092
6 2,883 Topitopol Judiflecorder recorder blodder j. [1] Topitopol Judiflecorder recorder blodder, and j. [1] ALD, DCLK deprol blatt b									1.131
9 2.797 Tortopol AußRecorder recorder (olden _									1.102
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10 2.797 Toptop AußRecorder recorder Johns Toptop Delds Print Top									1.035
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14 2.797 Topitopo AudRecorder recorderOldone Topitopo Badd end f S ALD BCLK apyso Bath_Oldot Baff Roll Rol	2 -2.797	Top:top0 AudRecorder:recorder0 done_r		AUD_BCLK			.001	-1.690	1.035
15 2.797 Topitopo AudRecorder recorderOldone Topitopo addr _end _f[7] ALD_BCLK apyso alta_0 _plot1 pl7(ak[0) 0.001 -1.690 1.		_ · · · · · _ · ·							1.035
16 2-797 Topttop AudRecorder recorder () Idone Topttop addr. end. [5] AUD. BCLK daysol altra Lold IpT7k(0) 0.001 -1.690									1.035
17							.001	-1.090	1.035
18 2-2797 Topt:top() Aud Recorder:recorder() (done _ f Topt:top() (addr_ end _ f 12) ALD_BCLK qsyso(altpl_ olsd pl f f f t o. 0.01 -1.690 1-1.69						sd 1 Inll 7 Idk [0] (.001	-1.690	
20 2-7.767 ToptopO AudRecorderrecorderO laddr_[7] ToptopO addr_end_f[12] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.690 21 2-7.767 ToptopO AudRecorderrecorderO laddr_[16] ToptopO addr_end_f[16] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.709 22 2-7.722 ToptopO AudRecorderrecorderO laddr_f[16] ToptopO addr_end_f[10] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.709 23 2-698 ToptopO AudRecorderrecorderO laddr_f[10] ToptopO addr_end_f[10] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.709 25 -2.627 ToptopO AudRecorderrecorderO laddr_f[10] ToptopO laddr_end_f[10] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.709 25 -2.627 ToptopO AudRecorderrecorderO laddr_f[18] ToptopO laddr_end_f[10] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.709 26 -2.627 ToptopO AudRecorderrecorderO laddr_f[18] ToptopO laddr_end_f[18] ALD_BCLK qsyso lattpl_O lad1 pl7]ck[0] 0.001 -1.709 26 -2.627 ToptopO AudRecorderrecorderO laddr_f[18] ToptopO laddr_end_f[18] Top	8 -2.797	Top:top0 AudRecorder:recorder0 done_r		AUD_BCLK					1.035
21		Top:top0 AudRecorder:recorder0 done r	Top:top0 addr_end_r[10		qsys0 altpll_0	sd1 pll7 dk[0] (.001	-1.690	
22			Top:top0 addr_end_r[11] AUD_BCLK .] AUD_BCLK	qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0	sd1 p 7 c k[0] (sd1 p 7 c k[0] (sd1 p 7 c k[0] (.001 .001 .001	-1.690 -1.690 -1.690	1.035 1.035 1.035
23 2-698 Toptopo AudRecorderrecordero addr_f[10] Toptopo addr_end_f[10] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 24 -2.635 Toptopo AudRecorderrecordero addr_f[9] Toptopo addr_end_f[9] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 25 -2.627 Toptopo AudRecorderrecordero addr_f[8] Toptopo addr_end_f[8] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 26 -2.627 Toptopo AudRecorderrecordero addr_f[21] Toptopo addr_end_f[8] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 28 -2.627 Toptopo AudRecorderrecordero addr_f[21] Toptopo addr_end_f[21] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 28 -2.622 Toptopo AudRecorderrecordero addr_f[21] Toptopo addr_end_f[3] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 29 -2.622 Toptopo AudRecorderrecordero addr_f[3] Toptopo addr_end_f[5] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.709 29 -2.622 Toptopo AudRecorderrecordero addr_f[14] Toptopo addr_end_f[5] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.696 31 -2.617 Toptopo AudRecorderrecordero addr_f[14] Toptopo addr_end_f[14] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.696 32 -2.616 Toptopo AudRecorderrecordero done_f Toptopo addr_end_f[14] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.687 32 -2.616 Toptopo AudRecorderrecordero done_f Toptopo addr_end_f[15] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.687 34 -2.616 Toptopo AudRecorderrecordero done_f Toptopo addr_end_f[15] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.687 35 -2.616 Toptopo AudRecorderrecordero done_f Toptopo addr_end_f[15] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.687 37 -2.616 Toptopo AudRecorderrecordero done_f Toptopo addr_end_f[15] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1.687 39 -2.616 Toptopo AudRecorderrecordero done_f Toptopo addr_end_f[15] ALD_BCLK qsyso altpl_0 sd1 pl7 ck[0] 0.001 -1		Top:top0 AudRecorder:recorder0 done_r	Top:top0 addr_end_r[11 Top:top0 addr_end_r[12	D AUD_BCLK D AUD_BCLK D AUD_BCLK	qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0	sd1 p 7 dk[0] (sd1 p 7 dk[0] (sd1 p 7 dk[0] (sd1 p 7 dk[0] (.001 .001 .001	-1.690 -1.690 -1.690 -1.690	1.035 1.035 1.035 1.035
24		Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7]	Top:top0 addr_end_r[11 Top:top0 addr_end_r[12 Top:top0 addr_end_r[7]] AUD_BCLK L] AUD_BCLK AUD_BCLK AUD_BCLK	qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0	sd1 pll7 dk[0] ()	.001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709	1.035 1.035 1.035 1.035 0.986
26 2-627 Top:topO AudRecorder:recorderO addr_[8] Top:topO addr_end_f[8] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.709 27 -2.627 Top:topO AudRecorder:recorderO addr_f[2] Top:topO addr_end_f[2] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.696 28 -2.626 Top:topO AudRecorder:recorderO addr_f[5] Top:topO addr_end_f[2] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.709 29 -2.622 Top:topO AudRecorder:recorderO addr_f[5] Top:topO addr_end_f[5] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.709 30 -2.618 Top:topO AudRecorder:recorderO addr_f[19] Top:topO addr_end_f[19] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.696 32 -2.616 Top:topO AudRecorder:recorderO addr_f[14] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 33 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[14] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 34 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[14] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 35 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[16] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 35 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[16] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 35 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[16] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 37 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[16] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 38 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[19] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[19] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorderO done_f Top:topO addr_end_f[2] ALD_BCLK qsysO altpl_0 sd1 pl7fck[0] 0.001 -1.687 41 -2.616 Top		Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[12] Top:top0 addr_end_r[7] Top:top0 addr_end_r[16]	aud_bclk Aud_bclk Aud_bclk Aud_bclk Aud_bclk Aud_bclk	qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0 qsys0 altpll_0	sd1 p 7 dk[0] ()	.001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.696	1.035 1.035 1.035 1.035 0.986 0.954
27	3 -2.698	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[12] Top:top0 addr_end_r[7] Top:top0 addr_end_r[16] Top:top0 addr_end_r[10]	I] AUD_BCLK I] AUD_BCLK I] AUD_BCLK AUD_BCLK I] AUD_BCLK I] AUD_BCLK	qsys0 altpl_0 qsys0 altpl_0 qsys0 altpl_0 qsys0 altpl_0 qsys0 altpl_0 qsys0 altpl_0 qsys0 altpl_0	sd1 p 7 dk 0] (sd1 p 7 dk 0] (.001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.696 -1.709	1.035 1.035 1.035 1.035 0.986
26 2-6.26 TopttopO AudRecorder recorder Oladdr _ [7] TopttopO addr _ end _ [7] ALD _ BCLK qsys0 altpl_0 olad plr] Clk[0] 0.001 -1.709	23 -2.698 24 -2.635 25 -2.627	Top:top0 AudRecorder:recorder0 [doner Top:top0 AudRecorder:recorder0 addrr[7] Top:top0 AudRecorder:recorder0 addrr[16] Top:top0 AudRecorder:recorder0 addrr[10] Top:top0 AudRecorder:recorder0 addrr[9] Top:top0 AudRecorder:recorder0 addrr[0]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[12] Top:top0 addr_end_r[7] Top:top0 addr_end_r[16] Top:top0 addr_end_r[10] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9]	I] AUD_BCLK I] AUD_BCLK AUD_BCLK AUD_BCLK I] AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	qsys0 altpll_0	sd1 p 7 dk 0 ()	.001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.696 -1.709 -1.709 -1.709	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846
29 2-6.22 Top:topO AudRecorder:recorderO addr_r[5] Top:topO addr_end_r[5] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.709 30 2-6.18 Top:topO AudRecorder:recorderO addr_r[19] Top:topO AudRecorder:recorderO addr_r[19] Top:topO AudRecorder:recorderO addr_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.696 32 2-6.16 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 33 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 34 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[18] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 35 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[18] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 35 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[18] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 37 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 38 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 38 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[2] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[2] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[2] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsysO altpl_0 sd1 pl7 ck[0] 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorderO do	-2.698 -4 -2.635 -5 -2.627 -6 -2.627	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[0]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[72] Top:top0 addr_end_r[73] Top:top0 addr_end_r[16] Top:top0 addr_end_r[10] Top:top0 addr_end_r[0] Top:top0 addr_end_r[0] Top:top0 addr_end_r[0]	I) AUD_BCLK I] AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK I] AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK AUD_BCLK	qsys0 altpl_0	sd1 p 7 dk 0 (sd1 p 7 dk 0 (.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846
2-2.618 TopttopO AudRecorder recorder O addr _ [19] TopttopO addr _ end _ [19] ALD _ BCLK qsys0 altpli_0 sol 1 pi17 ck[0] 0.001 -1.696	-2.698 -4 -2.635 -5 -2.627 -6 -2.627 -7 -2.627	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[8] Top:top0 AudRecorder:recorder0 addr_r[21]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[12] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[10] Top:top0 addr_end_r[9] Top:top0 addr_end_r[0] Top:top0 addr_end_r[0] Top:top0 addr_end_r[0] Top:top0 addr_end_r[21]	I) AUD_BCLK I.] AUD_BCLK I.] AUD_BCLK AUD_BCLK I.] AUD_BCLK I.] AUD_BCLK	qsys0 (altpl. 0) qsys0 (altpl. 0)	sd1 p r ck[0] (.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.696 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696	1.035 1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846 0.846
2-2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[14] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 33 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[15] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 33 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[15] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 35 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[15] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 35 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[16] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 35 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[18] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 37 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[18] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 39 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[19] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 39 -2.616 TopttopO AudRecorderrecorderO done r TopttopO addr_end_r[19] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 40 -2.616 TopttopO AudRecorderrrecorderO done r TopttopO addr_end_r[20] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 41 -2.616 TopttopO AudRecorderrrecorderO done r TopttopO addr_end_r[21] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 42 -2.616 TopttopO AudRecorderrrecorderO done r TopttopO addr_end_r[22] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 43 -2.616 TopttopO AudRecorderrrecorderO done r TopttopO addr_end_r[22] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 45 -2.616 TopttopO AudRecorderrrecorderO done r TopttopO addr_end_r[24] ALD_BCLK qsysO altpl_O sd1 pl77(dk[0) 0.001 -1.687 45 -2.616 TopttopO AudRecorderrrecorderO done r TopttopO addr_end_r[24] ALD_BCLK qsysO altpl_O sd1 pl	3 -2.698 44 -2.635 5 -2.627 66 -2.627 77 -2.627 88 -2.626	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[8] Top:top0 AudRecorder:recorder0 addr_f[8] Top:top0 AudRecorder:recorder0 addr_f[8] Top:top0 AudRecorder:recorder0 addr_f[8]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[16] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[8] Top:top0 addr_end_r[8] Top:top0 addr_end_r[7]	I) AUD_BCLK I] AUD_BCLK	qsys0 (altpl. 0) qsys0 (altpl. 0)	sd i jol7 (dk(0) (.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846 0.846 0.849
33 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[14] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687	23 -2.698 24 -2.635 25 -2.627 26 -2.627 27 -2.627 28 -2.626 29 -2.622	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[0] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2]	Top:top0 addr_end_r[11 Top:top0 addr_end_r[12] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[8] Top:top0 addr_end_r[8] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7]] AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK I] AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK AUD_BCIK	qsys0 [altpl_0]	sd 1 pl7 clk (0) ()	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.696 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709	1.035 1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846 0.846
34 2-6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[15] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 35 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[16] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 36 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[18] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 37 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[18] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 38 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[19] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 40 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[20] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 40 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO]addr_end_r[21] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 41 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO[addr_end_r[22] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 42 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO[addr_end_r[22] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 43 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO[addr_end_r[23] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 44 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO[addr_end_r[24] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 45 -2.6.16 TopttopO]AudRecorderrecorderO]done_r TopttopO[addr_end_r[24] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 45 -2.6.16 TopttopO]AudRecorderrecorderO[addr_r[15] TopttopO[addr_end_r[15] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.687 45 -2.6.16 TopttopO]AudRecorderrecorderO[addr_r[15] TopttopO[addr_end_r[15] ALD_BCLK qsysO alpli_O[sd1]pl7[ck[0] 0.001 -1.696 47 -2.6.11 TopttopO]AudRecorderrecorderO[addr_r[15] TopttopO[addr_end_r[25] ALD_BCLK qsysO alpl	23 -2.698 24 -2.635 25 -2.627 26 -2.627 27 -2.627 28 -2.626 29 -2.622 20 -2.618 21 -2.617	Top:top0 AudRecorder:recorder0 doner Top:top0 AudRecorder:recorder0 addrr[7] Top:top0 AudRecorder:recorder0 addrr[7] Top:top0 AudRecorder:recorder0 addrr[16] Top:top0 AudRecorder:recorder0 addrr[9] Top:top0 AudRecorder:recorder0 addrr[19] Top:top0 AudRecorder:recorder0 addrr[19]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[8] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[8] Top:top0 addr_end_r[8] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[12] Top:top0 addr_end_r[13] Top:top0 addr_end_r[14]	I) AUD_BCLK I] AUD_BCLK	qsys0 (altpl. 0)	sed i pit7 (clk(0) (c) sed i pit7 (c) sed i pit7 (c) sed i pit7 (clk(0) (c) sed i pit7 (clk(0) (c) sed i pit7	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.696 -1.696	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846 0.846 0.846 0.845 0.845 0.845
35 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[16] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 36 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[17] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 37 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 38 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[20] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 39 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[20] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[21] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[21] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 42 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[23] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 43 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 44 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 45 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 46 -2.612 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[15] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.687 46 -2.612 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[15] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.686 46 -2.612 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[17] ALD_BCLK qsysO altpl_0 sd1 pl7 clk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[25] Top:topO addr_end_r[25] AL	23 -2.698 24 -2.635 25 -2.627 26 -2.627 27 -2.627 28 -2.626 29 -2.622 20 -2.618 21 -2.617 22 -2.616	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10]	Top:top0 addr_end_r[11 Top:top0 addr_end_r[12 Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[4] Top:top0 addr_end_r[4] Top:top0 addr_end_r[4] Top:top0 addr_end_r[4] Top:top0 addr_end_r[4]	AUD_BCLK AUD_BCLK	qsys0 [altpl.]) qsys0 [altpl.] qsys0 [altpl.]) qsys0 [altpl.]] qsys0 [altpl.]] qsys0 [altpl.]] qsys0 [altpl.]] qsys0 [altpl.]]	sd 1 [n]7 [dk(0) c d n]7 [dk(0) n]	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.696 -1.709 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.854 0.846 0.846 0.845 0.845 0.841 0.845 0.841
36 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[17] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 37 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[18] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 38 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[20] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 39 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[20] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[21] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[22] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 42 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[23] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 43 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 44 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 45 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 45 -2.616 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 47 -2.611 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[15] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[25] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 50 -2.600 Top:topO AudRecorder:recorderO addr_r[25] Top:topO addr_end_r[25] ALD_BCLK q	23 -2.698 24 -2.635 25 -2.627 26 -2.627 27 -2.627 27 -2.626 29 -2.626 20 -2.618 21 -2.617 22 -2.616 23 -2.616	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 AudRecorder:recorder0 addr_r[14]	Toptopol addr _end _f[1] Toptopol addr _end _f[2] Toptopol addr _end _f[2] Toptopol addr _end _f[3] Toptopol addr _end _f[6] Toptopol addr _end _f[6] Toptopol addr _end _f[9] Toptopol addr _end _f[9] Toptopol addr _end _f[8] Toptopol addr _end _f[8] Toptopol addr _end _f[2] Toptopol addr _end _f[2] Toptopol addr _end _f[3] Toptopol addr _end _f[3] Toptopol addr _end _f[3] Toptopol addr _end _f[4] Toptopol addr _end _f[4] Toptopol addr _end _f[4] Toptopol addr _end _f[14]	AUD_BCLK AUD_BCLK	qsys0 [altpl_0]	sed 1 [n17 clk(0) cl sed 1 [n17 clk(0)	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.696 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.696 -1.709 -1.686 -1.687	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.846 0.846 0.846 0.845 0.845 0.841 0.859
37 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[18] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 38 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[19] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 39 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[20] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[21] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 42 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[22] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 42 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[23] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 43 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 44 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 45 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 45 -2.612 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[15] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 47 -2.611 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[17] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[27] Top:topO addr_end_r[25] ALD_BCLK	23 -2.698 24 -2.635 25 -2.627 26 -2.627 27 -2.627 28 -2.626 29 -2.626 20 -2.618 21 -2.616 21 -2.616 22 -2.616 23 -2.616 24 -2.616	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[7]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[8] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7]	I) AUD_BCLK I] AUD_BCLK	qsys0 (altpl0)	sd 1 [n]7 [dk(0) cd 1 [n]7 [dk	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.686 -1.687	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.846 0.846 0.849 0.845 0.845 0.845 0.845 0.845 0.845 0.845
39 -2.616 Top:topO AudRecorder:recorder0 done_r Top:topO addr_end_r[20] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 40 -2.616 Top:topO AudRecorder:recorder0 done_r Top:topO addr_end_r[21] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 41 -2.616 Top:topO AudRecorder:recorder0 done_r Top:topO addr_end_r[23] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 42 -2.616 Top:topO AudRecorder:recorder0 done_r Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 43 -2.616 Top:topO AudRecorder:recorder0 addr_r[24] Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 42 -2.616 Top:topO AudRecorder:recorder0 addr_r[24] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 45 -2.616 Top:topO AudRecorder:recorder0 addr_r[15] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 45 -2.612 Top:topO AudRecorder:recorder0 addr_r[15] Top:topO addr_end_r[15] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 47 -2.611 Top:topO AudRecorder:recorder0 addr_r[17] Top:topO addr_end_r[17] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorder0 addr_r[25] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorder0 addr_r[25] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 50 -2.600 Top:topO AudRecorder:recorder0 addr_r[25] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 51 -2.600 Top:topO AudRecorder:recorder0 addr_r[13] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 51 -2.600 Top:topO AudRecorder:recorder0 addr_r[15] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 51 -2.600 Top:topO AudRecorder:recorder0 addr_r[15]	23 -2.698 24 -2.635 25 -2.627 27 -2.627 27 -2.627 28 -2.626 29 -2.622 00 -2.618 11 -2.617 2.616 2.616 2.616 4 -2.616 4 -2.616	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[8] Top:top0 AudRecorder:recorder0 addr_r[8] Top:top0 AudRecorder:recorder0 addr_r[7]	Toptobol addr. end. [11] Toptobol addr. end. [12] Toptobol addr. end. [12] Toptobol addr. end. [16] Toptobol addr. end. [16] Toptobol addr. end. [16] Toptobol addr. end. [16] Toptobol addr. end. [19] Toptobol addr. end. [19] Toptobol addr. end. [19] Toptobol addr. end. [16] Toptobol addr. end. [16] Toptobol addr. end. [15] Toptobol addr. end. [16] Toptobol addr. end. [16] Toptobol addr. end. [16] Toptobol addr. end. [17] Toptobol addr. end. [15]	ALD_BCLK ALD_	qsys0 [altpl.]) qsys0 [altpl.]]	sed i jel7 (elk(0) c sed i jel	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.686 -1.709 -1.687 -1.687 -1.687	1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.846 0.846 0.846 0.845 0.845 0.841 0.859
40 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 add_end_r[2] AUD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687	33 -2.698 44 -2.635 56 -2.627 77 -2.627 78 -2.626 8 -2.626 9 -2.622 90 -2.618 11 -2.616 13 -2.616 15 -2.616 15 -2.616 16 -2.616	Top:top0 AudRecorder:recorder0 Joddr[7] Top:top0 AudRecorder:recorder0 Jodne[7]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[8] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[8] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[8] Top:top0 addr_end_r[14] Top:top0 addr_end_r[14] Top:top0 addr_end_r[15] Top:top0 addr_end_r[15] Top:top0 addr_end_r[15] Top:top0 addr_end_r[15] Top:top0 addr_end_r[15] Top:top0 addr_end_r[15]	ALD_BCLK ALD_	qsys0 (altpl. 0)	sd 1 [n] 7 [dk(0) sd 1 [.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.696 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.696 -1.687 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.036 1.036 1.035 1.036 1.035
41 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 addr_end_r[22] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 42 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 addr_end_r[23] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 43 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 addr_end_r[24] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 44 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 addr_end_r[24] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 45 -2.616 Top:top0 AudRecorder:recorder0 addr_r[15] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.687 46 -2.612 Top:top0 AudRecorder:recorder0 addr_r[15] Top:top0 addr_end_r[15] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 47 -2.611 Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 addr_end_r[17] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.709 48 -2.610 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 49 -2.606 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 50 -2.601 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696	33 -2.698 44 -2.635 45 -2.627 46 -2.627 47 -2.627 48 -2.626 40 -2.616 41 -2.616 42 -2.616 44 -2.616 45 -2.616 46 -2.616 47 -2.616 48 -2.616 48 -2.616 49 -2.616 40 -2.616 40 -2.616 40 -2.616 41 -2.616 42 -2.616 43 -2.616 44 -2.616 45 -2.616 46 -2.616 47 -2.616 48 -2.616 49 -2.616 40 -2.616	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10]	Toptobol addr. end. [f.1] Toptobol addr. end. [r.1] Toptobol addr. end. [r.1] Toptobol addr. end. [r.1] Toptobol addr. end. [r.1] Toptobol addr. end. [r.16] Toptobol addr. end. [r.10] Toptobol addr. end. [r.12] Toptobol addr. end. [r.12] Toptobol addr. end. [r.13] Toptobol addr. end. [r.14] Toptobol addr. end. [r.14] Toptobol addr. end. [r.14] Toptobol addr. end. [r.16]	ALD_BCLK ALD	qsys0 [altpl.]) qsys0 [altpl.]]	sed 1 [n17 [clk(0)] clc sed 1	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.686 -1.687 -1.687 -1.687 -1.687 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.036 0.996 0.9954 0.917 0.846 0.846 0.846 0.849 0.845 0.841 0.850 0.849 0.857 0.857 0.857 0.857 0.857
42 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[23] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 43 -2.616 Top:topO AudRecorder:recorderO addr_r[24] Top:topO addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 44 -2.616 Top:topO AudRecorder:recorderO done_r Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 45 -2.616 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[15] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.687 46 -2.612 Top:topO AudRecorder:recorderO addr_r[15] Top:topO addr_end_r[15] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 47 -2.611 Top:topO AudRecorder:recorderO addr_r[17] Top:topO addr_end_r[17] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.709 48 -2.610 Top:topO AudRecorder:recorderO addr_r[25] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 49 -2.606 Top:topO AudRecorder:recorderO addr_r[25] Top:topO addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 50 -2.601 Top:topO AudRecorder:recorderO addr_r[13] Top:topO addr_end_r[13] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 51 -2.600 Top:topO AudRecorder:recorderO addr_r[13] Top:topO addr_end_r[13] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696 51 -2.600 Top:topO AudRecorder:recorderO addr_r[13] Top:topO addr_end_r[13] ALD_BCLK qsys0 altpl_0 sd1 pl7(dk[0) 0.001 -1.696	3 -2.698 4 -2.635 5 -2.627 7 -2.627 8 -2.626 9 -2.618 1 -2.617 2 -2.616 4 -2.616 4 -2.616 6 -2.616 6 -2.616 8 -2.616 9 -2.616	Top:top0 AudRecorder:recorder0 Joddr_[7] Top:top0 AudRecorder:recorder0 Jodne_[7]	Toptopol addr end _fill Topttopol addr end _fill Topttopol addr end _fill Topttopol addr end _file Topttopol addr end _fi	AUD_BCLK AUD	qsys0 (altpl. 0)	sd 1 [n] 7 [dk(0) sd 1 [.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.687 -1.687 -1.687 -1.687 -1.687	1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.846 0.846 0.846 0.848 0.845 0.841 0.857 0.857 0.857 0.857
43	3 -2.698 4 -2.627 5 -2.627 7 -2.627 8 -2.628 9 -2.622 0 -2.618 11 -2.617 2.616 4 -2.616 6 -2.616 6 -2.616 7 -2.616 8 -2.616 9 -2.616 0 -2.616 0 -2.616 0 -2.616	Top:top0 AudRecorder:recorder0 done_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[10] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 addr_r[19]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[9] Top:top0 addr_end_r[2] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[14] Top:top0 addr_end_r[14] Top:top0 addr_end_r[15] Top:top0 addr_end_r[16] Top:top0 addr_end_r[17] Top:top0 addr_end_r[18] Top:top0 addr_end_r[17] Top:top0 addr_end_r[18] Top:top0 addr_end_r[17] Top:top0 addr_end_r[18] Top:top0 addr_end_r[18] Top:top0 addr_end_r[18] Top:top0 addr_end_r[18] Top:top0 addr_end_r[18] Top:top0 addr_end_r[18]	ALD_BCLK	qsys0 (altpl. 0)	sd 1 [n]7 [dk(0) cd 1 [n]7 [dk	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.696 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687	1.035 1.035 1.035 1.035 1.035 0.986 0.996 0.917 0.854 0.817 0.846 0.849 0.849 0.845 0.841 0.850 0.849 0.857 0.857 0.857 0.857 0.857
44 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 addr_end_r[24] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 45 -2.616 Top:top0 AudRecorder:recorder0 done_r Top:top0 addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.687 46 -2.612 Top:top0 AudRecorder:recorder0 addr_r[15] Top:top0 addr_end_r[15] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 47 -2.611 Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 addr_end_r[17] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.709 48 -2.610 Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 addr_end_r[17] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 49 -2.606 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 50 -2.601 Top:top0 AudRecorder:recorder0 addr_r[21] Top:top0 addr_end_r[25] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] ALD_BCLK qsys0 altpl_0 sd1 pl7 dk[0] 0.001 -1.696	3 -2.698 4 -2.627 5 -2.627 7 -2.627 9 -2.622 9 -2.622 10 -2.616 10 -2.616 11 -2.616 12 -2.616 13 -2.616 14 -2.616 15 -2.616 16 -2.616 17 -2.616 18 -2.616 19 -2.616 10 -2.616 10 -2.616 11 -2.616	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[12] Top:top0 AudRecorder:recorder0 addr_f[12]	Toptobol addr. end. [f.1] Toptobol addr. end. [r.1]	ALD_BCLK	qsys0 [altpl_0]	sed 1 [n17 cls(0) cls 1 n17 cls(0)	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.035 1.036 1.035
46 -2.612 Top:top0 AudRecorder:recorder0 addr_[15] Top:top0 addr_end_f[15] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 47 -2.611 Top:top0 AudRecorder:recorder0 addr_f[1] Top:top0 addr_end_f[1] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.709 48 -2.610 Top:top0 AudRecorder:recorder0 addr_f[17] Top:top0 addr_end_f[17] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 49 -2.660 Top:top0 AudRecorder:recorder0 addr_f[25] Top:top0 addr_end_f[25] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 50 -2.601 Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 addr_end_f[21] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_f[13] Top:top0 addr_end_f[13] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 52 -2.601 Top:top0 AudRecorder:recorder0 addr_f[13] Top:top0 addr_end_f[13] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696 53 -2.600 Top:top0 AudRecorder:recorder0 addr_f[13] Top:top0 addr_end_f[13] AUD_BCLK qsys0 altpl_0 sd1 plf7 dk[0] 0.001 -1.696	3 -2.698 4 -2.632 4 -2.627 7 -2.627 7 -2.627 9 -2.622 0 -2.618 3 -2.616 4 -2.616 5 -2.616 6 -2.616 7 -2.616 9 -2.616 9 -2.616 0 -2.616 9 -2.616 0 -2.616	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[8] Top:top0 AudRecorder:recorder0 addr_f[8] Top:top0 AudRecorder:recorder0 addr_f[8] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[19]	Topt:top0 addr_end_r[1] Topt:top0 addr_end_r[2] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[8]	AUD_BCLK AUD	qsys0 (altpl)	sd 1 [n]7 [dk(0) cd 1 [n]7 [dk	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.954 0.917 0.846 0.849 0.849 0.845 0.841 0.859 0.845 0.841 0.857 0.857 0.857 0.857 0.857
47 -2.611 Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 addr_end_r[1] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.709 48 -2.610 Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 addr_end_r[17] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696 49 -2.606 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696 50 -2.601 Top:top0 AudRecorder:recorder0 addr_r[22] Top:top0 addr_end_r[13] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696	3 -2.698 4 -2.627 7 -2.627 7 -2.627 9 -2.622 9 -2.622 1 -2.616 1 -2.616 2 -2.616 6 -2.616 6 -2.616 7 -2.616 8 -2.616 9 -2.616 1 -2.616 1 -2.616 2 -2.616 2 -2.616 3 -2.616 4 -2.616 4 -2.616 4 -2.616 4 -2.616 4 -2.616 7 -2.616 7 -2.616 8 -2.616 9 -2.616 1 -2.616 1 -2.616 1 -2.616 1 -2.616 1 -2.616 1 -2.616 1 -2.616 1 -2.616 2 -2.616 3 -2.616 4 -2.616	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[10] Top:top0 AudRecorder:recorder0 addr_f[12] Top:top0 AudRecorder:recorder0 addr_f[12]	Topstop0 addr_end_r[11] Topstop0 addr_end_r[2] Topstop0 addr_end_r[7] Topstop0 addr_end_r[7] Topstop0 addr_end_r[7] Topstop0 addr_end_r[7] Topstop0 addr_end_r[7] Topstop0 addr_end_r[8] Topstop0 addr_end_r[8] Topstop0 addr_end_r[7] Topstop0 addr_end_r[7] Topstop0 addr_end_r[7] Topstop0 addr_end_r[8]	ALD_BCLK	qsys0 (altpl0)	sd 1 [n]7 [dk(0) cd 1 [n]7 [dk	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.854 0.846 0.846 0.846 0.848 0.845 0.841 0.857
48 -2.610 Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 addr_end_r[17] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696 49 -2.606 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696 0.2601 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 pl7 clk[0] 0.001 -1.696 0.001 0.00	3 -2.698 44 -2.627 5 -2.627 78 -2.627 8 -2.626 9 -2.628 9 -2.628 11 -2.617 22 -2.616 44 -2.616 5 -2.616 8 -2.616 77 -2.616 8 -2.616 9 -2.616 10 -2	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[2] Top:top0 AudRecorder:recorder0 addr_f[2] Top:top0 AudRecorder:recorder0 addr_f[2] Top:top0 AudRecorder:recorder0 addr_f[2] Top:top0 AudRecorder:recorder0 addr_f[3] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[19]	Topt:top0 addr_end_r[11] Topt:top0 addr_end_r[2] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[8]	AUD_BCIK	qsys0 (altpl. 0)	sed 1 [n17 [ck](0) ckd 1 [n1	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 0.986 0.9986 0.994 0.917 0.854 0.846 0.846 0.846 0.849 0.857
49 -2.606 Top:top0 AudRecorder:recorder0 addr_r[25] Top:top0 addr_end_r[25] AUD_BCLK qsys0 altpl_0 sd1 pll7 clk[0] 0.001 -1.696 50 -2.601 Top:top0 AudRecorder:recorder0 addr_r[22] Top:top0 addr_end_r[22] AUD_BCLK qsys0 altpl_0 sd1 pll7 clk[0] 0.001 -1.696 51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] AUD_BCLK qsys0 altpl_0 sd1 pll7 clk[0] 0.001 -1.696	3 -2.698 4 -2.627 7 -2.627 7 -2.627 9 -2.622 9 -2.622 9 -2.622 -2.616 4 -2.616 5 -2.616 8 -2.616 8 -2.616 0 -2.616 1 -2.616 3 -2.616 0 -2.616 1 -2.616 3 -2.616 0 -2.616 1 -2.616 0 -2.616 1 -2.616 0 -2.616 1 -2.616 0 -2.616	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[2] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[9]	Top:top0 addr_end_r[11] Top:top0 addr_end_r[2] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[8] Top:top0 addr_end_r[8] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[7] Top:top0 addr_end_r[8]	ALD_BCLK ALD	qsys0 altpl_0	sd 1 [n]7 [dk(0) cd 1 [n]7 [dk	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.709 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.854 0.849 0.849 0.849 0.849 0.857
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51 -2.600 Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 addr_end_r[13] AUD_BCLK qsys0 altpll_0 sd1 pll7 dk[0] 0.001 -1.696	3 -2.698 4 -2.627 5 -2.627 7 -2.627 7 -2.627 9 -2.622 9 -2.622 9 -2.622 1 -2.616 4 -2.616 5 -2.616 8 -2.616 7 -2.616 8 -2.616 1 -2.616 1 -2.616 3 -2.616 3 -2.616 5 -2.616 5 -2.616 5 -2.616 6 -2.616 7 -2.616 6 -2.616 7 -2.616 8 -2.616 6 -2.616 7 -2.616 8 -2.616 6 -2.616 7 -2.616 8 -2.616 7 -2.616 8 -2.616 9 -2.6	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[21] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[19]	Topt:top0 addr_end_r[11] Topt:top0 addr_end_r[2] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[8] Topt:top0 addr_end_r[8] Topt:top0 addr_end_r[8] Topt:top0 addr_end_r[8] Topt:top0 addr_end_r[8] Topt:top0 addr_end_r[9] Topt:top0 addr_end_r[14] Topt:top0 addr_end_r[15] Topt:top0 addr_end_r[16] Topt:top0 addr_end_r[17] Topt:top0 addr_end_r[16] Topt:top0 addr_end_r[17] Topt:top0 addr_end_r[17]	ALD BCLK	qsys0 altpl_0	sd 1 [n]7 [dk(0) dd 1 [n]7 [dk	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.854 0.849 0.849 0.849 0.849 0.857
52 -2.535 Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 addr_end_r[12] AUD_BCLK qsys0 altpll_0 sd1 pll7 clk[0] 0.001 -1.709	3 -2.698 4 -2.627 7 -2.627 7 -2.627 9 -2.622 9 -2.622 10 -2.616 10 -2.616 10 -2.616 10 -2.616 10 -2.616 10 -2.616 10 -2.616 10 -2.616 10 -2.616 10 -2.616 11 -2.616 11 -2.616 12 -2.616 12 -2.616 13 -2.616 14 -2.616 14 -2.616 15 -2.616 17 -2.616 18 -2.616 19 -2.616 10	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[14] Top:top0 AudRecorder:recorder0 addr_f[15] Top:top0 AudRecorder:recorder0 addr_f[15] Top:top0 AudRecorder:recorder0 addr_f[17] Top:top0 AudRecorder:recorder0 addr_f[17] Top:top0 AudRecorder:recorder0 addr_f[17] Top:top0 AudRecorder:recorder0 addr_f[17] Top:top0 AudRecorder:recorder0 addr_f[17] Top:top0 AudRecorder:recorder0 addr_f[17]	Toptobol addr. end. [f.1] Toptobol addr. end. [r.1]	ALD_BCLK ALD	qsys0 altpl_0	sid i jol7 (dk(0) sid i jol7 (.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687 -1.696 -1.696	1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.854 0.846 0.846 0.846 0.849 0.857
52 2 522 Tempton (A. of December 20 and decemb	3 -2.698 4 -2.698 4 -2.627 7 -2.627 7 -2.627 9 -2.622 9 -2.622 1 -2.616 1 -2.616 5 -2.616 8 -2.616 8 -2.616 1 -2.617 1 -	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[1] Top:top0 AudRecorder:recorder0 addr_f[1]	Topt:top0 addr_end_r[11] Topt:top0 addr_end_r[2] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[8]	ALD_BCLK	qsys0 (altpl. 0)	sd 1 si7 clk(0)	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.854 0.846 0.849 0.845 0.841 0.857
	3 -2.698 4 -2.628 4 -2.627 7 -2.627 7 -2.627 9 -2.622 -2.616	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[1] Top:top0 AudRecorder:recorder0 addr_f[1]	Toptobol addr. end. [f.1] Toptobol addr. end. [r.1] Toptobol addr. end. [r.2] Toptobol addr. end. [r.1]	ALD_BCLK ALD	qsys0 altpl_0	sid i jol7 (ak(0) cid i	.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687 -1.696 -1.696 -1.709	1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.9964 0.917 0.854 0.846 0.849 0.845 0.841 0.857 0.8589 0.857 0.857 0.8589
54 -2.512 Top:top0 AudRecorder:recorder0 addr_r[3] Top:top0 addr_end_r[3] AUD_BCLK qsys0 altpl_0 sd1 pll7 dk[0] 0.001 -1.709	3 -2.698 4 -2.698 4 -2.627 5 -2.627 6 -2.627 7 -2.628 9 -2.626 9 -2.628 1 -2.616 4 -2.616 5 -2.616 9 -2.610 9 -2.601 9 -2.601 1 -2.600 9 -2.601	Top:top0 AudRecorder:recorder0 done_f Top:top0 AudRecorder:recorder0 addr_f[7] Top:top0 AudRecorder:recorder0 addr_f[16] Top:top0 AudRecorder:recorder0 addr_f[19] Top:top0 AudRecorder:recorder0 addr_f[9] Top:top0 AudRecorder:recorder0 addr_f[1] Top:top0 AudRecorder:recorder0 addr_f[1]	Topt:top0 addr_end_r[11] Topt:top0 addr_end_r[2] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[7] Topt:top0 addr_end_r[8]	ALD_BCLK ALD	qsys0 (altpl. 0)	sid i jal7 (sk(0) sid i jal7 (.001 .001 .001 .001 .001 .001 .001 .001	-1.690 -1.690 -1.690 -1.690 -1.690 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.709 -1.696 -1.696 -1.687	1.035 1.035 1.035 1.035 1.035 1.035 1.035 0.986 0.994 0.917 0.854 0.846 0.849 0.845 0.841 0.857

55	-2.503	Top:top0 AudRecorder:recorder0 addr_r[6]	TanitanOladde and eff.	AUD_BCLK	acus0 lated 0 lad t lall 7 lall (0)	0.001	-1.709	0.722
56	-2.487		Top:top0 addr_end_r[6]		qsys0 altpll_0 sd1 pll7 dk[0]	0.001		0.722
57	80.502	Top:top0 AudRecorder:recorder0 addr_r[23] Debounce:deb1 neg_r	Top:top0 addr_end_r[23] Top:top0 state_r[1]	AUD_BCLK qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0] qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-1.696 -0.254	2.564
58	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
59	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
60	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
61	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.084	2.176
62	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
63	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.084	2.176
64	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.084	2.176
65	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[7]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
66	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[8]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
67	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[9]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
68	81.060					83.333	-0.084	2.176
		Debounce:deb1 neg_r	Top:top0 addr_end_r[10]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]			
69	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
70	81.060	Debounce:deb1 neg_r	Top:top0 addr_end_r[12]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.084	2.176
71	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.134	2.322
72	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
73	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
74	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.134	2.322
75	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[4]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
76	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[5]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
77	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[6]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
78	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[7]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
79	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[8]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
80								
	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[9]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
81	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[10]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
82	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[11]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
83	81.132	Top:top0 state_r[0]	Top:top0 addr_end_r[12]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.134	2.322
84	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[13]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
85	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[14]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
86	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[15]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
87	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[16]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
88	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[17]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
89	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[18]	qsys0 altpl 0 sd1 pl 7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
90	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[19]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
					qsys0 aitpii_0 sd1 pii/ cik[0] qsys0 altpll 0 sd1 pll7 clk[0]			
91	81.241	Debource:deb1 neg_r	Top:top0 addr_end_r[20]	qsys0 altpll_0 sd1 pll7 dk[0]		83.333	-0.081	1.998
92	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[21]	qsys0 altpll_0 sd1 pll7 dk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
93	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[22]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
94	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[23]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.081	1.998
95	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[24]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	-0.081	1.998
96	81.241	Debounce:deb1 neg_r	Top:top0 addr_end_r[25]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	-0.081	1.998
97	81.268	Top:top0 state_r[2]	Top:top0 addr_end_r[0]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.129	2.181
98	81.268	Top:top0 state_r[2]	Top:top0 addr_end_r[1]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.129	2.181
99	81.268	Top:top0 state_r[2]	Top:top0 addr_end_r[2]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 clk[0]	83.333	0.129	2.181
100	81.268	Top:top0 state_r[2]	Top:top0 addr_end_r[3]	qsys0 altpll_0 sd1 pll7 clk[0]	qsys0 altpll_0 sd1 pll7 dk[0]	83.333	0.129	2.181
	1200mV (OC Model Setup: 'CLOCK_50'		117 1 1 2 1 1 1 1 1	117 1 1 2 1 1 1 1 2 3			
	Slack	From Node	To	Node	Launch Clock Latch Cloc	k Relationship	Clock Skew	Data Delay
	-0.722				AUD_BCLK CLOCK_50	1.000	-0.390	1.309
1 2	-0.722	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe	r:saram wrapper ujadar rj25j				
4			Lab 2 agree gove 0 ICDD AMM/cappe					
		Top:top0 AudRecorder:recorder0 write_r		er:sdram_wrapper_0 addr_r[22]	AUD_BCLK CLOCK_50	1.000	-0.390	1.309
3	-0.722	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe	er:sdram_wrapper_0 addr_r[22] er:sdram_wrapper_0 addr_r[20]	AUD_BCLK CLOCK_50 AUD_BCLK CLOCK_50	1.000 1.000	-0.390 -0.390	1.309 1.309
3 4	-0.722 -0.684	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	er:sdram_wrapper_0 addr_r[22] er:sdram_wrapper_0 addr_r[20] er:sdram_wrapper_0 addr_r[5]	AUD_BCLK CLOCK_50 AUD_BCLK CLOCK_50 AUD_BCLK CLOCK_50	1.000 1.000 1.000	-0.390 -0.390 -0.134	1.309 1.309 1.527
3 4 5	-0.722 -0.684 -0.680	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[1]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	er:sdram_wrapper_0 addr_r[22] er:sdram_wrapper_0 addr_r[20] er:sdram_wrapper_0 addr_r[5] er:sdram_wrapper_0 addr_r[1]	AUD_BCLK	1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139	1.309 1.309 1.527 1.518
3 4 5 6	-0.722 -0.684 -0.680 -0.661	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[9]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	er:sdram_wrapper_0 addr_r[22] er:sdram_wrapper_0 addr_r[20] er:sdram_wrapper_0 addr_r[5] er:sdram_wrapper_0 addr_r[1] er:sdram_wrapper_0 addr_r[9]	AUD_BCLK	1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134	1.309 1.309 1.527 1.518 1.504
3 4 5 6 7	-0.722 -0.684 -0.680 -0.661 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	er:sdram_wrapper_0 addr_r[22] er:sdram_wrapper_0 addr_r[20] er:sdram_wrapper_0 addr_r[5] er:sdram_wrapper_0 addr_r[1] er:sdram_wrapper_0 addr_r[9] er:sdram_wrapper_0 data_r[15]	AUD_BCLK CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363	1.309 1.309 1.527 1.518 1.504 1.264
3 4 5 6 7 8	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	rr:sdram_wrapper_0 addr_r[22] rr:sdram_wrapper_0 addr_r[20] rr:sdram_wrapper_0 addr_r[5] rr:sdram_wrapper_0 addr_r[1] rr:sdram_wrapper_0 addr_r[1] rr:sdram_wrapper_0 addr_r[15] rr:sdram_wrapper_0 data_r[15]	AUD_BCLK	1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363	1.309 1.309 1.527 1.518 1.504 1.264 1.264
3 4 5 6 7 8 9	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	er:sdram_wrapper_0 addr_r[22] er:sdram_wrapper_0 addr_r[20] er:sdram_wrapper_0 addr_r[5] er:sdram_wrapper_0 addr_r[1] er:sdram_wrapper_0 addr_r[9] er:sdram_wrapper_0 data_r[13] er:sdram_wrapper_0 data_r[14] er:sdram_wrapper_0 data_r[14]	AUD_BCLK	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363	1,309 1,309 1,527 1,518 1,504 1,264 1,264 1,264
3 4 5 6 7 8 9	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	erisdram_wrapper_0 addr_r[22] erisdram_wrapper_0 addr_r[20] erisdram_wrapper_0 addr_r[2] erisdram_wrapper_0 addr_r[1] erisdram_wrapper_0 addr_r[1] erisdram_wrapper_0 data_r[13] erisdram_wrapper_0 data_r[14] erisdram_wrapper_0 data_r[14] erisdram_wrapper_0 data_r[13]	AUD_BCLK	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363	1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264
3 4 5 6 7 8 9 10	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	ersdram_wrapper_0 addr_r[22] ersdram_wrapper_0 addr_r[20] ersdram_wrapper_0 addr_r[3] ersdram_wrapper_0 addr_r[1] ersdram_wrapper_0 addr_r[1] ersdram_wrapper_0 datdr_r[1] ersdram_wrapper_0 data_r[1] ersdram_wrapper_0 data_r[1] ersdram_wrapper_0 data_r[1] ersdram_wrapper_0 data_r[1]	AUD_BCIK CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363	1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264
3 4 5 6 7 8 9 10 11	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAWrappe Lab3_qsys:qsys0 SDRAWrappe	ersdram, wrapper_0 addr_f[22] ersdram, wrapper_0 addr_f[20] ersdram, wrapper_0 addr_f[3] ersdram, wrapper_0 addr_f[1] ersdram, wrapper_0 addr_f[1] ersdram, wrapper_0 addr_f[1] ersdram, wrapper_0 data_f[15] ersdram, wrapper_0 data_f[17]	AUD_BGLK CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363	1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264
3 4 5 6 7 8 9 10 11 12 13	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0 SDRAMWirappe	ersdram_wrapper_0 addr_[72] ersdram_wrapper_0 addr_[72] ersdram_wrapper_0 addr_[7] ersdram_wrapper_0 addr_[7] ersdram_wrapper_0 addr_[7] ersdram_wrapper_0 daddr_[7] ersdram_wrapper_0 data_[14] ersdram_wrapper_0 data_[14] ersdram_wrapper_0 data_[14] ersdram_wrapper_0 data_[17] ersdram_wrapper_0 data_[17] ersdram_wrapper_0 data_[17] ersdram_wrapper_0 data_[17] ersdram_wrapper_0 data_[17] ersdram_wrapper_0 data_[17]	AUD_BCIK CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363	1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264
3 4 5 6 7 8 9 10 11 12 13 14	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0[addr_r[5] Top:top0]AudRecorder:recorder0[addr_r[1] Top:top0]AudRecorder:recorder0[addr_r[9] Top:top0]AudRecorder:recorder0[write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	ersdram_wrapper_0 addr_r[22] ersdram_wrapper_0 addr_r[20] ersdram_wrapper_0 addr_r[7] ersdram_wrapper_0 addr_r[1] ersdram_wrapper_0 addr_r[9] ersdram_wrapper_0 data_r[1] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[13] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[19] ersdram_wrapper_0 data_r[19] ersdram_wrapper_0 data_r[19] ersdram_wrapper_0 data_r[19] ersdram_wrapper_0 data_r[18]	AUD_BCIK CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363	1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264
3 4 5 6 7 8 9 10 11 12 13 14 15	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	er sadram, wrapper_0 addr_[720] er sadram, wrapper_0 addr_[720] er sadram, wrapper_0 addr_[720] er sadram, wrapper_0 addr_[72] er sadram, wrapper_0 addr_[72] er sadram, wrapper_0 dadar_[13] er sadram, wrapper_0 dadar_[14] er sadram, wrapper_0 dadar_[14] er sadram, wrapper_0 dadar_[14] er sadram, wrapper_0 dadar_[12] er sadram, wrapper_0 dadar_[16] er sadram, wrapper_0 dadar_[18] er sadram, wrapper_0 dadar_[18] er sadram, wrapper_0 dadar_[18]	AUD_BGLK CLOCK_50	1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363	1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264
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3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[9] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAWWrappe Lab3_qsys:qsys0 SDRAWWrappe	arrsdram_wrapper_0 addr_f[22] arrsdram_wrapper_0 addr_f[20] arrsdram_wrapper_0 addr_f[2] arrsdram_wrapper_0 addr_f[1] arrsdram_wrapper_0 addr_f[1] arrsdram_wrapper_0 addr_f[1] arrsdram_wrapper_0 data_f[12]	AUD_BGLK CLOCK_50	1.000 1.000	-0.390 -0.390 -0.134 -0.139 -0.134 -0.363 -0	1.309 1.309 1.527 1.518 1.504 1.264 1.213 1.213 1.213
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r	Lab3_qsysrqsys0 (SDRAMWrappe Lab3_qsysrqsys0 (SDRAMWrappe	arradram_wrapper_0 addr_r[22] srsdram_wrapper_0 addr_r[20] srsdram_wrapper_0 addr_r[1] srsdram_wrapper_0 addr_r[1] srsdram_wrapper_0 addr_r[1] srsdram_wrapper_0 data_r[14] srsdram_wrapper_0 data_r[14] srsdram_wrapper_0 data_r[14] srsdram_wrapper_0 data_r[14] srsdram_wrapper_0 data_r[14] srsdram_wrapper_0 data_r[12] srsdram_wrapper_0 data_r[17] srsdram_wrapper_0 data_r[17] srsdram_wrapper_0 data_r[17] srsdram_wrapper_0 data_r[17] srsdram_wrapper_0 data_r[17] srsdram_wrapper_0 datdr_r[17] srsdram_wrapper_0 datdr_r[17]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.191 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363	1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.660 -0.626 -0.626 -0.626	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	ersdram_wrapper_0 addr_r[22] ersdram_wrapper_0 addr_r[20] ersdram_wrapper_0 addr_r[2] ersdram_wrapper_0 addr_r[3] ersdram_wrapper_0 addr_r[1] ersdram_wrapper_0 addr_r[3] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[14] ersdram_wrapper_0 data_r[16] ersdram_wrapper_0 data_r[16] ersdram_wrapper_0 data_r[8] ersdram_wrapper_0 datdr_r[25] ersdram_wrapper_0 datdr_r[26] ersdram_wrapper_0 datdr_r[27] ersdram_wrapper_0 datdr_r[27]	AUD_BCIK CLOCK_50	1.000 1.000	0.390 0.390 0.134 0.134 0.139 0.134 0.363	1.309 1.309 1.309 1.527 1.528 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.213
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	-0.722 -0.684 -0.680 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626	Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]addr_r[5] Top:top0[AudRecorder:recorder0]addr_r[7] Top:top0]AudRecorder:recorder0]addr_r[9] Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0]AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]write_r Top:top0[AudRecorder:recorder0]ddd_r[7] Top:top0[AudDSP:dsp0]read_r Top:top0[AudDSP:dsp0]ddd_r[7] Top:top0[AudDSP:dsp0]ddd_r[7] Top:top0[AudRecorder:recorder0]ddd_r[7] Top:top0[AudRecorder:recorder0]ddd_r[7]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	arrisdram_wrapper_0 addr_f[22] arrisdram_wrapper_0 addr_f[20] arrisdram_wrapper_0 addr_f[2] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[2]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.190 0.191 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.390 0.128 0.161 0.118	1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.499 1.433
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.620 -0.651 -0.650	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudDSP:dsp0 red_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	ersidram, wrapper_0 addr_[72] ersidram, wrapper_0 addr_[72] ersidram, wrapper_0 addr_[73] ersidram, wrapper_0 addr_[73] ersidram, wrapper_0 addr_[73] ersidram, wrapper_0 data_[73] ersidram, wrapper_0 data_[74] ersidram, wrapper_0 data_[74] ersidram, wrapper_0 data_[74] ersidram, wrapper_0 data_[74] ersidram, wrapper_0 data_[73] ersidram, wrapper_0 data_[74] ersidram, wrapper_0 data_[74] ersidram, wrapper_0 data_[78] ersidram, wrapper_0 addr_[78]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.139 0.134 0.363	1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.413 1.499 1.433 1.470 1.425
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.620 -0.617 -0.617 -0.609 -0.596	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 add_r[5] Top:top0 AudRecorder:recorder0 add_r[7] Top:top0 AudRecorder:recorder0 add_r[7] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 add_r[7] Top:top0 AudRecorder:recorder0 add_r[7] Top:top0 AudRecorder:recorder0 add_r[19] Top:top0 AudRecorder:recorder0 add_r[19] Top:top0 AudRecorder:recorder0 add_r[19] Top:top0 AudRecorder:recorder0 add_r[19] Top:top0 AudRecorder:recorder0 add_r[1]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	arrisdram_wrapper_0 addr_f[22] srisdram_wrapper_0 addr_f[20] srisdram_wrapper_0 addr_f[20] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 data_f[12] srisdram_wrapper_0 addr_f[23] srisdram_wrapper_0 addr_f[24] srisdram_wrapper_0 addr_f[24] srisdram_wrapper_0 addr_f[26] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[28]	AUD_BGLK CLOCK_50	1.000 1.000	-0.390 -0.139 -0.134 -0.139 -0.134 -0.134 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.163 -0.390 -0.390 -0.128 -0.161 -0.118 -0.161 -0.128	1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.409 1.433 1.470 1.425
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3 4 5 6 7 8 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.650 -0	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudSP:dsp0 read_r Top:top0 AudSP:dsp0 read_r Top:top0 AudSP:dsp0 read_r Top:top0 AudRecorder:recorder0 addr_r[1]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	ersidram, wrapper_0 addr_[12] ersidram, wrapper_0 addr_[12] ersidram, wrapper_0 addr_[12] ersidram, wrapper_0 addr_[13] ersidram, wrapper_0 addr_[13] ersidram, wrapper_0 data_[14] ersidram, wrapper_0 data_[17] ersidram, wrapper_0 data_[17] ersidram, wrapper_0 data_[18] ersidram, wrapper_0 addr_[18] ersidram, wrapper_0 addr_[17]	AUD_BCIK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.134 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.183	1.309 1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.213 1.409 1.433 1.470 1.425 1.445 1.433 1.447
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 23 24 25	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.620 -0.617 -0.617 -0.617 -0.617 -0.617 -0.617 -0.617 -0.617 -0.618 -0.618 -0.619 -0.650 -0	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[S] Top:top0 AudRecorder:recorder0 addr_r[S] Top:top0 AudRecorder:recorder0 addr_r[S] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[T]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	arrisdram_wrapper_0 addr_f[22] arrisdram_wrapper_0 addr_f[20] arrisdram_wrapper_0 addr_f[20] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[2] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 -0.390 -0.134 -0.139 -0.134 -0.1363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.163 -0.390 -0.128 -0.118 -0.161 -0.128 -0.199 -0.199 -0.198 -0.161 -0.128 -0.199 -0.199 -0.198 -0.161 -0.118 -0.128 -0.134	1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.419 1.421 1.425 1.433 1.470 1.425 1.433 1.447 1.429
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26	-0.722 -0.684 -0.680 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.650 -0.550 -0	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s]	Lab3_qsys:qsys0 (SDRAMWrappe Lab3_qsys:qsys0 (SDRAMWrappe	arradram_wrapper_0 addr_[72] srisdram_wrapper_0 addr_[72] srisdram_wrapper_0 addr_[72] srisdram_wrapper_0 addr_[72] srisdram_wrapper_0 addr_[72] srisdram_wrapper_0 addr_[72] srisdram_wrapper_0 data_[72] srisdram_wrapper_0 data_[72] srisdram_wrapper_0 data_[72] srisdram_wrapper_0 data_[72] srisdram_wrapper_0 data_[72] srisdram_wrapper_0 addr_[72] srisdram_wrapper_0 addr_[73] srisdram_wrapper_0 addr_[74] srisdram_wrapper_0 addr_[74] srisdram_wrapper_0 addr_[74]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128	1.309 1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.413 1.429 1.433 1.447 1.425 1.433 1.447 1.429
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	-0.722 -0.684 -0.680 -0.661 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.620 -0.650 -0.598 -0.598 -0.598 -0.598 -0.598	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 add_r[5] Top:top0 AudRecorder:recorder0 add_r[7] Top:top0 AudRecorder:recorder0 add_r[7] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 addr_r[24] Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[16] Top:top0 AudRecorder:recorder0 addr_r[17]	Lab3_qsys:qsys0 SDRAMWirappe Lab3_qsys:qsys0 SDRAMWirappe	arrisdram_wrapper_0 addr_f[22] srisdram_wrapper_0 addr_f[20] srisdram_wrapper_0 addr_f[20] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 data_f[12] srisdram_wrapper_0 data_f[12] srisdram_wrapper_0 data_f[12] srisdram_wrapper_0 data_f[12] srisdram_wrapper_0 data_f[12] srisdram_wrapper_0 addr_f[12] srisdram_wrapper_0 addr_f[23] srisdram_wrapper_0 addr_f[24] srisdram_wrapper_0 addr_f[25] srisdram_wrapper_0 addr_f[26] srisdram_wrapper_0 addr_f[27] srisdram_wrapper_0 addr_f[16] srisdram_wrapper_0 addr_f[16] srisdram_wrapper_0 addr_f[16] srisdram_wrapper_0 addr_f[16] srisdram_wrapper_0 addr_f[16]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.134 0.134 0.134 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.163 0.161 0.118 0.118 0.118 0.118 0.119 0.118 0.119 0.118	1.309 1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.433 1.470 1.425 1.445 1.433 1.470 1.429 1.433
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28	-0.722 -0.684 -0.680 -0.660 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.620 -0.650 -0.556 -0	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 Aud	Lab3_qsystqsys0 (SDRAMWrappe Lab3_qsystqsys0 (SDRAMWrappe	arrisdram, wrapper_0 addr_f[22] arrisdram_wrapper_0 addr_f[20] arrisdram_wrapper_0 addr_f[2] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[19] arrisdram_wrapper_0 data_f[19] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 data_f[18] arrisdram_wrapper_0 datdr_f[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 -0.190 -0.193 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.390 -0.390 -0.128 -0.161 -0.118 -0.161 -0.128 -0.139 -0.118 -0.118 -0.119 -0.118 -0.124 -0.124 -0.124 -0.134 -0.147	1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.213 1.419 1.425 1.433 1.447 1.425 1.433 1.447 1.429 1.436 1.414
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20	-0.722 -0.684 -0.680 -0.660 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.620 -0.611 -0.595 -0.595 -0.595 -0.595 -0.595 -0.588 -0.588 -0.588 -0.583 -0.595 -0.583 -0.595 -0.583 -0.555	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[15] Top:top0 AudRecorder:recorder0 addr_r[15] Top:top0 AudRecorder:recorder0 addr_r[22] Top:top0 AudRecorder:recorder0 addr_r[22] Top:top0 AudRecorder:recorder0 addr_r[22]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	arrisdram, wrapper_0 addr_[123] **risdram_wrapper_0 addr_[120] **risdram_wrapper_0 addr_[120] **risdram_wrapper_0 addr_[12] **risdram_wrapper_0 addr_[12] **risdram_wrapper_0 addr_[12] **risdram_wrapper_0 data_[13] **risdram_wrapper_0 data_[14] **risdram_wrapper_0 data_[14] **risdram_wrapper_0 data_[14] **risdram_wrapper_0 data_[12] **risdram_wrapper_0 data_[13] **risdram_wrapper_0 data_[13] **risdram_wrapper_0 addr_[120] **risdram_wrapper_0 addr_[13] **risdram_wrapper_0 addr_[13] **risdram_wrapper_0 addr_[13] **risdram_wrapper_0 addr_[13] **risdram_wrapper_0 addr_[16] **risdram_wrapper_0 addr_[16] **risdram_wrapper_0 addr_[17]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.1083 0.1083 0.1081 0.118 0.161 0.128 0.118 0.118 0.134 0.124 0.134 0.124	1.309 1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.419 1.433 1.449 1.425 1.445 1.433 1.447 1.429 1.436 1.414 1.388
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 30 30 30 30 30 30 30 30 30 30 30 30	0.722 0.684 0.661 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.626 0.620 0.620 0.620 0.690 0.595 0.595 0.598 0.598 0.598 0.598 0.598 0.597 0.598	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[19] Top:top0 AudRecorder:recorder0 addr_r[11] Top:top0 AudRecorder:recorder0 addr_r[12] Top:top0 AudRecorder:recorder0 addr_r[13] Top:top0 AudRecorder:recorder0 addr_r[23] Top:top0 AudRecorder:recorder0 addr_r[23] Top:top0 AudRecorder:recorder0 addr_r[23]	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe	arrisdram_wrapper_0 addr_f[22] arrisdram_wrapper_0 addr_f[20] arrisdram_wrapper_0 addr_f[20] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 addr_f[1] arrisdram_wrapper_0 data_f[12] arrisdram_wrapper_0 data_f[12] arrisdram_wrapper_0 data_f[12] arrisdram_wrapper_0 data_f[12] arrisdram_wrapper_0 data_f[12] arrisdram_wrapper_0 data_f[12] arrisdram_wrapper_0 addr_f[23] arrisdram_wrapper_0 addr_f[24] arrisdram_wrapper_0 addr_f[25] arrisdram_wrapper_0 addr_f[26] arrisdram_wrapper_0 addr_f[27]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.390 0.128 0.161 0.118 0.161 0.128 0.134 0.124 0.134 0.147	1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.413 1.425 1.433 1.470 1.425 1.433 1.447 1.429 1.436 1.436 1.441 1.388 1.408
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 30 31 31 31 31 31 31 31 31 31 31 31 31 31	-0.722 -0.694 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.650 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.626 -0.627 -0.630 -0.530 -0	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudSP:ddpp read_r Top:top0 AudSP:ddpp read_r Top:top0 AudSP:ddpp addr_r[24] Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 AudRecorder:recorder0 addr_r[17] Top:top0 AudRecorder:recorder0 addr_r[18] Top:top0 AudRecorder:recorder0 addr_r[19]	Lab3_qsystqsys0 (SDRAMWrappe Lab3_qsystqsys0 (SDRAMWrappe	arrisdram, wrapper_Oladdr_[22] srisdram_wrapper_Oladdr_[20] srisdram_wrapper_Oladdr_[20] srisdram_wrapper_Oladdr_[1] srisdram_wrapper_Oladdr_[1] srisdram_wrapper_Oladdr_[1] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[15] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 -0.390 -0.194 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.128 -0.118 -0.161 -0.128 -0.139 -0.118 -0.151 -0.118 -0.124 -0.134 -0.124 -0.134 -0.124 -0.139	1.309 1.309 1.309 1.309 1.507 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.263 1.213 1.213 1.213 1.433 1.447 1.425 1.433 1.447 1.425 1.436 1.436 1.436 1.436 1.436 1.436 1.436 1.436 1.436
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 31 31 31 31 31 31 31 31 31 31 31 31	-0.722 -0.680 -0.661 -0.650 -0	Top:top0 AudRecorder:recorder) Artie_r Top:top0 AudRecorder:recorder) Add_r[5] Top:top0 AudRecorder:recorder) Add_r[7] Top:top0 AudRecorder:recorder) Add_r[7] Top:top0 AudRecorder:recorder) Add_r[7] Top:top0 AudRecorder:recorder0 Artie_r Top:top0 AudRe	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe La	arrisdram_wrapper_0 addr_f[22] srisdram_wrapper_0 addr_f[20] srisdram_wrapper_0 addr_f[20] srisdram_wrapper_0 addr_f[1] srisdram_wrapper_0 addr_f[2] srisdram_wrapper_0 addr_f[2] srisdram_wrapper_0 addr_f[2]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.134 0.134 0.1363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.180 0.181 0.181 0.181 0.181 0.181 0.181 0.181 0.184 0.193 0.184 0.194	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.213 1.413 1.425 1.445 1.445 1.433 1.447 1.429 1.436 1.414 1.388 1.408 1.364 1.390 1.369
3 4 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 31 32 33 33 33 33 34 34 35 36 36 36 37 38 38 38 38 38 38 38 38 38 38 38 38 38	0.722 0.684 0.661 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.626 0.626 0.626 0.626 0.626 0.628 0.628 0.630 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.626 0.626 0.626 0.626 0.627 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.650 0.626 0.626 0.627 0.650 0.556 0.556 0.556 0.556 0.556 0.557 0.555	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[5] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[7] Top:top0 AudRecorder:recorder0 addr_r[1] Top:top0 AudRecorder:recorder0 addr_r[2] Top:top0 AudRecorder:recorder0 AudRec	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe La	arrisdram_wrapper_Oladdr_[22] arrisdram_wrapper_Oladdr_[22] arrisdram_wrapper_Oladdr_[23] arrisdram_wrapper_Oladdr_[13] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[15] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[17]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.199 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.139 0.139 0.139 0.128 0.139 0.139 0.134 0.124 0.124 0.124 0.124 0.124 0.124 0.124 0.139 0.139	1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.419 1.421 1.433 1.470 1.425 1.443 1.447 1.429 1.436 1.436 1.436 1.438 1.408 1.388 1.408 1.364 1.390 1.369 1.166
3 4 5 6 7 8 9 10 111 12 13 144 15 16 17 18 19 20 21 22 23 224 25 6 27 28 29 30 31 32 33 33 34	-0.722 -0.684 -0.669 -0.661 -0.650 -0	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudDSP:dsp0 ead_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_q	arrisdram, wrapper_Oladdr_[12] srisdram_wrapper_Oladdr_[12] srisdram_wrapper_Oladdr_[13] srisdram_wrapper_Oladdr_[13] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[15] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.10363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.139 0.118 0.161 0.128 0.134 0.124 0.134 0.124 0.134 0.124 0.166 0.199 0.166	1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.263 1.213 1.213 1.213 1.419 1.425 1.433 1.447 1.425 1.433 1.447 1.429 1.436 1.414 1.388 1.408 1.364 1.390 1.399 1.166
3 4 5 6 7 8 9 10 111 12 13 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35	-0.722 -0.680 -0.661 -0.650 -0	Top:top0 AudRecorder:recorder) avite_r Top:top0 AudRecorder:recorder) add_r[5] Top:top0 AudRecorder:recorder) add_r[7] Top:top0 AudRecorder:recorder) add_r[7] Top:top0 AudRecorder:recorder) avite_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 addr_r[24] Top:top0 AudSP:dsp0 Audr_r[15] Top:top0 AudRecorder:recorder0 Audr_r[15] Top:top0 AudRecorder:recorder0 Audr_r[15] Top:top0 AudRecorder:recorder0 Audr_r[16] Top:top0 AudRecorder:recorder0 Audr_r[17] Top:top0 AudRecorder:recorder0 Audr_r[18] Top:top0 AudRecorder:recorder0 Audr_r	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe Lab3_q	arrisdram, wrapper_0 addr_[22] stradram_wrapper_0 addr_[28] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[19] stradram_wrapper_0 data_r[19] stradram_wrapper_0 data_r[19] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 data_r[18] stradram_wrapper_0 datdr_[17] stradram_wrapper_0 datdr_[17] stradram_wrapper_0 datdr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.390 0.128 0.161 0.118 0.161 0.128 0.191 0.118 0.114 0.124 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.139 0.166	1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.409 1.413 1.470 1.425 1.445 1.433 1.447 1.429 1.436 1.441 1.388 1.364 1.390 1.369 1.166 1.166
3 4 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 21 22 23 24 5 26 27 28 29 30 31 32 33 34 35 36	-0.722 -0.684 -0.680 -0.661 -0.650 -0.550 -0.550 -0.550 -0.550 -0.550	Top:top0 AudRecorder-recorder0 write_r Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 write_r Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder-sod	Lab3_qsystqsys0 SDRAMWrappe Lab3_qsystqsys0 SDRAMWrappe Lab4_qsystqsys0 SDRAMWrappe Lab4_q	arrisdram, wrapper_Oladdr_[12] srisdram_wrapper_Oladdr_[12] srisdram_wrapper_Oladdr_[13] srisdram_wrapper_Oladdr_[13] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 -0.194 -0.193 -0.134 -0.139 -0.134 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.363 -0.390 -0.128 -0.161 -0.118 -0.161 -0.128 -0.139 -0.139 -0.124 -0.147 -0.124 -0.147 -0.124 -0.166 -0.139 -0.160 -0.363 -0.363 -0.363	1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.213 1.413 1.419 1.425 1.433 1.447 1.425 1.433 1.447 1.429 1.436 1.438 1.408 1.364 1.390 1.369 1.166 1.166
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 33 34 35 36 36 37	-0.722 -0.680 -0.660 -0.660 -0.650 -0.550 -0.550 -0.550 -0.552 -0.552	Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder0 AudRecorder:recorder0 AudRecorder:recorder0 AudRecorder:recorder0 AudRecorder:recorder0 AudRecorder:recorder0 AudRecor	Lab3_qsys:qsys0 SDRAMWrappe Lab3_qsys:qsys0 SDRAMWrappe La	arrisdram, wrapper_Oladdr_[22] arrisdram_wrapper_Oladdr_[28] arrisdram_wrapper_Oladdr_[27] arrisdram_wrapper_Oladdr_[18] arrisdram_wrapper_Oladdr_[19] arrisdram_wrapper_Oladdr_[19] arrisdram_wrapper_Oladdr_[19] arrisdram_wrapper_Oladdr_[19] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.134 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.181 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.128 0.161 0.166 0.139 0.166 0.134 0.166 0.134 0.166 0.139 0.166 0.166 0.139 0.166 0.166 0.166 0.166 0.166 0.166 0.166 0.166 0.166 0.166	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.419 1.425 1.445 1.445 1.445 1.445 1.447 1.429 1.436 1.414 1.388 1.408 1.364 1.390 1.369 1.166 1.166 1.166
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3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 31 33 33 34 34 35 36 36 37 38 38 39 39 30 30 30 30 30 30 30 30 30 30 30 30 30	-0.722 -0.684 -0.680 -0.661 -0.650 -0.550 -0	Top:top0 AudRecorder-recorder0 write_r Top:top0 AudRecorder-recorder0 addr_r[1] Top:top0 AudRecorder-recorder0 addr_r[1] Top:top0 AudRecorder-recorder0 addr_r[1] Top:top0 AudRecorder-recorder0 addr_r[1] Top:top0 AudRecorder-recorder0 write_r Top:top0 AudRecorder-recorder0 addr_r[1] Top:top0 AudRecorder-recorder0 addr_r[2] Top:top0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recorder0 AudRecorder-recordero-Recorder-Recorder-Recorder-Recorder-Recorder-Recorder-Recorder-	Lab3_qsysrqsys0 SDRAMWrappe Lab3_qsysrqsys0 SDRAMWrappe Lab3_q	arrisdram_wrapper_Oladdr_[122] arrisdram_wrapper_Oladdr_[120] arrisdram_wrapper_Oladdr_[120] arrisdram_wrapper_Oladdr_[13] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[15] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[18] arrisdram_wrapper_Oladdr_[18] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.190 0.191 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.139 0.134 0.124 0.124 0.124 0.124 0.124 0.124 0.134 0.166 0.139 0.166 0.139 0.166	1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.413 1.421 1.433 1.447 1.425 1.433 1.447 1.429 1.438 1.408 1.308 1.408 1.309 1.166 1.166 1.166 1.166 1.166 1.166 1.166
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3 4 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 21 22 3 24 5 26 27 30 31 32 33 33 34 35 36 37 38 39 40 41 42 43 44 45 6	-0.722 -0.684 -0.680 -0.661 -0.650 -0.550 -0.550 -0.550 -0.550 -0.550 -0.550 -0.550 -0.551 -0.551 -0.551 -0.551	Top:top0 AudRecorder-recorder0 write_r Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recorder0 write_r Top:top0 AudRecorder-recorder0 addr_r[s] Top:top0 AudRecorder-recor	Lab3_qsysrqsys0 SDRAMWrappe Lab3_qsysrqsys0 SDRAMWrappe Lab3_q	arrisdram_wrapper_Oladdr_[22] arrisdram_wrapper_Oladdr_[23] arrisdram_wrapper_Oladdr_[24] arrisdram_wrapper_Oladdr_[15] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.194 0.199 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.139 0.191 0.118 0.161 0.128 0.139 0.191 0.118 0.161 0.124 0.134 0.147 0.124 0.166 0.139 0.363 0.369 0.369 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.213 1.429 1.433 1.447 1.425 1.433 1.447 1.429 1.436 1.166 1.159 1.159 1.159
3 4 5 5 6 7 8 9 10 111 122 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 9 40 41 42 43 44 45 46 47	-0.722 -0.680 -0.660 -0.660 -0.650 -0	Top:top0 AudRecorder:recorder0 ardr [5] Top:top0 AudRecorder:recorder0 addr [6] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 write _r Top:top0 AudRecorder:recorder0 addr _r[7] Top:top0 AudRecorder:recorder0 addr _r[7] Top:top0 AudRecorder:recorder0 addr _r[19] Top:top0 AudRecorder:recorder0 addr _r[19] Top:top0 AudRecorder:recorder0 addr _r[19] Top:top0 AudRecorder:recorder0 addr _r[19] Top:top0 AudRecorder:recorder0 addr _r[1] Top:top0 AudRecorder:recorder0 addr _r[2] Top:top0 AudDSP:ddp0 read _r Top:top0 AudSP:ddp0 read _r Top:top0 AudSP:	Lab3_qsystqsys0 (SDRAMWrappe Lab3_qsystqsys0	arrisdram, wrapper_Oladdr_[12] srisdram_wrapper_Oladdr_[12] srisdram_wrapper_Oladdr_[13] srisdram_wrapper_Oladdr_[13] srisdram_wrapper_Oladdr_[14] srisdram_wrapper_Oladdr_[15] srisdram_wrapper_Oladdr_[15] srisdram_wrapper_Oladdr_[16] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[18] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[17] srisdram_wrapper_Oladdr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 -0.390 -0.194 -0.134 -0.139 -0.134 -0.363 -0.369 -0.369 -0.369 -0.369 -0.369 -0.369 -0.369	1.309 1.309 1.309 1.309 1.309 1.507 1.518 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.263 1.213 1.213 1.213 1.213 1.433 1.447 1.425 1.433 1.447 1.425 1.436 1.169 1.159 1.159 1.159 1.159
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 33 34 35 36 37 38 38 39 39 39 40 40 40 40 40 40 40 40 40 40 40 40 40	-0.722 -0.680 -0.661 -0.650 -0.620 -0.650 -0	Top:top0 AudRecorder:recorder) addr_r[s] Top:top0 AudRecorder:recorder) write_r Top:top0 AudRecorder:recorder0 write_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudDSP:dsp0 read_r Top:top0 AudSSP:dsp0 read_r Top:top0 AudRecorder:recorder0 addr_r[s] Top:top0 AudRecorder:recorder	Lab3_qsysiqsys0 SDRAMWrappe Lab3_qsysiqsys0 SDRAMWrappe Lab3_q	arrisdram_wrapper_0 addr_[22] arrisdram_wrapper_0 addr_[28] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 data_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.194 0.199 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.134 0.161 0.128 0.134 0.161 0.161 0.128 0.134 0.161 0.161 0.161 0.160 0.363 0.369 0.369 0.369 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.504 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.409 1.213 1.413 1.421 1.433 1.470 1.425 1.433 1.447 1.429 1.436 1.444 1.388 1.408 1.364 1.390 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.159 1.159 1.159 1.159
3 4 5 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 8 29 30 31 32 33 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49	-0.722 -0.684 -0.680 -0.661 -0.650 -0.550 -0.550 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551	Top:top0] AudRecorder-recorder0] write _r Top:top0 AudRecorder-recorder0 addr _r[1] Top:top0 AudRecorder-recorder0] addr _r[1] Top:top0 AudRecorder-recorder0] addr _r[1] Top:top0 AudRecorder-recorder0] addr _r[1] Top:top0 AudRecorder-recorder0] write _r Top:top0 AudRecorder-recorder	Lab3_qsystqsys0 SDRAMWrappe Lab3_qsystqsys0 SDRAMWrappe Lab3_q	arrisdram_wrapper_Oladdr_[122] arrisdram_wrapper_Oladdr_[123] arrisdram_wrapper_Oladdr_[13] arrisdram_wrapper_Oladdr_[13] arrisdram_wrapper_Oladdr_[14] arrisdram_wrapper_Oladdr_[15] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[16] arrisdram_wrapper_Oladdr_[17] arrisdram_wrapper_Oladdr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.139 0.118 0.161 0.124 0.124 0.124 0.124 0.134 0.147 0.124 0.166 0.139 0.363 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.413 1.213 1.429 1.433 1.447 1.425 1.433 1.447 1.426 1.308 1.408 1.300 1.366 1.169 1.159
3 4 5 5 6 7 8 9 10 111 122 13 14 15 16 17 18 19 20 21 22 23 23 24 25 6 27 28 29 30 31 32 33 4 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	-0.722 -0.680 -0.660 -0.660 -0.650 -0.550 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551	Top:top0 AudRecorder:recorder0 ardr_[5] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_[7] Top:top0 A	Lab3_qsysiqsys0 (SDRAMWrappe Lab3_qsysiqsys0	arrisdram_wrapper_0 addr_[22] stradram_wrapper_0 addr_[28] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 addr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.134 0.139 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.118 0.128 0.134 0.128 0.199 0.161 0.118 0.134 0.147 0.124 0.166 0.139 0.134 0.160 0.363 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.413 1.429 1.433 1.470 1.425 1.445 1.433 1.470 1.429 1.436 1.66 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.169 1.159
3 4 5 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 21 22 23 24 5 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 5 6 47 48 49 50 51	-0.722 -0.684 -0.680 -0.661 -0.650 -0.550 -0.550 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551	Top:top0] AudRecorder-recorder0] write _r Top:top0 AudRecorder-recorder0 addr _r[1] Top:top0 AudRecorder-recorder0] addr _r[1] Top:top0 AudRecorder-recorder0] addr _r[1] Top:top0 AudRecorder-recorder0] addr _r[1] Top:top0 AudRecorder-recorder0] write _r Top:top0 AudRecorder-recorder	Lab3_qsystqsys0 SDRAMWrappe Lab3_qsystqsys0 SDRAMWrappe Lab3_q	arrisdram_wrapper_0 addr_[22] stradram_wrapper_0 addr_[28] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 addr_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 data_[18] stradram_wrapper_0 addr_[18]	AUD_BGLK CLOCK_50	1.000 1.000	0.390 0.390 0.194 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.128 0.161 0.118 0.161 0.128 0.139 0.118 0.161 0.124 0.124 0.124 0.124 0.134 0.147 0.124 0.166 0.139 0.363 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.413 1.213 1.429 1.433 1.447 1.425 1.433 1.447 1.426 1.308 1.408 1.300 1.366 1.169 1.159
3 4 5 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 1 22 2 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 9 40 14 14 2 43 44 44 45 66 47 48 99 50 51 52	-0.722 -0.680 -0.660 -0.660 -0.650 -0.550 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551 -0.551	Top:top0 AudRecorder:recorder0 ardr_[5] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 addr_[7[3] Top:top0 AudRecorder:recorder0 write_r Top:top0 AudRecorder:recorder0 addr_[7] Top:top0 A	Lab3_qsysiqsys0 (SDRAMWrappe Lab3_qsysiqsys0	arrisdram_wrapper_0 addr_[123] arrisdram_wrapper_0 addr_[120]	AUD_BGLK CLOCK_50 AUD_BGLK CLOC	1.000 1.000	0.390 0.134 0.139 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.118 0.128 0.134 0.128 0.199 0.161 0.118 0.134 0.147 0.124 0.166 0.139 0.134 0.160 0.363 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.413 1.429 1.433 1.470 1.425 1.445 1.433 1.470 1.429 1.436 1.66 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.169 1.159
3 4 5 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51	-0.722 -0.684 -0.680 -0.661 -0.650 -0.550 -0.550 -0.550 -0.550 -0.551	Top:topol AudRecorder recorder 0 lwrite _r Top:topol AudRecorder recorder 0 laddr _r [1] Top:topol AudRecorder recorder 0 lwrite _r Top:topol AudRecorder 0 lwrite _r Top:topol	Lab3_qsysrqsys0 SDRAMWrappe Lab3_qsysrqsys0 SDRAMWrappe Lab3_q	arrisdram, wrapper_Oladdr_[123] arrisdram, wrapper_Oladdr_[120] arrisdram, wrapper_Oladdr_[13] arrisdram, wrapper_Oladdr_[13] arrisdram, wrapper_Oladdr_[14] arrisdram, wrapper_Oladdr_[15] arrisdram, wrapper_Oladdr_[14] arrisdram, wrapper_Oladdr_[16] arrisdram, wrapper_Oladdr_[17] arrisdram, wrapper_Oladdr_[17] arrisdram, wrapper_Oladdr_[18]	AUD_BGLK CLOCK_50 AUD_BGLK CLOC	1.000 1.000	0.390 0.194 0.199 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.390 0.118 0.161 0.118 0.161 0.128 0.134 0.161 0.128 0.134 0.161 0.124 0.161 0.134 0.161 0.166 0.139 0.166 0.134 0.166 0.139 0.166 0.134 0.166 0.139 0.166 0.134 0.166 0.139 0.166 0.134 0.166 0.139 0.166 0.134 0.166 0.139 0.166 0.139 0.166 0.139 0.166 0.160 0.363 0.369	1.309 1.309 1.309 1.309 1.309 1.527 1.518 1.527 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.409 1.425 1.433 1.470 1.425 1.433 1.470 1.425 1.436 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.159
3 4 5 5 6 7 8 9 10 111 12 13 14 15 16 17 18 19 20 1 22 2 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 9 40 14 14 2 43 44 44 45 66 47 48 99 50 51 52	-0.722 -0.684 -0.660 -0.660 -0.650 -0.550 -0.550 -0.551	Top:top0 AudRecorder:recorder0 ardr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 addr [7] Top:top0 AudRecorder:recorder0 write _r Top:top0 AudRecorder:recorder0 addr _r[7] Top:top0 AudRecorder:recorder0 addr _r[7] Top:top0 AudRecorder:recorder0 addr _r[7] Top:top0 AudRecorder:recorder0 addr _r[7] Top:top0 AudRecorder:recorder0 addr _r[1] Top:top0 AudRecorder:recorder0 addr _r[1] Top:top0 AudRecorder:recorder0 addr _r[1] Top:top0 AudRecorder:recorder0 addr _r[2] Top:top0 AudRecorder:recor	Lab3_qsystqsys0 (SDRAMWrappe Lab3_qsystqsys0	arrisdram_wrapper_0 addr_[22] arrisdram_wrapper_0 addr_[28] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 addr_[18] arrisdram_wrapper_0 data_[18]	AUD_BGLK CLOCK_50 AUD_BGLK CLOC	1.000 1.000	0.390 0.390 0.193 0.193 0.134 0.139 0.134 0.139 0.134 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.363 0.181 0.161 0.118 0.161 0.128 0.139 0.118 0.161 0.162 0.139 0.166 0.139 0.166 0.134 0.166 0.139 0.166	1.309 1.309 1.309 1.309 1.309 1.507 1.518 1.524 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.264 1.213 1.213 1.213 1.469 1.433 1.447 1.425 1.433 1.447 1.425 1.436 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.166 1.159

55	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
56	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
57	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
58	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
59	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
60	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
61	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
62	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
63	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
64	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
65	-0.540	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
66	-0.538	Top:top0 AudRecorder:recorder0 addr_r[21]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.129	1.386
67	-0.534	Top:top0 AudDSP:dsp0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.161	1.350
68	-0.525	Top:top0 AudRecorder:recorder0 addr_r[18]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.378
69	-0.525	Top:top0 AudRecorder:recorder0 addr_r[24]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.378
70	-0.517	Top:top0 AudDSP:dsp0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.128	1.366
71	-0.516	Top:top0 AudRecorder:recorder0 addr_r[14]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.369
72	-0.511	Top:top0 AudRecorder:recorder0 addr_r[25]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.147	1.341
73	-0.510	Top:top0 AudRecorder:recorder0 addr_r[0]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.128	1.359
74	-0.509	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
75	-0.509	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
76	-0.509	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
77	-0.509	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
78	-0.509	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
79	-0.509	Top:top0 AudRecorder:recorder0 write_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
80	-0.507	Top:top0 AudRecorder:recorder0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.350
81	-0.504	Top:top0 AudDSP:dsp0 addr_r[10]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.160	1.321
82	-0.492	Top:top0 AudRecorder:recorder0 addr_r[20]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.147	1.322
83	-0.484	Top:top0 AudDSP:dsp0 addr_r[6]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.130	1.331
84	-0.460	Top:top0 AudDSP:dsp0 addr_r[19]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.155	1.282
85	-0.455	Top:top0 AudRecorder:recorder0 addr_r[4]	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.139	1.293
86	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
87	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
88	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
89	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
90	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
91	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
92	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
93	-0.453	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
94	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
95	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
96	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
97	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
98	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
99	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
100	-0.444	Top:top0 AudDSP:dsp0 read_r	Lab3_qsys:qsys0 SDRAMWrapper:sdram_wrapper_0 addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
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	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[0]
3	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[10]
4	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[11]
5	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[12]
6	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[13]
7	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[14]
В	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[15]
9	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[16]
10	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[17]
11	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[18]
12	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[19]
13	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[1]
14	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[20]
15	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[21]
16	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[22]
17	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[23]
18	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[24]
19	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[25]
20	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[26]
21	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[2]
22	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[3]
23	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[4]
24	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[5]
25	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[6]
26	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[7]
27	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[8]
28	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 addr_r[9]
29	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[0]
30	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[1]
31	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 counter_r[2]
32	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 dadrck_p
33	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[0]
34	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[10]
35	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[11]
36	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[12]
37	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[13]
38	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[14]
39	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[15]
40	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[1]
41	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[2]
42	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[3]
43	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[4]
44	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[5]
45	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[6]
46	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[7]
47	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[8]
48	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_nxt_r[9]
49	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[0]
50	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[10]
51	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[11]
52	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[12]
53	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[13]
54	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[14]

55	-1.000	1.000	2,000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[15]
56	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0[AudDSP:dsp0[data_r[1]]
57	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[2]
58	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[3]
59	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[4]
60	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[5]
61	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[6]
62	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[7]
63	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[8]
64	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 data_r[9]
65	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[0]
66	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[10]
67	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[11]
68	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[12]
69	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[13]
70	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[14]
71	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[15]
72	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[1]
73	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[2]
74	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[3]
75	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[4]
76	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[5]
77	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[6]
78	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[7]
79	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 del data r[8]
80	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 del_data_r[9]
81	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 done r
82	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 read r
83	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 state r.S CALC
84	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 state r.S IDLE
85	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 state r.S PAUSE
86	-1.000	1.000	2.000	Min Period	AUD BCLK	Rise	Top:top0 AudDSP:dsp0 state r.S PLAY
87	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_r[0]
88	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_r[1]
89	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_r[2]
90	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 bit_counter_r[3]
91	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data r[0]
92	-1.000	1,000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 data r[10]
93	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 data_[10]
94	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 data_r[11]
95	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 data_r[12]
96	-1.000	1.000	2.000	Min Period	AUD BCLK	Fall	Top:top0 AudPlayer:player0 data_r[15]
96	-1.000	1.000	2.000	Min Period Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[14] Top:top0 AudPlayer:player0 data_r[15]
98	-1.000	1.000	2.000	Min Period Min Period		Fall	Top:top0[AudPlayer:player0[data_r[15]
98					AUD_BCLK	Fall	
	-1.000	1.000	2.000	Min Period	AUD_BCLK		Top:top0 AudPlayer:player0 data_r[2]
100	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0 AudPlayer:player0 data_r[3]

Problem & Solution

- 1. Port is multiple driven
 - a. Check whether there is the same signal with different logic assignment in the always_comb block
- 2. Improper register removal
 - a. Check whether state transition logic or always_ff block is correct
- 3. Timing assignment not met
 - a. Some calculations like the division to implement linear interpolation needed extra clock cycles but did not affect this task
 - b. This may be due to the fact that the calculated quotient (signal increment) does not affect any other registers immediately, only until another LRCLK

Conclusion & Suggestion:

All that said, we had a lot of fun doing this experiment. From the happy debugging time in the start, and starting to look forward to the moment of recording, to the happiness of constantly replaying music in the end.

In addition, we have learned more about using the Qsys library in Quartus II, and we have written our own components to transform the original codebase written for SRAM into one that can work with SDRAM.