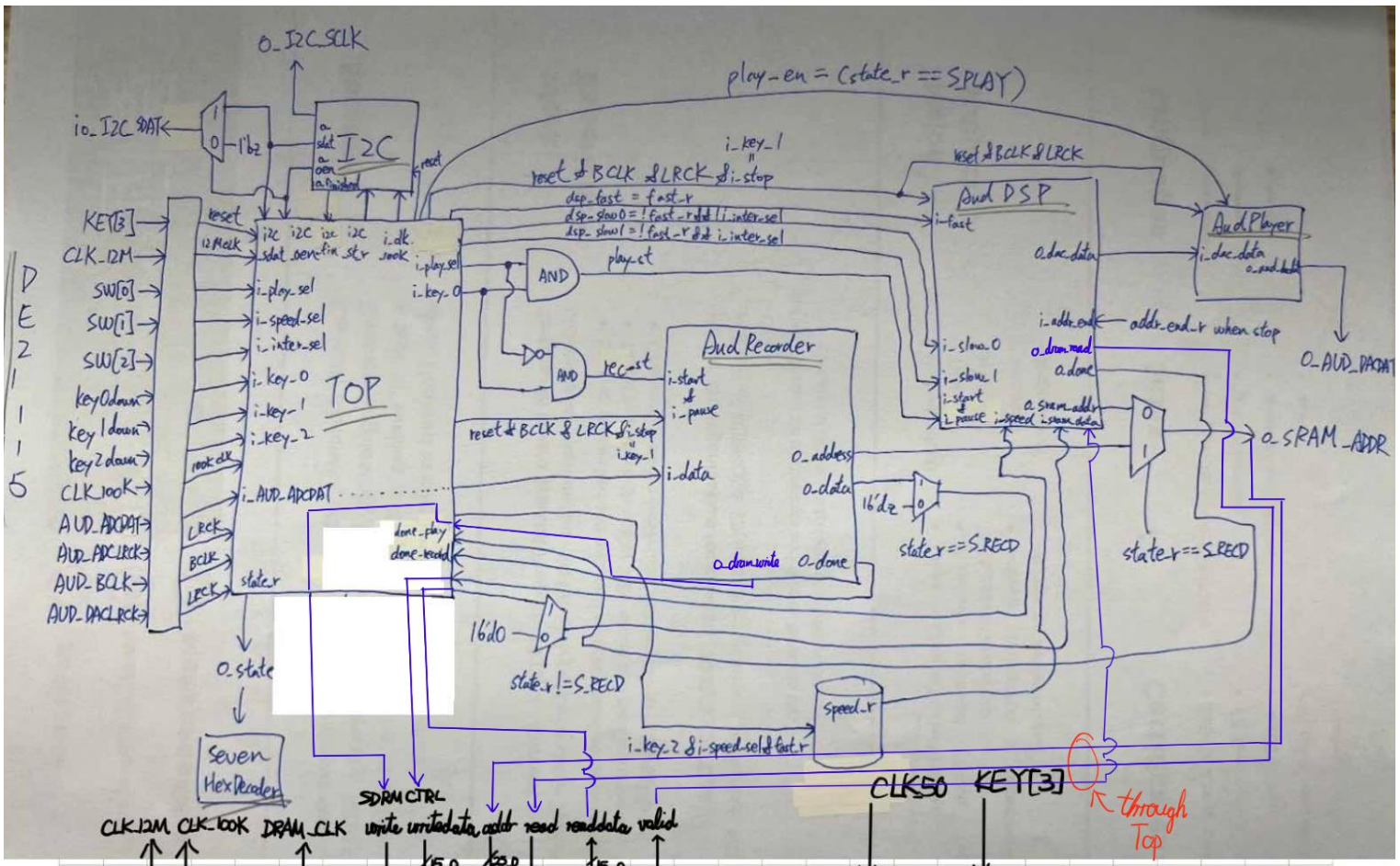
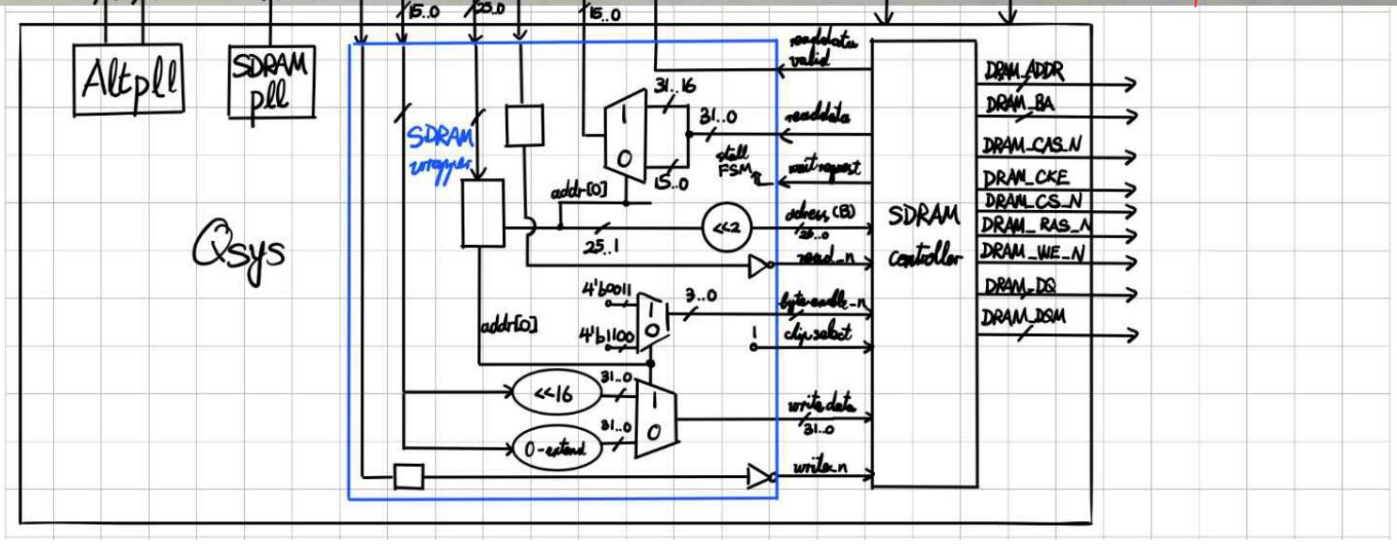
Team09_Lab3_Report

File Structure

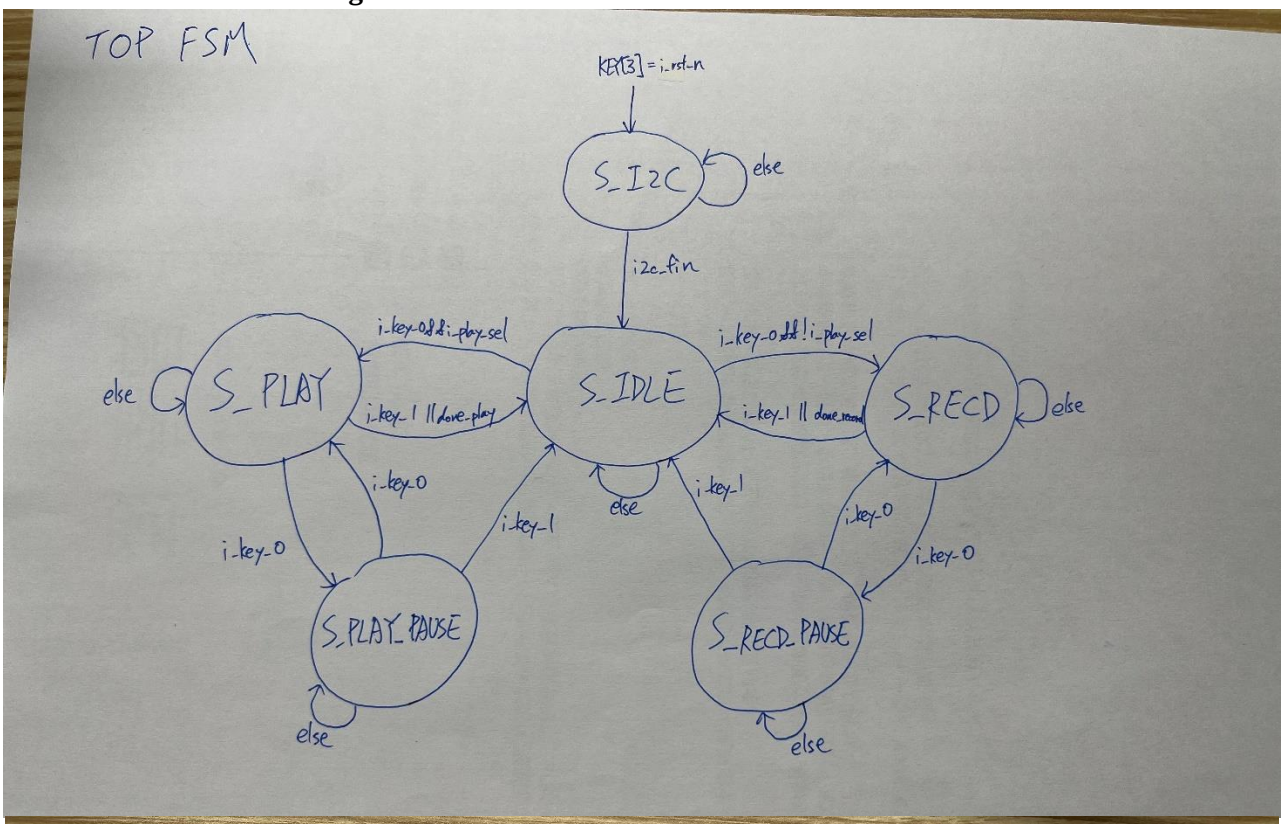
- team09_lab3/team09_lab3_report : This file contains information about the source code in the directory and the instructions of lab3.
- team09_lab3/src : The files at this level are modules that implement the digital recorder.
- team09_lab3/src/DE2_115 : The files in this folder are the DE2_115 related files.
- team09_lab3/src/Altpll/synthesis : The files in this folder are the Qsys generated HDL .qip and .v files.

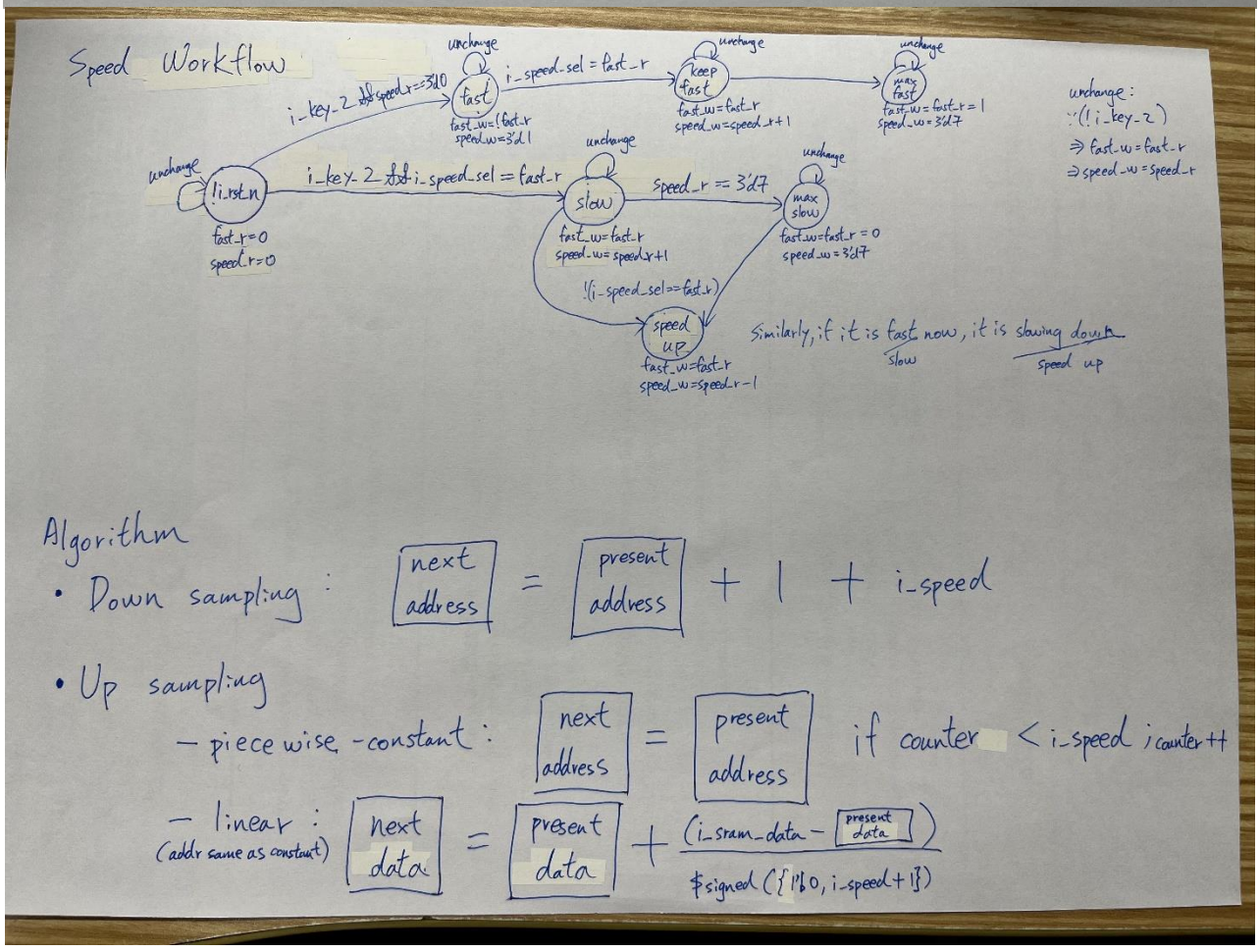
System Architecture





Hardware Scheduling





Bonus

We have implemented storing and loading recorded audio with the onboard SDRAM chip. This is done by utilizing the Qsys components *System and SDRAM Clocks for DE-series Boards* and *SDRAM Controller*.

We have also written our own Avalon Memory Mapped Master component *sdram_wrapper* to better fit the pre-existing codes written for storing and loading with SRAM.

In the end, we have successfully stored and played more than 32 seconds of audio in the SDRAM, with only a few signals and conditions added to the original codebase.

Fitter Summary

Fitter Summary

Fitter Status	Successful - Tue Nov 07 22:16:58 2023
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,530 / 114,480 (1 %)
Total combinational functions	1,298 / 114,480 (1 %)
Dedicated logic registers	724 / 114,480 (< 1 %)
Total registers	843
Total pins	518 / 529 (98 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	2 / 4 (50 %)

Timing Analyzer

Timing Closure Recommendations

Summary [hide details]

This design contains failing setup paths with a worst-case slack of -73.658 ns. Run Report Timing Closure Recomme

Top Failing Paths [hide details]

	Slack	From	To	Recommendations
1	-73.658	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	Report recommendations for this path
2	-73.654	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	Report recommendations for this path
3	-73.652	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	Report recommendations for this path
4	-73.652	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	Report recommendations for this path
5	-73.648	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	Report recommendations for this path

Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-73.658	-1808.155
2	qsys0|altpll_0|sd1|pll7|clk[0]	-6.194	-155.253
3	CLOCK_50	-2.595	-104.802
4	qsys0|altpll_0|sd1|pll7|clk[1]	78.622	0.000

Slow 1200mV 85C Model Minimum Pulse Width Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.210	-215.235
2	CLOCK_50	9.590	0.000
3	qsys0|altpll_0|sd1|pll7|clk[0]	41.373	0.000
4	qsys0|altpll_0|sd1|pll7|clk[1]	4999.706	0.000

Slow 1200mV 85C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-73.658	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.853
2	-73.513	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.708
3	-73.504	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.699
4	-73.341	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.392	76.642
5	-73.316	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.288	76.513
6	-73.264	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.459
7	-73.196	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.392	76.497
8	-73.187	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.392	76.488
9	-73.171	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.288	76.368
10	-73.162	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.288	76.359
11	-73.119	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.314
12	-73.110	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.305
13	-73.013	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.208
14	-72.979	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.311
15	-72.963	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.469	76.341
16	-72.872	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.204
17	-72.868	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.063
18	-72.859	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.054
19	-72.848	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.180
20	-72.834	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.166
21	-72.825	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.157
22	-72.818	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.469	76.196
23	-72.809	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	76.004
24	-72.809	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.469	76.187
25	-72.753	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.085
26	-72.738	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.070
27	-72.727	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.059
28	-72.718	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.050
29	-72.703	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.035
30	-72.694	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	76.026
31	-72.664	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	75.859
32	-72.655	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.286	75.850
33	-72.608	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.940
34	-72.599	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.931
35	-72.593	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.925
36	-72.584	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.916
37	-72.499	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.831
38	-72.449	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.781
39	-72.354	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.686
40	-72.345	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.677
41	-72.304	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.636
42	-72.295	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.627
43	-72.290	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.622
44	-72.186	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.392	75.487
45	-72.145	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.477
46	-72.136	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.423	75.468
47	-72.041	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.392	75.342
48	-72.032	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.392	75.333
49	-47.744	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.898
50	-47.636	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.790
51	-47.620	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	49.108
52	-47.487	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	48.975
53	-47.426	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	48.197
54	-47.423	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.246	48.687

55	-47.398	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.142	48.558
56	-47.350	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.504
57	-47.315	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.246	48.579
58	-47.307	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.075	48.400
59	-47.305	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	48.076
60	-47.303	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.606	48.897
61	-47.290	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.142	48.450
62	-47.278	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.502	48.768
63	-47.269	Top:top0|AudDSP:dsp0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.423
64	-47.259	Top:top0|AudDSP:dsp0|data_r[10]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	48.030
65	-47.242	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.396
66	-47.226	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.500	48.714
67	-47.220	Top:top0|AudDSP:dsp0|data_r[11]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	47.991
68	-47.186	Top:top0|AudDSP:dsp0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.340
69	-47.170	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.606	48.764
70	-47.145	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.502	48.635
71	-47.138	Top:top0|AudDSP:dsp0|data_r[4]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.292
72	-47.128	Top:top0|AudDSP:dsp0|data_r[12]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	47.899
73	-47.120	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	48.608
74	-47.099	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.253
75	-47.093	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.500	48.581
76	-47.090	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.122	47.986
77	-47.088	Top:top0|AudDSP:dsp0|data_r[13]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	47.859
78	-47.061	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	AUD_BCLK	AUD_BCLK	1.000	0.277	48.356
79	-47.050	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	48.538
80	-47.048	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	-0.209	47.857
81	-47.045	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[1]	AUD_BCLK	AUD_BCLK	1.000	0.323	48.386
82	-47.032	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	-0.247	47.803
83	-47.013	Top:top0|AudDSP:dsp0|data_r[14]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.247	47.784
84	-47.004	Top:top0|AudDSP:dsp0|data_r[6]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.158
85	-46.999	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.500	48.487
86	-46.991	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.136	48.145
87	-46.986	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.185	48.189
88	-46.975	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	CLOCK_50	AUD_BCLK	1.000	0.500	48.463
89	-46.969	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.122	47.865
90	-46.961	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.081	48.060
91	-46.954	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[11]	AUD_BCLK	AUD_BCLK	1.000	0.277	48.249
92	-46.953	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	AUD_BCLK	AUD_BCLK	1.000	0.277	48.248
93	-46.948	Top:top0|AudDSP:dsp0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.246	48.212
94	-46.941	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	CLOCK_50	AUD_BCLK	1.000	0.637	48.566
95	-46.937	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	AUD_BCLK	AUD_BCLK	1.000	0.323	48.278
96	-46.930	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[12]	AUD_BCLK	AUD_BCLK	1.000	0.277	48.225
97	-46.927	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	-0.209	47.736
98	-46.925	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	CLOCK_50	AUD_BCLK	1.000	0.683	48.596
99	-46.923	Top:top0|AudDSP:dsp0|data_r[10]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.122	47.819
100	-46.923	Top:top0|AudDSP:dsp0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.142	48.083

Slow 1200mV 85C Model Setup: 'qsys0|altpll_0|sd1|pll7|clk[0]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-6.194	Top:top0|AudDSP:dsp0|done_r	Top:top0|state_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.683	2.450
2	-6.026	Top:top0|AudRecorder:recorder0|done_r	Top:top0|state_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.646	2.319
3	-5.997	Top:top0|AudRecorder:recorder0|done_r	Top:top0|state_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.641	2.295
4	-5.904	Top:top0|AudDSP:dsp0|done_r	Top:top0|state_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.678	2.165
5	-5.529	Top:top0|AudRecorder:recorder0|addr_r[20]	Top:top0|addr_end_r[20]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	2.227
6	-5.515	Top:top0|AudRecorder:recorder0|addr_r[4]	Top:top0|addr_end_r[4]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	2.183
7	-5.432	Top:top0|AudRecorder:recorder0|addr_r[11]	Top:top0|addr_end_r[11]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	2.100
8	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
9	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
10	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
11	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[3]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
12	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[4]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
13	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[5]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
14	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[6]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
15	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[7]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
16	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[8]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
17	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[9]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
18	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[10]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
19	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[11]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
20	-5.408	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[12]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.251	2.096
21	-5.305	Top:top0|AudRecorder:recorder0|addr_r[7]	Top:top0|addr_end_r[7]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.973
22	-5.204	Top:top0|AudRecorder:recorder0|addr_r[16]	Top:top0|addr_end_r[16]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.902
23	-5.151	Top:top0|AudRecorder:recorder0|addr_r[10]	Top:top0|addr_end_r[10]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.819
24	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[13]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
25	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[14]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
26	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[15]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
27	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[16]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
28	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[17]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
29	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[18]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
30	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[19]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
31	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[20]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
32	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[21]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
33	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[22]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
34	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[23]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
35	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[24]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
36	-5.090	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[25]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.249	1.780
37	-5.047	Top:top0|AudRecorder:recorder0|addr_r[9]	Top:top0|addr_end_r[9]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.715
38	-5.036	Top:top0|AudRecorder:recorder0|addr_r[8]	Top:top0|addr_end_r[8]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.704
39	-5.035	Top:top0|AudRecorder:recorder0|addr_r[2]	Top:top0|addr_end_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.703
40	-5.033	Top:top0|AudRecorder:recorder0|addr_r[0]	Top:top0|addr_end_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.701
41	-5.027	Top:top0|AudRecorder:recorder0|addr_r[5]	Top:top0|addr_end_r[5]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.695
42	-5.027	Top:top0|AudRecorder:recorder0|addr_r[21]	Top:top0|addr_end_r[21]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.725
43	-5.014	Top:top0|AudRecorder:recorder0|addr_r[19]	Top:top0|addr_end_r[19]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.712
44	-5.013	Top:top0|AudRecorder:recorder0|addr_r[14]	Top:top0|addr_end_r[14]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.711
45	-5.012	Top:top0|AudRecorder:recorder0|addr_r[24]	Top:top0|addr_end_r[24]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.710
46	-5.007	Top:top0|AudRecorder:recorder0|addr_r[1]	Top:top0|addr_end_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.675
47	-5.002	Top:top0|AudRecorder:recorder0|addr_r[17]	Top:top0|addr_end_r[17]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.700
48	-5.000	Top:top0|AudRecorder:recorder0|addr_r[15]	Top:top0|addr_end_r[15]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.698
49	-4.990	Top:top0|AudRecorder:recorder0|addr_r[25]	Top:top0|addr_end_r[25]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.688
50	-4.979	Top:top0|AudRecorder:recorder0|addr_r[13]	Top:top0|addr_end_r[13]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.677
51	-4.979	Top:top0|AudRecorder:recorder0|addr_r[22]	Top:top0|addr_end_r[22]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.677
52	-4.863	Top:top0|AudRecorder:recorder0|addr_r[12]	Top:top0|addr_end_r[12]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.531
53	-4.832	Top:top0|AudRecorder:recorder0|addr_r[18]	Top:top0|addr_end_r[18]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.530
54	-4.823	Top:top0|AudRecorder:recorder0|addr_r[3]	Top:top0|addr_end_r[3]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.491

55	-4.804	Top:top0|AudRecorder:recorder0|addr_r[6]	Top:top0|addr_end_r[6]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.271	1.472
56	-4.770	Top:top0|AudRecorder:recorder0|addr_r[23]	Top:top0|addr_end_r[23]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.241	1.468
57	77.875	Debounce:deb1|neg_r	Top:top0|state_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.519	4.937
58	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
59	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
60	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
61	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
62	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
63	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
64	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
65	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
66	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
67	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
68	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
69	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
70	78.872	Debounce:deb1|neg_r	Top:top0|addr_end_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.129	4.330
71	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
72	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
73	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
74	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
75	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
76	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
77	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
78	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
79	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
80	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
81	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
82	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
83	78.977	Top:top0|state_r[0]	Top:top0|addr_end_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.315	4.669
84	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
85	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
86	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
87	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[16]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
88	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[17]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
89	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[18]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
90	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[19]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
91	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[20]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
92	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[21]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
93	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[22]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
94	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[23]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
95	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[24]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
96	79.190	Debounce:deb1|neg_r	Top:top0|addr_end_r[25]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.127	4.014
97	79.229	Top:top0|state_r[2]	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.309	4.411
98	79.229	Top:top0|state_r[2]	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.309	4.411
99	79.229	Top:top0|state_r[2]	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.309	4.411
100	79.229	Top:top0|state_r[2]	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.309	4.411

Slow 1200mV 85C Model Setup: 'CLOCK_50'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-2.595	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.966	2.617
2	-2.595	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.966	2.617
3	-2.595	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.966	2.617
4	-2.500	Top:top0|AudRecorder:recorder0|addr_r[1]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.501	2.987
5	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
6	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
7	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
8	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
9	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
10	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
11	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
12	-2.495	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.546
13	-2.487	Top:top0|AudRecorder:recorder0|addr_r[9]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.983
14	-2.451	Top:top0|AudRecorder:recorder0|addr_r[5]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.947
15	-2.406	Top:top0|AudDSP:dsp0|addr_r[24]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.557	2.837
16	-2.390	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.966	2.412
17	-2.390	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.966	2.412
18	-2.390	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.966	2.412
19	-2.383	Top:top0|AudDSP:dsp0|addr_r[16]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.557	2.814
20	-2.360	Top:top0|AudRecorder:recorder0|addr_r[13]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.460	2.888
21	-2.351	Top:top0|AudRecorder:recorder0|addr_r[7]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.488	2.851
22	-2.339	Top:top0|AudRecorder:recorder0|addr_r[19]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.460	2.867
23	-2.337	Top:top0|AudRecorder:recorder0|addr_r[12]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.501	2.824
24	-2.316	Top:top0|AudRecorder:recorder0|addr_r[11]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.488	2.816
25	-2.309	Top:top0|AudDSP:dsp0|addr_r[5]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.490	2.807
26	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
27	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
28	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
29	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
30	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
31	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
32	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
33	-2.306	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.348
34	-2.301	Top:top0|AudRecorder:recorder0|addr_r[16]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.825
35	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
36	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
37	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
38	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
39	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
40	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
41	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
42	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
43	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
44	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
45	-2.296	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.345
46	-2.292	Top:top0|AudRecorder:recorder0|addr_r[3]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.788
47	-2.291	Top:top0|AudDSP:dsp0|addr_r[21]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.566	2.713
48	-2.291	Top:top0|AudDSP:dsp0|addr_r[15]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.553	2.726
49	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
50	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
51	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
52	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
53	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
54	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340

55	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
56	-2.289	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.937	2.340
57	-2.279	Top:top0|AudRecorder:recorder0|addr_r[15]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.460	2.807
58	-2.274	Top:top0|AudDSP:dsp0|addr_r[4]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.565	2.697
59	-2.272	Top:top0|AudRecorder:recorder0|addr_r[8]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.768
60	-2.270	Top:top0|AudRecorder:recorder0|addr_r[2]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.501	2.757
61	-2.269	Top:top0|AudDSP:dsp0|addr_r[9]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.556	2.701
62	-2.265	Top:top0|AudRecorder:recorder0|addr_r[21]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.473	2.780
63	-2.255	Top:top0|AudDSP:dsp0|addr_r[8]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.556	2.687
64	-2.254	Top:top0|AudRecorder:recorder0|addr_r[23]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.778
65	-2.247	Top:top0|AudRecorder:recorder0|addr_r[22]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.491	2.744
66	-2.243	Top:top0|AudRecorder:recorder0|addr_r[17]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.767
67	-2.240	Top:top0|AudDSP:dsp0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.557	2.671
68	-2.235	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
69	-2.235	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
70	-2.235	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
71	-2.235	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
72	-2.235	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
73	-2.235	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.948	2.275
74	-2.222	Top:top0|AudRecorder:recorder0|addr_r[18]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.746
75	-2.220	Top:top0|AudDSP:dsp0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.486	2.722
76	-2.211	Top:top0|AudRecorder:recorder0|addr_r[24]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.735
77	-2.207	Top:top0|AudRecorder:recorder0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.488	2.707
78	-2.197	Top:top0|AudRecorder:recorder0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.464	2.721
79	-2.169	Top:top0|AudDSP:dsp0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.556	2.601
80	-2.151	Top:top0|AudRecorder:recorder0|addr_r[25]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.491	2.648
81	-2.145	Top:top0|AudDSP:dsp0|addr_r[6]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.483	2.650
82	-2.135	Top:top0|AudRecorder:recorder0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.492	2.631
83	-2.104	Top:top0|AudRecorder:recorder0|addr_r[20]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.491	2.601
84	-2.102	Top:top0|AudRecorder:recorder0|addr_r[4]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.501	2.589
85	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
86	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
87	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
88	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
89	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
90	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
91	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
92	-2.100	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.946	2.142
93	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
94	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
95	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
96	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
97	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
98	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
99	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140
100	-2.091	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.939	2.140

Slow 1200mV 85C Model Minimum Pulse Width: 'AUD_BCLK'

	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.210	1.000	4.210	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[0]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[10]
4	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[11]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[12]
6	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[13]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[14]
8	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[15]
9	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[16]
10	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[17]
11	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[18]
12	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[19]
13	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[1]
14	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[20]
15	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[21]
16	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[22]
17	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[23]
18	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[24]
19	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[25]
20	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[26]
21	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[2]
22	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[3]
23	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[4]
24	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[5]
25	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[6]
26	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[7]
27	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[8]
28	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[9]
29	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[0]
30	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[1]
31	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[2]
32	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|daclrck_p
33	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[0]
34	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[10]
35	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[11]
36	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[12]
37	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[13]
38	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[14]
39	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[15]
40	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[1]
41	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[2]
42	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[3]
43	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[4]
44	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[5]
45	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[6]
46	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[7]
47	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[8]
48	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[9]
49	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[0]
50	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[10]
51	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[11]
52	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[12]
53	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[13]
54	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[14]

55	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[15]
56	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[1]
57	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[2]
58	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[3]
59	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[4]
60	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[5]
61	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[6]
62	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[7]
63	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[8]
64	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[9]
65	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[0]
66	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[10]
67	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[11]
68	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[12]
69	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[13]
70	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[14]
71	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[15]
72	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[1]
73	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[2]
74	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[3]
75	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[4]
76	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[5]
77	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[6]
78	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[7]
79	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[8]
80	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[9]
81	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|done_r
82	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|read_r
83	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_CALC
84	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_IDLE
85	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_PAUSE
86	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_PLAY
87	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[0]
88	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[1]
89	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[2]
90	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[3]
91	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[0]
92	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[10]
93	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[11]
94	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[12]
95	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[13]
96	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[14]
97	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[15]
98	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[1]
99	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[2]
100	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[3]

Slow 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-66.398	-1640.870
2	qsys0|altpll_0|sd1|pll7|clk[0]	-5.683	-141.183
3	CLOCK_50	-2.383	-96.510
4	qsys0|altpll_0|sd1|pll7|clk[1]	79.074	0.000

Slow 1200mV 0C Model Minimum Pulse Width Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.210	-215.235
2	CLOCK_50	9.607	0.000
3	qsys0|altpll_0|sd1|pll7|clk[0]	41.360	0.000
4	qsys0|altpll_0|sd1|pll7|clk[1]	4999.709	0.000

Slow 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-66.398	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	69.296
2	-66.275	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	69.173
3	-66.259	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	69.157
4	-66.079	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.087	69.076
5	-66.050	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.948
6	-66.043	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.989	68.942
7	-65.956	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.087	68.953
8	-65.940	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.087	68.937
9	-65.927	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.825
10	-65.920	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.989	68.819
11	-65.911	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.809
12	-65.904	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.989	68.803
13	-65.826	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.724
14	-65.777	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.158	68.845
15	-65.735	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.758
16	-65.703	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.601
17	-65.687	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.585
18	-65.658	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.681
19	-65.654	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.158	68.722
20	-65.648	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.546
21	-65.638	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.158	68.706
22	-65.620	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.643
23	-65.612	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.635
24	-65.596	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.619
25	-65.539	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.562
26	-65.535	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.558
27	-65.525	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.423
28	-65.519	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.542
29	-65.519	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.542
30	-65.509	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.988	68.407
31	-65.497	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.520
32	-65.481	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.504
33	-65.416	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.439
34	-65.400	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.423
35	-65.396	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.419
36	-65.380	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.403
37	-65.330	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.353
38	-65.270	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.293
39	-65.207	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.230
40	-65.191	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.214
41	-65.147	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.170
42	-65.131	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.154
43	-65.129	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.152
44	-65.078	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.087	68.075
45	-65.006	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.029
46	-64.990	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.113	68.013
47	-64.955	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.087	67.952
48	-64.939	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	3.087	67.936
49	-43.021	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	44.168
50	-42.939	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	44.086
51	-42.805	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.559	44.353
52	-42.699	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.230	43.948
53	-42.689	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.559	44.237
54	-42.673	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.820
55	-42.667	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.460
56	-42.663	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.132	43.814
57	-42.637	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.430
58	-42.629	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.071	43.719
59	-42.617	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.230	43.866
60	-42.591	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.738
61	-42.581	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.132	43.732
62	-42.566	Top:top0|AudDSP:dsp0|data_r[11]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.359
63	-42.520	Top:top0|AudDSP:dsp0|data_r[10]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.313
64	-42.518	Top:top0|AudDSP:dsp0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.665
65	-42.497	Top:top0|AudDSP:dsp0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.644
66	-42.486	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.658	44.133
67	-42.457	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.559	44.005
68	-42.451	Top:top0|AudDSP:dsp0|data_r[13]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.244
69	-42.450	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.560	43.999
70	-42.449	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.596
71	-42.406	Top:top0|AudDSP:dsp0|data_r[12]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.199
72	-42.402	Top:top0|AudDSP:dsp0|data_r[4]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.549
73	-42.397	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[1]	AUD_BCLK	AUD_BCLK	1.000	0.301	43.717
74	-42.370	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.658	44.017
75	-42.367	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.514
76	-42.355	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	AUD_BCLK	AUD_BCLK	1.000	0.256	43.630
77	-42.341	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.559	43.889
78	-42.334	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.560	43.883
79	-42.331	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.110	43.240
80	-42.322	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.559	43.870
81	-42.319	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.112
82	-42.315	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	AUD_BCLK	AUD_BCLK	1.000	0.301	43.635
83	-42.307	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.173	43.499
84	-42.307	Top:top0|AudDSP:dsp0|data_r[14]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.100
85	-42.301	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.110	43.210
86	-42.299	Top:top0|AudDSP:dsp0|data_r[15]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.092
87	-42.289	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	-0.226	43.082
88	-42.284	Top:top0|AudDSP:dsp0|data_r[6]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.431
89	-42.281	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.071	43.371
90	-42.280	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	-0.193	43.106
91	-42.278	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[11]	AUD_BCLK	AUD_BCLK	1.000	0.256	43.553
92	-42.273	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	AUD_BCLK	AUD_BCLK	1.000	0.256	43.548
93	-42.271	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.559	43.819
94	-42.271	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.075	43.365
95	-42.271	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[2]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.418
96	-42.250	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	-0.193	43.076
97	-42.246	Top:top0|AudDSP:dsp0|data_r[7]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.128	43.393
98	-42.240	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[12]	AUD_BCLK	AUD_BCLK	1.000	0.256	43.515
99	-42.233	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	CLOCK_50	AUD_BCLK	1.000	0.559	43.781
100	-42.230	Top:top0|AudDSP:dsp0|data_r[11]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.110	43.139

Slow 1200mV 0C Model Setup: 'qsys0|altpll_0|sd1|pll7|clk[0]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-5.683	Top:top0|AudDSP:dsp0|done_r	Top:top0|state_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.333	2.290
2	-5.465	Top:top0|AudRecorder:recorder0|done_r	Top:top0|state_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.289	2.116
3	-5.433	Top:top0|AudRecorder:recorder0|done_r	Top:top0|state_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.293	2.080
4	-5.332	Top:top0|AudDSP:dsp0|done_r	Top:top0|state_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-3.329	1.943
5	-5.067	Top:top0|AudRecorder:recorder0|addr_r[20]	Top:top0|addr_end_r[20]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	2.081
6	-5.051	Top:top0|AudRecorder:recorder0|addr_r[4]	Top:top0|addr_end_r[4]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	2.041
7	-4.936	Top:top0|AudRecorder:recorder0|addr_r[11]	Top:top0|addr_end_r[11]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.926
8	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
9	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
10	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
11	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[3]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
12	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[4]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
13	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[5]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
14	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[6]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
15	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[7]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
16	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[8]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
17	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[9]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
18	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[10]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
19	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[11]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
20	-4.920	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[12]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.932	1.928
21	-4.839	Top:top0|AudRecorder:recorder0|addr_r[7]	Top:top0|addr_end_r[7]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.829
22	-4.753	Top:top0|AudRecorder:recorder0|addr_r[16]	Top:top0|addr_end_r[16]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.767
23	-4.661	Top:top0|AudRecorder:recorder0|addr_r[10]	Top:top0|addr_end_r[10]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.651
24	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[13]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
25	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[14]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
26	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[15]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
27	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[16]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
28	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[17]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
29	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[18]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
30	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[19]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
31	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[20]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
32	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[21]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
33	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[22]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
34	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[23]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
35	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[24]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
36	-4.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[25]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.930	1.626
37	-4.587	Top:top0|AudRecorder:recorder0|addr_r[9]	Top:top0|addr_end_r[9]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.577
38	-4.583	Top:top0|AudRecorder:recorder0|addr_r[21]	Top:top0|addr_end_r[21]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.597
39	-4.582	Top:top0|AudRecorder:recorder0|addr_r[8]	Top:top0|addr_end_r[8]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.572
40	-4.580	Top:top0|AudRecorder:recorder0|addr_r[2]	Top:top0|addr_end_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.570
41	-4.565	Top:top0|AudRecorder:recorder0|addr_r[0]	Top:top0|addr_end_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.555
42	-4.565	Top:top0|AudRecorder:recorder0|addr_r[5]	Top:top0|addr_end_r[5]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.555
43	-4.565	Top:top0|AudRecorder:recorder0|addr_r[24]	Top:top0|addr_end_r[24]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.579
44	-4.555	Top:top0|AudRecorder:recorder0|addr_r[19]	Top:top0|addr_end_r[19]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.569
45	-4.554	Top:top0|AudRecorder:recorder0|addr_r[1]	Top:top0|addr_end_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.544
46	-4.553	Top:top0|AudRecorder:recorder0|addr_r[17]	Top:top0|addr_end_r[17]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.567
47	-4.552	Top:top0|AudRecorder:recorder0|addr_r[14]	Top:top0|addr_end_r[14]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.566
48	-4.539	Top:top0|AudRecorder:recorder0|addr_r[15]	Top:top0|addr_end_r[15]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.553
49	-4.535	Top:top0|AudRecorder:recorder0|addr_r[25]	Top:top0|addr_end_r[25]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.549
50	-4.526	Top:top0|AudRecorder:recorder0|addr_r[13]	Top:top0|addr_end_r[13]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.540
51	-4.523	Top:top0|AudRecorder:recorder0|addr_r[22]	Top:top0|addr_end_r[22]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.537
52	-4.393	Top:top0|AudRecorder:recorder0|addr_r[12]	Top:top0|addr_end_r[12]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.383
53	-4.368	Top:top0|AudRecorder:recorder0|addr_r[18]	Top:top0|addr_end_r[18]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.382
54	-4.359	Top:top0|AudRecorder:recorder0|addr_r[3]	Top:top0|addr_end_r[3]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.349
55	-4.343	Top:top0|AudRecorder:recorder0|addr_r[6]	Top:top0|addr_end_r[6]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.950	1.333
56	-4.315	Top:top0|AudRecorder:recorder0|addr_r[23]	Top:top0|addr_end_r[23]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-2.926	1.329
57	78.334	Debounce:deb1|neg_r	Top:top0|state_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.475	4.523
58	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
59	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
60	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
61	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
62	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
63	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
64	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
65	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
66	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
67	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
68	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
69	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
70	79.227	Debounce:deb1|neg_r	Top:top0|addr_end_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.118	3.987
71	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
72	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
73	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
74	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
75	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
76	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
77	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
78	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
79	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
80	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
81	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
82	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
83	79.321	Top:top0|state_r[0]	Top:top0|addr_end_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.289	4.300
84	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
85	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
86	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
87	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[16]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
88	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[17]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
89	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[18]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
90	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[19]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
91	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[20]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
92	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[21]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
93	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[22]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
94	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[23]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
95	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[24]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
96	79.531	Debounce:deb1|neg_r	Top:top0|addr_end_r[25]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.116	3.685
97	79.600	Top:top0|state_r[2]	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.285	4.017
98	79.600	Top:top0|state_r[2]	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.285	4.017
99	79.600	Top:top0|state_r[2]	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.285	4.017
100	79.600	Top:top0|state_r[2]	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.285	4.017

Slow 1200mV 0C Model Setup: 'CLOCK_50'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
47	-2.105	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.967	2.127
48	-2.105	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.967	2.127
49	-2.103	Top:top0|AudDSP:dsp0|addr_r[8]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.603	2.489
50	-2.102	Top:top0|AudDSP:dsp0|addr_r[9]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.603	2.488
51	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
52	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
53	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
54	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
55	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
56	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
57	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
58	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
59	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
60	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
61	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
62	-2.095	Top:top0|AudRecorder:recorder0|addr_r[17]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.569
63	-2.094	Top:top0|AudDSP:dsp0|addr_r[5]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.545	2.538
64	-2.089	Top:top0|AudRecorder:recorder0|addr_r[2]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.546	2.532
65	-2.082	Top:top0|AudDSP:dsp0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.604	2.467
66	-2.081	Top:top0|AudRecorder:recorder0|addr_r[24]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.555
67	-2.078	Top:top0|AudDSP:dsp0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.540	2.527
68	-2.070	Top:top0|AudRecorder:recorder0|addr_r[23]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.544
69	-2.065	Top:top0|AudRecorder:recorder0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.539
70	-2.064	Top:top0|AudRecorder:recorder0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.532	2.521
71	-2.061	Top:top0|AudRecorder:recorder0|addr_r[22]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.507
72	-2.052	Top:top0|AudRecorder:recorder0|addr_r[18]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.526
73	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
74	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
75	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
76	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
77	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
78	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
79	-2.025	Top:top0|AudRecorder:recorder0|addr_r[25]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.471
80	-2.000	Top:top0|AudDSP:dsp0|addr_r[6]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.446
81	-1.987	Top:top0|AudRecorder:recorder0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.537	2.439
82	-1.986	Top:top0|AudRecorder:recorder0|addr_r[20]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.432
83	-1.970	Top:top0|AudDSP:dsp0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.603	2.356
84	-1.969	Top:top0|AudRecorder:recorder0|addr_r[4]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.546	2.412
85	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
86	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
87	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
88	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
89	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
90	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
91	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
92	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
93	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
94	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
95	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
96	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
97	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
98	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
99	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
100	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
55	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
56	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
57	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
58	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
59	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
60	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
61	-2.101	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.960	2.130
62	-2.095	Top:top0|AudRecorder:recorder0|addr_r[17]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.569
63	-2.094	Top:top0|AudDSP:dsp0|addr_r[5]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.545	2.538
64	-2.089	Top:top0|AudRecorder:recorder0|addr_r[2]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.546	2.532
65	-2.082	Top:top0|AudDSP:dsp0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.604	2.467
66	-2.081	Top:top0|AudRecorder:recorder0|addr_r[24]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.555
67	-2.078	Top:top0|AudDSP:dsp0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.540	2.527
68	-2.070	Top:top0|AudRecorder:recorder0|addr_r[23]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.544
69	-2.065	Top:top0|AudRecorder:recorder0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.539
70	-2.064	Top:top0|AudRecorder:recorder0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.532	2.521
71	-2.061	Top:top0|AudRecorder:recorder0|addr_r[22]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.507
72	-2.052	Top:top0|AudRecorder:recorder0|addr_r[18]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.515	2.526
73	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
74	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
75	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
76	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
77	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
78	-2.039	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.969	2.059
79	-2.025	Top:top0|AudRecorder:recorder0|addr_r[25]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.471
80	-2.000	Top:top0|AudDSP:dsp0|addr_r[6]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.446
81	-1.987	Top:top0|AudRecorder:recorder0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.537	2.439
82	-1.986	Top:top0|AudRecorder:recorder0|addr_r[20]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.543	2.432
83	-1.970	Top:top0|AudDSP:dsp0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.603	2.356
84	-1.969	Top:top0|AudRecorder:recorder0|addr_r[4]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.546	2.412
85	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
86	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
87	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
88	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
89	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
90	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
91	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
92	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
93	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
94	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
95	-1.952	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.960	1.981
96	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
97	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
98	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
99	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971
100	-1.949	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.967	1.971

Slow 1200mV 0C Model Minimum Pulse Width: 'AUD_BCLK'

	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.210	1.000	4.210	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[0]
3	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[10]
4	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[11]
5	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[12]
6	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[13]
7	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[14]
8	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[15]
9	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[16]
10	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[17]
11	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[18]
12	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[19]
13	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[1]
14	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[20]
15	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[21]
16	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[22]
17	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[23]
18	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[24]
19	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[25]
20	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[26]
21	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[2]
22	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[3]
23	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[4]
24	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[5]
25	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[6]
26	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[7]
27	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[8]
28	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[9]
29	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[0]
30	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[1]
31	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[2]
32	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|daclrck_p
33	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[0]
34	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[10]
35	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[11]
36	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[12]
37	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[13]
38	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[14]
39	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[15]
40	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[1]
41	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[2]
42	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[3]
43	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[4]
44	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[5]
45	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[6]
46	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[7]
47	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[8]
48	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[9]
49	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[0]
50	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[10]
51	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[11]
52	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[12]
53	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[13]
54	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[14]
55	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[15]
56	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[1]
57	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[2]
58	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[3]
59	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[4]
60	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[5]
61	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[6]
62	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[7]
63	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[8]
64	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[9]
65	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[0]
66	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[10]
67	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[11]
68	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[12]
69	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[13]
70	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[14]
71	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[15]
72	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[1]
73	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[2]
74	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[3]
75	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[4]
76	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[5]
77	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[6]
78	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[7]
79	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[8]
80	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[9]
81	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|done_r
82	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|read_r
83	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_CALC
84	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_IDLE
85	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_PAUSE
86	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_PLAY
87	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[0]
88	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[1]
89	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[2]
90	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[3]
91	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[0]
92	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[10]
93	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[11]
94	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[12]
95	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[13]
96	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[14]
97	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[15]
98	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[1]
99	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[2]
100	-1.285	1.000	2.285	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[3]

Fast 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-35.334	-872.362
2	qsys0|altpll_0|sd1|pll7|clk[0]	-3.227	-80.252
3	CLOCK_50	-0.722	-25.743
4	qsys0|altpll_0|sd1|pll7|clk[1]	80.867	0.000

Fast 1200mV 0C Model Minimum Pulse Width Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.000	-268.143
2	CLOCK_50	9.234	0.000
3	qsys0|altpll_0|sd1|pll7|clk[0]	41.446	0.000
4	qsys0|altpll_0|sd1|pll7|clk[1]	4999.779	0.000

Fast 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-35.334	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.901
2	-35.254	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.821
3	-35.230	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.797
4	-35.181	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.685	36.764
5	-35.178	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.730	36.806
6	-35.134	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.701
7	-35.101	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.685	36.684
8	-35.098	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.730	36.726
9	-35.077	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.685	36.660
10	-35.074	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.730	36.702
11	-35.054	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.621
12	-35.030	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.597
13	-35.010	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.654
14	-35.001	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.568
15	-34.958	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.775	36.631
16	-34.942	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.586
17	-34.940	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.507
18	-34.930	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.574
19	-34.929	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.573
20	-34.921	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.488
21	-34.906	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.550
22	-34.897	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.464
23	-34.884	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.528
24	-34.878	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.775	36.551
25	-34.862	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.506
26	-34.860	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.427
27	-34.858	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.502
28	-34.854	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.775	36.527
29	-34.849	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.493
30	-34.838	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.482
31	-34.836	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.669	36.403
32	-34.825	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.469
33	-34.804	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.448
34	-34.780	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.424
35	-34.778	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.422
36	-34.754	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.398
37	-34.737	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.381
38	-34.734	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.378
39	-34.657	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.301
40	-34.656	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.300
41	-34.654	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.298
42	-34.633	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.277
43	-34.630	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.274
44	-34.590	Top:top0|speed_r[0]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.730	36.218
45	-34.576	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.220
46	-34.552	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.746	36.196
47	-34.510	Top:top0|speed_r[2]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.730	36.138
48	-34.486	Top:top0|speed_r[1]	Top:top0|AudDSP:dsp0|del_data_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.730	36.114
49	-22.482	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.582
50	-22.410	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.510
51	-22.401	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.459
52	-22.344	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.402
53	-22.329	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.139	23.445
54	-22.326	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.184	23.487

55	-22.301	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	23.166
56	-22.282	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.123	23.382
57	-22.262	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.362
58	-22.257	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.139	23.373
59	-22.254	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.184	23.415
60	-22.246	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.069	23.322
61	-22.243	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.114	23.364
62	-22.221	Top:top0|AudDSP:dsp0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.279
63	-22.220	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.320
64	-22.212	Top:top0|AudDSP:dsp0|data_r[10]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	23.077
65	-22.210	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	CLOCK_50	AUD_BCLK	1.000	0.123	23.310
66	-22.201	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.259
67	-22.200	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.300
68	-22.192	Top:top0|AudDSP:dsp0|data_r[9]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	23.057
69	-22.189	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.069	23.265
70	-22.186	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	0.114	23.307
71	-22.182	Top:top0|AudDSP:dsp0|data_r[5]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.028	23.217
72	-22.158	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[14]	CLOCK_50	AUD_BCLK	1.000	0.200	23.335
73	-22.153	Top:top0|AudDSP:dsp0|data_r[4]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.211
74	-22.150	Top:top0|AudDSP:dsp0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.208
75	-22.149	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[3]	CLOCK_50	AUD_BCLK	1.000	0.123	23.249
76	-22.145	Top:top0|AudDSP:dsp0|data_r[12]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	23.010
77	-22.144	Top:top0|AudDSP:dsp0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.202
78	-22.140	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.240
79	-22.139	Top:top0|AudDSP:dsp0|data_r[11]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	23.004
80	-22.136	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[15]	AUD_BCLK	AUD_BCLK	1.000	-0.072	23.071
81	-22.130	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	-0.108	23.029
82	-22.119	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.219
83	-22.109	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.139	23.225
84	-22.106	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[1]	CLOCK_50	AUD_BCLK	1.000	0.229	23.312
85	-22.106	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.184	23.267
86	-22.101	Top:top0|AudDSP:dsp0|data_r[8]	Top:top0|AudDSP:dsp0|del_data_r[7]	AUD_BCLK	AUD_BCLK	1.000	-0.142	22.966
87	-22.090	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[12]	CLOCK_50	AUD_BCLK	1.000	0.200	23.267
88	-22.088	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[2]	CLOCK_50	AUD_BCLK	1.000	0.123	23.188
89	-22.087	Top:top0|AudDSP:dsp0|data_r[14]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	22.952
90	-22.086	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	CLOCK_50	AUD_BCLK	1.000	0.200	23.263
91	-22.082	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	Top:top0|AudDSP:dsp0|del_data_r[13]	CLOCK_50	AUD_BCLK	1.000	0.123	23.182
92	-22.082	Top:top0|AudDSP:dsp0|data_r[6]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.140
93	-22.077	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	Top:top0|AudDSP:dsp0|del_data_r[11]	CLOCK_50	AUD_BCLK	1.000	0.200	23.254
94	-22.077	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	CLOCK_50	AUD_BCLK	1.000	0.123	23.177
95	-22.075	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[14]	AUD_BCLK	AUD_BCLK	1.000	0.130	23.212
96	-22.069	Top:top0|AudDSP:dsp0|data_r[13]	Top:top0|AudDSP:dsp0|del_data_r[13]	AUD_BCLK	AUD_BCLK	1.000	-0.142	22.934
97	-22.068	Top:top0|AudDSP:dsp0|data_r[0]	Top:top0|AudDSP:dsp0|del_data_r[3]	AUD_BCLK	AUD_BCLK	1.000	0.051	23.126
98	-22.067	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[10]	CLOCK_50	AUD_BCLK	1.000	0.139	23.183
99	-22.066	Top:top0|AudDSP:dsp0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[10]	AUD_BCLK	AUD_BCLK	1.000	0.069	23.142
100	-22.064	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	Top:top0|AudDSP:dsp0|del_data_r[15]	CLOCK_50	AUD_BCLK	1.000	0.184	23.225

Fast 1200mV 0C Model Setup: 'qsys0\|altpll_0\|sd1\|pll7\|clk[0]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-3.227	Top:top0|AudDSP:dsp0|done_r	Top:top0|state_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.900	1.255
2	-3.091	Top:top0|AudRecorder:recorder0|done_r	Top:top0|state_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.865	1.154
3	-3.059	Top:top0|AudDSP:dsp0|done_r	Top:top0|state_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.895	1.092
4	-3.039	Top:top0|AudRecorder:recorder0|done_r	Top:top0|state_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.860	1.107
5	-2.899	Top:top0|AudRecorder:recorder0|addr_r[20]	Top:top0|addr_end_r[20]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	1.131
6	-2.883	Top:top0|AudRecorder:recorder0|addr_r[4]	Top:top0|addr_end_r[4]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	1.102
7	-2.866	Top:top0|AudRecorder:recorder0|addr_r[11]	Top:top0|addr_end_r[11]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	1.085
8	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
9	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
10	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
11	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[3]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
12	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[4]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
13	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[5]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
14	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[6]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
15	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[7]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
16	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[8]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
17	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[9]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
18	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[10]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
19	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[11]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
20	-2.797	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[12]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.690	1.035
21	-2.767	Top:top0|AudRecorder:recorder0|addr_r[7]	Top:top0|addr_end_r[7]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.986
22	-2.722	Top:top0|AudRecorder:recorder0|addr_r[16]	Top:top0|addr_end_r[16]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.954
23	-2.698	Top:top0|AudRecorder:recorder0|addr_r[10]	Top:top0|addr_end_r[10]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.917
24	-2.635	Top:top0|AudRecorder:recorder0|addr_r[9]	Top:top0|addr_end_r[9]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.854
25	-2.627	Top:top0|AudRecorder:recorder0|addr_r[0]	Top:top0|addr_end_r[0]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.846
26	-2.627	Top:top0|AudRecorder:recorder0|addr_r[8]	Top:top0|addr_end_r[8]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.846
27	-2.627	Top:top0|AudRecorder:recorder0|addr_r[21]	Top:top0|addr_end_r[21]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.859
28	-2.626	Top:top0|AudRecorder:recorder0|addr_r[2]	Top:top0|addr_end_r[2]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.845
29	-2.622	Top:top0|AudRecorder:recorder0|addr_r[5]	Top:top0|addr_end_r[5]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.841
30	-2.618	Top:top0|AudRecorder:recorder0|addr_r[19]	Top:top0|addr_end_r[19]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.850
31	-2.617	Top:top0|AudRecorder:recorder0|addr_r[14]	Top:top0|addr_end_r[14]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.849
32	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[13]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
33	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[14]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
34	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[15]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
35	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[16]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
36	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[17]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
37	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[18]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
38	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[19]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
39	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[20]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
40	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[21]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
41	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[22]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
42	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[23]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
43	-2.616	Top:top0|AudRecorder:recorder0|addr_r[24]	Top:top0|addr_end_r[24]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.848
44	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[24]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
45	-2.616	Top:top0|AudRecorder:recorder0|done_r	Top:top0|addr_end_r[25]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.687	0.857
46	-2.612	Top:top0|AudRecorder:recorder0|addr_r[15]	Top:top0|addr_end_r[15]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.844
47	-2.611	Top:top0|AudRecorder:recorder0|addr_r[1]	Top:top0|addr_end_r[1]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.830
48	-2.610	Top:top0|AudRecorder:recorder0|addr_r[17]	Top:top0|addr_end_r[17]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.842
49	-2.606	Top:top0|AudRecorder:recorder0|addr_r[25]	Top:top0|addr_end_r[25]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.838
50	-2.601	Top:top0|AudRecorder:recorder0|addr_r[22]	Top:top0|addr_end_r[22]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.833
51	-2.600	Top:top0|AudRecorder:recorder0|addr_r[13]	Top:top0|addr_end_r[13]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.832
52	-2.535	Top:top0|AudRecorder:recorder0|addr_r[12]	Top:top0|addr_end_r[12]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.754
53	-2.522	Top:top0|AudRecorder:recorder0|addr_r[18]	Top:top0|addr_end_r[18]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.754
54	-2.512	Top:top0|AudRecorder:recorder0|addr_r[3]	Top:top0|addr_end_r[3]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.731

55	-2.503	Top:top0|AudRecorder:recorder0|addr_r[6]	Top:top0|addr_end_r[6]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.709	0.722
56	-2.487	Top:top0|AudRecorder:recorder0|addr_r[23]	Top:top0|addr_end_r[23]	AUD_BCLK	qsys0|altpll_0|sd1|pll7|clk[0]	0.001	-1.696	0.719
57	80.502	Debounce:deb1|neg_r	Top:top0|state_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.254	2.564
58	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
59	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
60	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
61	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
62	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
63	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
64	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
65	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
66	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
67	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
68	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
69	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
70	81.060	Debounce:deb1|neg_r	Top:top0|addr_end_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.084	2.176
71	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
72	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
73	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
74	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
75	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[4]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
76	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[5]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
77	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[6]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
78	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[7]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
79	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[8]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
80	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[9]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
81	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[10]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
82	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[11]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
83	81.132	Top:top0|state_r[0]	Top:top0|addr_end_r[12]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.134	2.322
84	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[13]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
85	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[14]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
86	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[15]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
87	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[16]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
88	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[17]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
89	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[18]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
90	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[19]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
91	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[20]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
92	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[21]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
93	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[22]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
94	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[23]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
95	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[24]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
96	81.241	Debounce:deb1|neg_r	Top:top0|addr_end_r[25]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	-0.081	1.998
97	81.268	Top:top0|state_r[2]	Top:top0|addr_end_r[0]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.129	2.181
98	81.268	Top:top0|state_r[2]	Top:top0|addr_end_r[1]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.129	2.181
99	81.268	Top:top0|state_r[2]	Top:top0|addr_end_r[2]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.129	2.181
100	81.268	Top:top0|state_r[2]	Top:top0|addr_end_r[3]	qsys0|altpll_0|sd1|pll7|clk[0]	qsys0|altpll_0|sd1|pll7|clk[0]	83.333	0.129	2.181

Fast 1200mV 0C Model Setup: 'CLOCK_50'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.722	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.390	1.309
2	-0.722	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.390	1.309
3	-0.722	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.390	1.309
4	-0.684	Top:top0|AudRecorder:recorder0|addr_r[5]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.527
5	-0.680	Top:top0|AudRecorder:recorder0|addr_r[1]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.139	1.518
6	-0.661	Top:top0|AudRecorder:recorder0|addr_r[9]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.504
7	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
8	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
9	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
10	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
11	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
12	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
13	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
14	-0.650	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.264
15	-0.626	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.390	1.213
16	-0.626	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.390	1.213
17	-0.626	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.390	1.213
18	-0.620	Top:top0|AudRecorder:recorder0|addr_r[7]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.128	1.469
19	-0.617	Top:top0|AudDSP:dsp0|addr_r[24]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.161	1.433
20	-0.611	Top:top0|AudRecorder:recorder0|addr_r[19]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.118	1.470
21	-0.609	Top:top0|AudDSP:dsp0|addr_r[16]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.161	1.425
22	-0.596	Top:top0|AudRecorder:recorder0|addr_r[11]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.128	1.445
23	-0.595	Top:top0|AudRecorder:recorder0|addr_r[12]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.139	1.433
24	-0.588	Top:top0|AudRecorder:recorder0|addr_r[13]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.118	1.447
25	-0.586	Top:top0|AudDSP:dsp0|addr_r[5]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.429
26	-0.583	Top:top0|AudRecorder:recorder0|addr_r[16]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.436
27	-0.571	Top:top0|AudRecorder:recorder0|addr_r[3]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.414
28	-0.558	Top:top0|AudRecorder:recorder0|addr_r[22]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.147	1.388
29	-0.555	Top:top0|AudRecorder:recorder0|addr_r[23]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.408
30	-0.553	Top:top0|AudDSP:dsp0|addr_r[21]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.166	1.364
31	-0.552	Top:top0|AudRecorder:recorder0|addr_r[2]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.139	1.390
32	-0.552	Top:top0|AudDSP:dsp0|addr_r[9]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.160	1.369
33	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
34	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
35	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
36	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
37	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
38	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
39	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
40	-0.552	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.363	1.166
41	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
42	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
43	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
44	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
45	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
46	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
47	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
48	-0.551	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.159
49	-0.550	Top:top0|AudDSP:dsp0|addr_r[15]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.155	1.372
50	-0.548	Top:top0|AudRecorder:recorder0|addr_r[8]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.391
51	-0.548	Top:top0|AudDSP:dsp0|addr_r[4]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.165	1.360
52	-0.545	Top:top0|AudRecorder:recorder0|addr_r[17]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.398
53	-0.545	Top:top0|AudRecorder:recorder0|addr_r[15]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.118	1.404
54	-0.543	Top:top0|AudDSP:dsp0|addr_r[8]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.160	1.360

55	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
56	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
57	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
58	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
59	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
60	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
61	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
62	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
63	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
64	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
65	-0.540	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.150
66	-0.538	Top:top0|AudRecorder:recorder0|addr_r[21]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.129	1.386
67	-0.534	Top:top0|AudDSP:dsp0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.161	1.350
68	-0.525	Top:top0|AudRecorder:recorder0|addr_r[18]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.378
69	-0.525	Top:top0|AudRecorder:recorder0|addr_r[24]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.378
70	-0.517	Top:top0|AudDSP:dsp0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.128	1.366
71	-0.516	Top:top0|AudRecorder:recorder0|addr_r[14]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.124	1.369
72	-0.511	Top:top0|AudRecorder:recorder0|addr_r[25]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.147	1.341
73	-0.510	Top:top0|AudRecorder:recorder0|addr_r[0]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.128	1.359
74	-0.509	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
75	-0.509	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
76	-0.509	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
77	-0.509	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
78	-0.509	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
79	-0.509	Top:top0|AudRecorder:recorder0|write_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.372	1.114
80	-0.507	Top:top0|AudRecorder:recorder0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.134	1.350
81	-0.504	Top:top0|AudDSP:dsp0|addr_r[10]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.160	1.321
82	-0.492	Top:top0|AudRecorder:recorder0|addr_r[20]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.147	1.322
83	-0.484	Top:top0|AudDSP:dsp0|addr_r[6]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.130	1.331
84	-0.460	Top:top0|AudDSP:dsp0|addr_r[19]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.155	1.282
85	-0.455	Top:top0|AudRecorder:recorder0|addr_r[4]	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.139	1.293
86	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
87	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
88	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
89	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
90	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
91	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
92	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
93	-0.453	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|data_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.369	1.061
94	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
95	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
96	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
97	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
98	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
99	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054
100	-0.444	Top:top0|AudDSP:dsp0|read_r	Lab3_qsys:qsys0|SDRAMWrapper:sdram_wrapper_0|addr_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.367	1.054

Fast 1200mV 0C Model Minimum Pulse Width: 'AUD_BCLK'

	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[0]
3	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[10]
4	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[11]
5	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[12]
6	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[13]
7	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[14]
8	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[15]
9	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[16]
10	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[17]
11	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[18]
12	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[19]
13	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[1]
14	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[20]
15	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[21]
16	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[22]
17	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[23]
18	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[24]
19	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[25]
20	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[26]
21	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[2]
22	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[3]
23	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[4]
24	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[5]
25	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[6]
26	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[7]
27	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[8]
28	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|addr_r[9]
29	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[0]
30	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[1]
31	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[2]
32	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|daclrck_p
33	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[0]
34	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[10]
35	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[11]
36	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[12]
37	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[13]
38	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[14]
39	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[15]
40	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[1]
41	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[2]
42	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[3]
43	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[4]
44	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[5]
45	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[6]
46	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[7]
47	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[8]
48	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_nxt_r[9]
49	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[0]
50	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[10]
51	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[11]
52	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[12]
53	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[13]
54	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[14]

55	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[15]
56	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[1]
57	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[2]
58	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[3]
59	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[4]
60	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[5]
61	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[6]
62	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[7]
63	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[8]
64	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|data_r[9]
65	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[0]
66	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[10]
67	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[11]
68	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[12]
69	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[13]
70	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[14]
71	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[15]
72	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[1]
73	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[2]
74	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[3]
75	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[4]
76	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[5]
77	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[6]
78	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[7]
79	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[8]
80	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|del_data_r[9]
81	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|done_r
82	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|read_r
83	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_CALC
84	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_IDLE
85	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_PAUSE
86	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|state_r.S_PLAY
87	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[0]
88	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[1]
89	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[2]
90	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|bit_counter_r[3]
91	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[0]
92	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[10]
93	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[11]
94	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[12]
95	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[13]
96	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[14]
97	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[15]
98	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[1]
99	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[2]
100	-1.000	1.000	2.000	Min Period	AUD_BCLK	Fall	Top:top0|AudPlayer:player0|data_r[3]

Problem & Solution

1. Port is multiple driven
    a. Check whether there is the same signal with different logic assignment in the always_comb block
2. Improper register removal
    a. Check whether state transition logic or always_ff block is correct
3. Timing assignment not met
    a. Some calculations like the division to implement linear interpolation needed extra clock cycles but did not affect this task
    b. This may be due to the fact that the calculated quotient (signal increment) does not affect any other registers immediately, only until another LRCLK

Conclusion & Suggestion:

All that said, we had a lot of fun doing this experiment. From the happy debugging time in the start, and starting to look forward to the moment of recording, to the happiness of constantly replaying music in the end.

In addition, we have learned more about using the Qsys library in Quartus II, and we have written our own components to transform the original codebase written for SRAM into one that can work with SDRAM.