Architecture class overview

```
Mux-
    Setup(Readable Hardware, Readable Hardware)
    Select(bool)
    Read()
Control
    Setup(Memory, All Muxes)
    Clock(){
        switch(opcode){
            Case add:
                mux1.Select(0)
                Etc..
        }
    }
Memory
    Setup(File, Control)
    Clock(){
        If Control.Write(){
            Write data
        }
        etc...
    }
    Load(address){
        Return memory[address]
    }
    store(byte, address)
        Memory[address] = byte
    }

Registers{
    Setup(){
        Pc = 0x200
```

```
        }
        Store(number,data)
        load(number)
        Store and load for all special registers
        StoreStack(data)
        LdStack()
ShiftLeft
        shift(value)
ALU
        Setup(Registers, mux, Control)
        Clock()
                control.read()
                switch
                        Case xor:
                                Register.read xor mux.read
        read()
```