CSC 350 Project 2 - Mid Project Report

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A) Our program overview has been defined in which we have a Main, Fetch/Decode, Execute/Writeback, Register, Memory, and Display classes. The base hardware components including the memory and register classes have been implemented in software. Opcode classes have been defined and are beginning to be worked on. The interactions between those components have also been abstractly defined however they have not been fully implemented, work is continuing in this area.

B) Trying to simulate all hardware components such as the control, ALU, and muxes through java proved to be too complicated as the various electrical interactions didn't transfer well to software, especially if pipelining was to occur. We changed our approach to simulate a Fetch/Decode block and an Execute/Writeback block instead of each individual piece of hardware.

C) In addition to simulating a basic 8-bit processor, a version using a simple 2-stage pipeline, fetch/decode followed by execute/writeback, will also be implemented.