CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: 8-2

Team Members: Sam Burrell

Justin Jaeckel

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Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*
  - *We show up to meetings for full amount of time and work diligently.*
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
  - *We will communicate via the messaging application Discord.*
- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*
  - *Writing everything in camel case and making sure our comments are thought out to easily describe the process*
- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please*

include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:
    - *We will meet Monday Wednesday and Thursday to work on lab.*
- **Peer Evaluation Criteria:** *Please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.*
    - *Overall willingness to show up and Contribution/work to get things done. We will use GitHub to organize and combine work efforts*

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part	Estimated Time	Design		Test	
		Lead	Timeline	Lead	Timeline
High-level design	1 hr	Sam	By Oct 7th	Justin	Oct 7th
Test programs	4 hr	Justin	Oct 28th	Sam	Oct 28th
Control logic	2 hr	Sam	Oct 14th	Justin	Oct 14th
Fetch logic	3 hr	Justin	Oct 14th	Sam	Oct 14th
Barrel shifter	2 hr	Sam	Oct 21st	Justin	Oct 21st
ALU integration + Misc updates	2 hr	Justin	Oct 21st	Sam	Oct 21st
High-level integration	4 hr	Sam	Oct 28th	Justin	Oct 28th
Synthesis (human effort)	1.5 hr	Justin	Oct 28th	Sam	Oct 28th

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Sam Burrell **Date** 10/5/2022

Student Signature Justin Jaeckel **Date** 10/5/2022

Student Signature _____ **Date** _____