JINKYU PARK

Digital Signal Processing Engineer

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SUMMARY STATEMENT

Dedicated digital signal processing engineer from theoretical algorithm to hardware level implementation. Variously involved signal processing system projects with diverse industry fields such as commercial wireless repeater, military synthetic aperture radar, and automobile Lidar. Also, studied about wide system level which is from a technique for analog to digital converter in ASIC level to a physical layer for wireless system level.

PROFESSIONAL EXPERIENCE

DSP Engineer

LightIC Technologies USA, Santa Clara, California — March 2021 – Present

Achievements

- Improved detection probability, resolution, system linearity, scan rate for Light Detection and Ranging (Lidar) system
- Built up Lidar signal processing simulator by using Python

Key Responsibilities

- Analyzed raw Lidar signal and debugged the system implementation
- Implemented signal function block for high performance Lidar
- Build digital signal processing algorithm for laser linearity, target detection of Lidar on software level (Python)
- Implemented the algorithms on hardware level by using FPGA (Verilog-HDL)
- Analyzed and measured the prototype Lidar performance
- Development environment : Python for digital signal processing, Xilinx Zynq FPGA, Xilinx Vivado on Linux and Windows

Senior FPGA Engineer

Sodick America Inc., San Jose, California — July 2019 – March 2021

Achievements

- Developed in-house low-latency protocol by using 10Gb transceiver optical fiber communication for high precision milling machine and high performance wired electrical discharge machining

Key Responsibilities

- Coded high-speed RTL code (Verilog-HDL) for optical communication protocol, simulation / verification
- Implemented and verified PCIe interface with CPU, AXI in FPGA
- The RTL module similar with Internet/Link layer of TCP/IP
- Analyzed and measured the communication frame performance
- Development environment : Microsemi PolarFire, Microsemi Libero SoC, Synplify, Questa, Identify on Linux and Windows

Research / Teaching Assistant

The university of Texas at Dallas, Richardson, Texas — January 2014 – May 2019

- Researched self-calibration for A successive approximation ADC
- Assisted under-graduate classes and lab exercises

Research Engineer

Agency for Defense Development (South Korea's national research organization), Daejeon, South Korea — May 2009 – March 2012

Achievements

- Developed prototype Synthetic Aperture Radar (SAR) for Unmanned Aerial Vehicle (UAV)
- Developed radar signal processing software for satellite physical layer (L0 processor)

Key Responsibilities

- Developed signal processing algorithm for compensation against airframe turbulence
- Verified SAR signal processing for aerial vehicle and implemented a SAR signal receiver module (high speed signal processing module, VHDL); digital down converter, channel equalizer, compensation function against airframe turbulence, flexible sampling rate scheme, pulse compression and presumming function by FPGA and DSP

- Implemented 1G Ethernet PCS/PMA Xilinx for burst data communication between FPGA and Linux signal processing block
- Analyzed a performance of other SAR systems
- Coded satellite radar signal processing protocol program by C++
- Analyzed the satellite navigation coordinator and earth-based coordinate system, received signal characteristic base on the orbit of the satellite
- Conducted environment and robustness test of signal processing block (from third party) for prototype SAR
- Research / development environment : Matlab, C++, Xilinx Virtex6, ISE, ModelSim, Xilinx Chipscope, Cadence tool for board design on Unix and Windows

Digital Signal Processing / RTL Engineer

Solid Technologies INC., Seoul, South Korea — July 2007 – March 2009

Achievements

- Developed a digital signal processing board of digital optical repeater system for expand cell coverage of CDMA and WCDMA
- Developed prototype wireless communication repeater by using Ethernet protocol and cable
- Developed Interference / echo Cancellation System (ICS) on GSM
- Developed Digital Pre-Distortion (DPD) for wireless communication repeater front-end

Key Responsibilities

- Coded a digital signal processing module for digital filter, channel equalizer, digital up/down converter, simulation / verification
- Developed a wireless communication channel estimation algorithm (adapter signal processing) and generation of echo cancelled GSM signal by Matlab
- Implemented and verified the ICS algorithm by using the FPGA and DSP
- Designed the crest factor reduction (CFR) algorithm and DPD algorithm by using Matlab
- Coded the CFR and DPD algorithm (VHDL) on digital signal processing board
- Designed prototype digital signal processing board for a power over Ethernet for cordless repeater system
- Coded interface between FPGA, ADC and DAC in severe environment
- Conducted the performance and environment robustness test of the digital signal processing board (signal generator, spectrum analyzer, and temperature chamber) in laboratory
- Implemented synchronous Ethernet by 1G Ethernet PCS/PMA and SGMII Xilinx with Marvell Ethernet PHY
- Research / development environment : Matlab, C++, Xilinx Virtex5, ISE, Modelsim, Xilinx Chipscope, Cadence tool for board design on Windows

Education

M. Eng. Electrical Engineering (3.697/4.0 GPA)**,** The university of Texas at Dallas, Richardson, TX — May 2020

Incomplete Ph. D. Electrical Engineering, The university of Texas at Dallas, Richardson, TX — From January 2014

Specializations: Analog/digital mixed signal circuit design, system analysis base on signal processing

M. Eng. Electrical Engineering (4.38/4.50 GPA), Pukyong National University, Busan, South Korea — August 2007

B. Eng. Electrical Engineering (3.94/4.50 GPA), Pukyong National University, Busan, South Korea — August 2005

Academic Research

A successive approximation (SAR) ADC

The university of Texas at Dallas, Richardson, TX — August 2015 – June 2019

- Researched digital background calibration and self-calibration for SAR ADC
- Developed algorithms for ideal performance with SAR ADC base on digital signal processing algorithm
- Developed SAR ADC operation/calibration logic block by using NI FPGA(VHDL), verification of prototype SAR ADC performance
- Tape-out configuration block for analog circuit; coded Verilog-HDL, lay-out for silicon

Wireless communication physical layer simulation software with ETRI (South Korea's national research organization)

Pukyong National University, Busan, South Korea — March 2003 – November 2007

- Developed control algorithm of transmission power and modulation level for cognitive radio systems

- Developed the simulator of evaluating interference between IEEE802.16e (draft in 2004) and the WLAN by using C++
- Coded a software simulator for evaluating the interference between the WLAN system and the IEEE802.22 by using C++
- Developed a radar function in spectrum engineering advanced monte carlo analysis tool by using JAVA(2012)

PUBLICATIONS

JOURNAL PAPER

[1] **Jinkyu Park**, Chang Heon Lim and Jin-Yul Kim, “An On/Off Power Control for OFDM Transmission Scheme in a Cochannel Interference Environment”, *The Journal of Korea Institute Electromagnetic Engineering Society,* vol. 32, no. 11, pp. 1182-1189, Nov. 2007

[2] **Jinkyu Park** and Chang Heon Lim, “A Spread Spectrum System Using Adaptive Modulation and Switched Diversity”, *The Journal of Korea Institute Electromagnetic Engineering Society,* vol. 18, no. 4, pp. 440-447, Apr. 2007

[3] **Jinkyu Park** and Chang Heon Lim, “A Power Control for OFDM Transmission Scheme in a Cochannel Interference Environment”, *The Journal of Korea Information and Communications Society,* vol. 32, no. 3, pp. 271-280, Mar. 2007

CONFERENCE PROCEEDING

[1] **Jinkyu Park** and Won Namgoong, “An Approach to Compensate for Capacitor Mismatches in SAR ADC Using Multiple Comparisons”, *the IEEE International Symposium on Circuits and Systems,* May. 2019

[2] **Jinkyu Park** and Chang Heon Lim, “An Adaptive Modulation Scheme with Switched Diversity for Rayleigh Fading Channels”, *Proceeding of the IEEE Asia-Pacific Conference on Communication,* Aug. 2006

SOFTWEAR COPYRIGHT

[1] Jung Hun Hwang and **Jinkyu Park**, "CCSDS file analysis software on MS-SAR project", Korea Copyright Commission, S-2011-005191, Aug. 2011