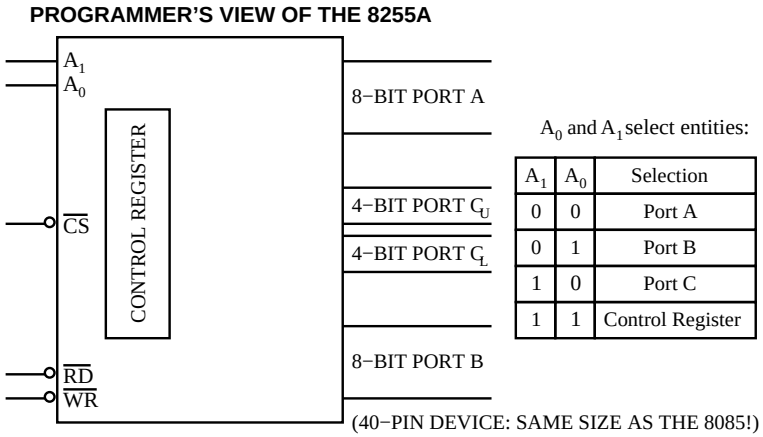
EE309: Computer Organization, Architecture and MicroProcessors

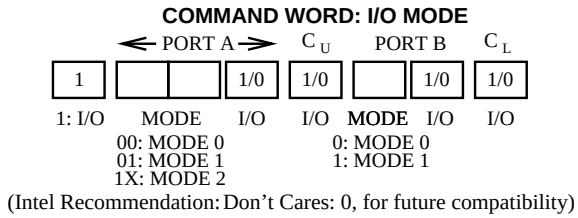
http://www.ee.iitb.ac.in/∼sumantra/courses/up/up.html

The 8255A: Programmable Peripheral Interface

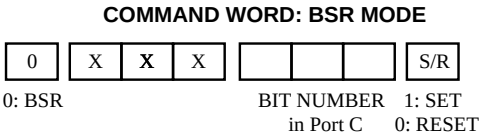


A_0 and A_1 select entities:

A_1	A_0	Selection
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Register

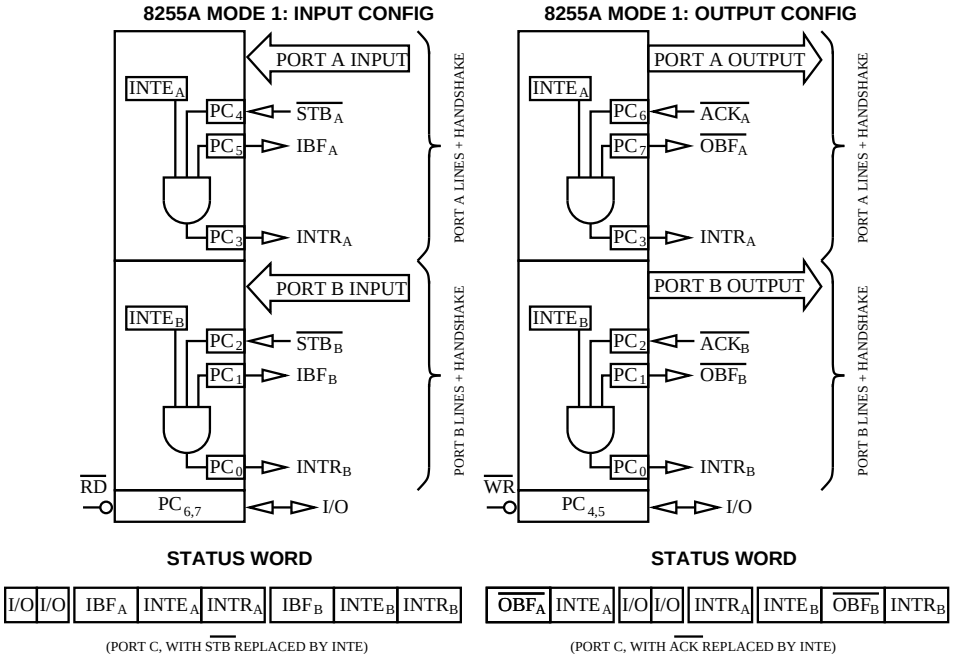


(Intel Recommendation: Don't Cares: 0, for future compatibility)



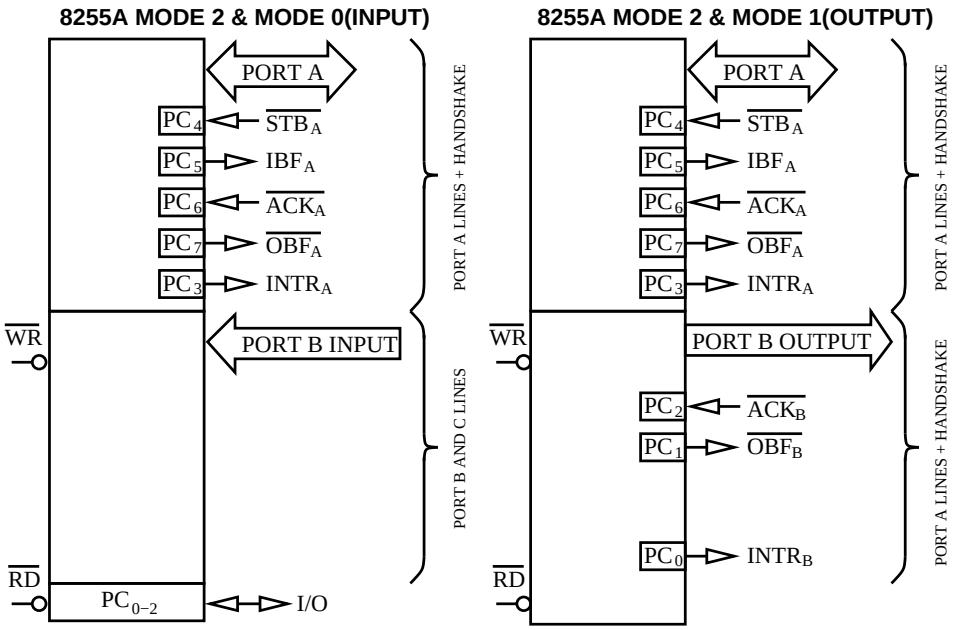
BSR Mode

- To set / reset bits in Port C, the control word is written in the Control Register
- BSR Control Word affects one bit at a time
- Does not affect the I/O mode



I/O Mode

1. **Mode 0**
   - Simple I/O for Ports A, B, C
   - A port is either an input port, or an output port
   - Inputs are not latched, outputs are
   - Ports do not have interrupt or handshake capability
2. **Mode 1**
   - Ports A and B: a port is either an input port, or an output port
   - Each port uses 3 lines of Port C for handshaking, the remaining 2 bits can be used for simple I/O (Mode 0)
   - Input and output data are latched
   - Interrupt Logic is supported
3. **Mode 2**
   - Port A used as a bidirectional port
   - Port B can be used in either Mode 0 or Mode 1
   - Port A uses 5 bits of Port C for handshaking: the remaining can be used for simple I/O (Mode 0) for Port B in Mode 0, or as handshaking lines for Port B in Mode 1

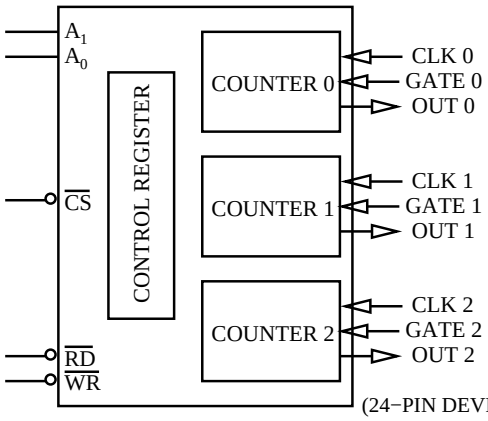


The 8253/4: Programmable Interval Timer

The 6 Modes of the 8253/4

1. **Mode 0: Interrupt on Terminal Count**
   - Rules for OUT:
     - After the count reaches 0, OUT goes high
     - OUT remains high until a new count or command word is loaded
     - Counting temporarily stops when the GATE is disabled, and continues again when the GATE goes to logic high
   - Auxiliary Rules: If count register reloaded while counting is on, then
     - After first byte of count written, the current counting stops
     - After second byte of count written, the counting restarts with the new count number
   - Rules for GATE
     - Low / going low: disables counting
     - High: enables counting
     - Other cases: no effect
2. **Mode 1: Programmable One-Shot / Hardware Retriggerable One-Shot**
   - Rules for OUT
     - OUT is initially high
     - When GATE is triggered, OUT goes low
     - After the end of the count, OUT goes high again
   - Auxiliary Rule: If new count loaded while output is low, doesn't affect duration of one-shot OUT negative pulse until the next trigger

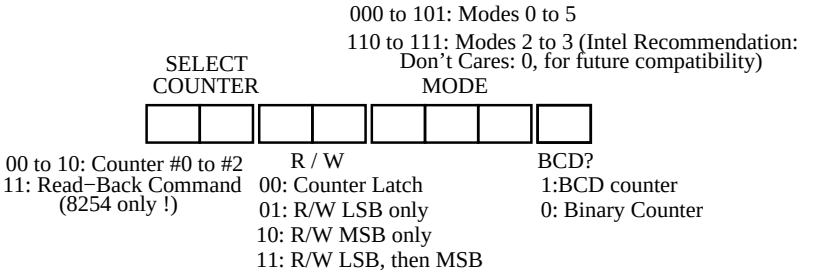
PROGRAMMER'S VIEW OF THE 8253/4



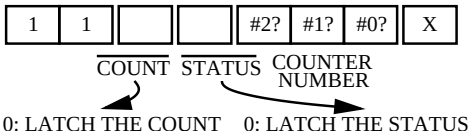
A_0 and A_1 select entities:

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

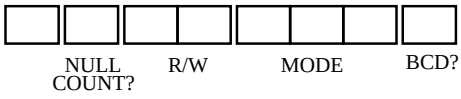
THE 8253/4 CONTROL WORD



8254 READ−BACK COMMAND



8254 READ−BACK STATUS



- The current count can be read anytime, doesn't affect one-shot pulse
- Rules for GATE
  - Rising: Initiates counting, resets OUT on next clock
  - Other cases: no effect

3. **Mode 2: Interrupt on Terminal Count**

- Rules for OUT
  - Generate a pulse of width = clock period, at a given interval
  - When a count is loaded, OUT goes high and remains high until count = 1, then goes low for one clock period (at the count of 0)
  - Count reloaded automatically, the pulse generated continuously
  - count = 1 is not allowed !
- Auxiliary Rule: If count register reloaded while counting is on, then
  - The current output pulse timing is not affected
  - The next one is, according to the new value of the count
- Rules for GATE
  - Low / going low: disables counting, OUT goes high immediately

  - Rising: Initiates counting
  - High: Enables counting

4. **Mode 3: Square Wave Generator**
   - Rules for OUT
     - When the count N is loaded, OUT is high
     - If N is even, the pulse stays high for the first $N/2$ clock cycles, and low for the next $N/2$. If N is odd, the pulse stays high for $(N+1)/2$ clock cycles, and then low for $(N-1)/2$ clock cycles
     - When the count should have hit 0 (0 is not counted), OUT goes low for the next cycle, and the count is reloaded again
     - For an even count, the count is decremented by 2
     - For an odd count, for the first (high) half, the count is first decremented by 1, then by 2. For the second (low) half, the count is first decremented by 3, then by 2.
   - Auxiliary Rule: If count register reloaded while counting is on, then
     - The current output pulse timing is not affected
     - The next one is, according to the value of N
   - Rules for GATE
     - Low / going low: disables counting, OUT goes high immediately
     - Rising: Initiates counting
     - High: Enables counting

5. **Mode 4: Software-Triggered Strobe**
   - Rules for OUT
     - OUT is initially high
     - Goes low for one clock period *at* the end of the count, and then goes high after the end of the count
   - Auxiliary Rule If count register reloaded while counting is on, then the new count is initialized on the next clock pulse
   - Rules for GATE
     - Low / going low: disables counting
     - High: Enables counting
     - Other cases: no effect

6. **Mode 5: Hardware-Triggered Strobe**
   - Rules for OUT
     - OUT is initially high
     - Goes low for one clock period *at* the end of the count
   - Auxiliary Rule If count register reloaded while counting is on, then the new count is initialized on the next clock pulse
   - Rules for GATE
     - Rising: Initiates counting
     - Other cases: no effect