

1 General Description

The RDA5802N series is the newest generation single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity, RDS/RBDS and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. The RDA5802N series have three type package sizes , respective are RDA5802N (QFN 4X4 mm, 24pins), RDA5802NS (QFN 3X3 mm, 20pins) and RDA5802NM (QFN 2X2 mm, 12pins). All these make it very suitable for portable devices.

The RDA5802N series has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5802N series support frequency range is from 50MHz to 115MHz.

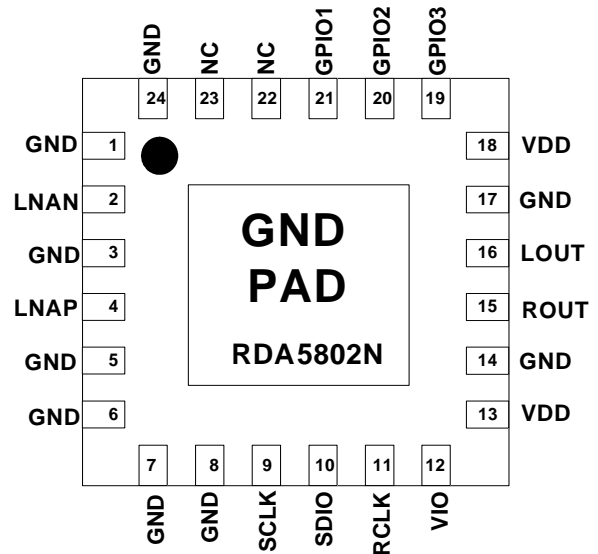


Figure1-1. RDA5802N Top View

1.1 Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
 - Total current consumption lower than 20mA at 3.0V power supply when under normal situation
- Support worldwide frequency band
 - 50 -115 MHz
- Support flexible channel spacing mode
 - 100KHz, 200KHz, 50KHz and 25KHz
- Support RDS/RBDS
- Digital low-IF tuner
 - Image-reject down-converter
 - High performance A/D converter
 - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
 - Fully integrated on-chip RF and IF VCO
 - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
 - Mono/stereo switch
 - Soft mute
 - High cut
- Programmable de-emphasis (50/75 μ s)
- Receive signal strength indicator (RSSI) and SNR
- Bass boost
- Volume control and mute
- I²S digital output interface
- Line-level analog output voltage
- 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
- Only support 2-wire bus interface

- Directly support 32Ω resistance loading
- Integrated LDO regulator
 - 1.8 to 5.5 V operation voltage
- Support QFN 4X4mm 24pins, QFN 3X3mm 20pins and QFN 2x2mm 12pins three package types.

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook

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2 Functional Description

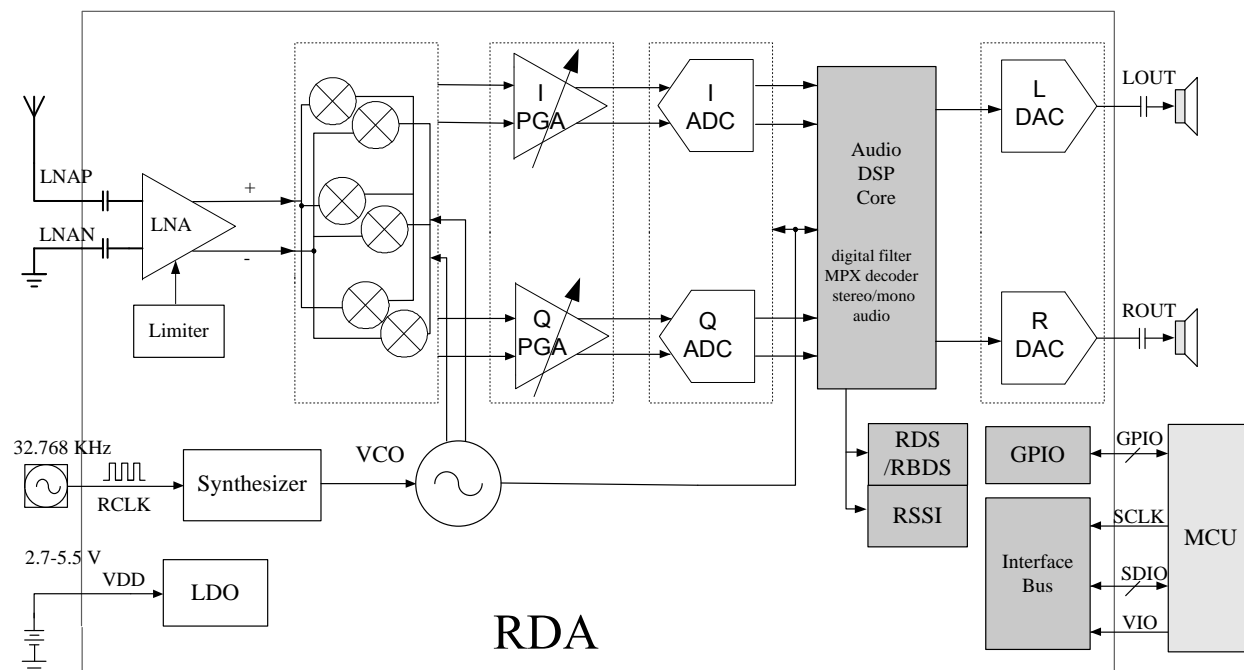


Figure 2-1. RDA5802N FM Tuner Block Diagram

2.1 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (50 to 115MHz), a multi-phase image-reject mixer array, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports (LNAP and LNA) and supports any input port by set according registers bits (LNA_PORT_SEL[1:0]). Its default input common mode voltage is GND.

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The multi-phase mixer array down converts the LNA output differential RF signal to low-IF, it also has image-reject function and harmonic tones rejection.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomously switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

2.2 Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to multi-phase, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 50MHz to 115MHz.

2.3 Power Supply

The RDA5802N integrated one LDO which supplies power to the chip. The external supply voltage range is 1.8-5.5 V.

2.4 RESET and Control Interface select

The RDA5802N is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The RDA5802N only support I²C control interface bus mode.

2.5 Control Interface

The RDA5802N only supports I²C control interface.

The I²C interface is compliant to I²C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I²C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5802N. There is no visible register address in I²C interface transfers. The I²C interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5802N always gives out ACK after every byte,

and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5802N sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5802N will return the bus to MCU, and MCU will give out STOP condition.

2.6 I²S Audio Data Interface

The RDA5802N supports I²S (Inter IC Sound Bus) audio interface. The interface is fully compliant with I²S bus specification. When setting I2SEN bit high, RDA5802N will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I²S master and transmitter, the sample rate is 48Kbps, 44.1kbps, 32kbps,.... RDA5802N also support as I²S slaver mode and transmitter, the sample rate is less than 100kbps.

2.7 GPIO Outputs

The RDA5802N has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST.

Constant low, high or high-Z functionality is available regardless of the state of VDD supplies or the ENABLE bit.

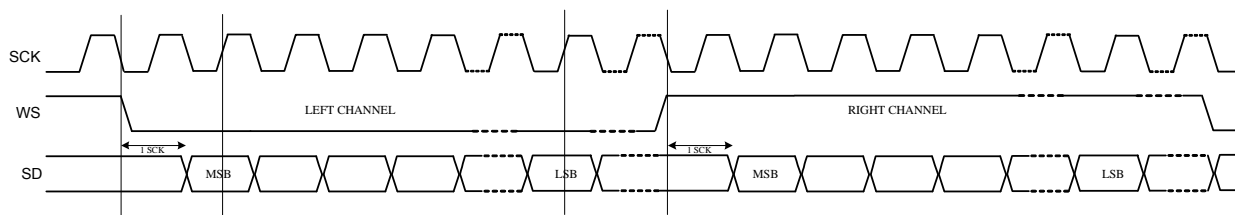


Figure 3-2 I2S Digital Audio Format

3 Electrical Characteristics

Table 3-1 DC Electrical Specification (Recommended Operation Conditions):

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------|---------|---------|---------|------|
| VDD | Supply Voltage | 1.8 | 3.3 | 5.5 | V |
| VIO | Interface Supply Voltage | 1.0 | - | 3.6 | V |
| T _{amb} | Ambient Temperature | -20 | 27 | +75 | °C |
| V _{IL} | CMOS Low Level Input Voltage | 0 | | 0.3*VIO | V |
| V _{IH} | CMOS High Level Input Voltage | 0.7*VIO | | VIO | V |
| V _{TH} | CMOS Threshold Voltage | | 0.5*VIO | | V |

Table 3-2 DC Electrical Specification (Absolute Maximum Ratings):

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------------|------------------------------|------|-----|---------|------|
| VIO | Interface Supply Voltage | -0.5 | | +3.6 | V |
| T _{amb} | Ambient Temperature | -40 | | +90 | °C |
| I _{IN} | Input Current ⁽¹⁾ | -10 | | +10 | mA |
| V _{IN} | Input Voltage ⁽¹⁾ | -0.3 | | VIO+0.3 | V |
| V _{Ina} | LNA FM Input Level | | | +10 | dBm |

Notes:

1. For Pin: SCLK, SDIO

Table 3-3 Power Consumption Specification

(VDD = 3 V, VIO=3 V, T_A = 25 °C, unless otherwise specified)

| SYMBOL | DESCRIPTION | CONDITION | TYP | UNIT |
|------------------|-------------------------------|----------------------|-----|------|
| I _{VDD} | Supply Current ⁽¹⁾ | ENABLE=1 | 20 | mA |
| I _{VDD} | Supply Current ⁽²⁾ | ENABLE=1 | 21 | mA |
| I _{VIO} | Interface Supply Current | SCLK and RCLK active | 60 | μA |
| I _{PD} | Powerdown Current | ENABLE=0 | 5 | μA |
| I _{VIO} | Interface Powerdown Current | ENABLE=0 | 10 | μA |

Notes:

1. For strong input signal condition
2. For weak input signal condition

4 Receiver Characteristics

Table 4-1 Receiver Characteristics

(VDD = 3 V, VIO=3 V, T_A = 25 °C, unless otherwise specified)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNIT | |
|--|---|------------------------|-------------------------|-----|------|----------|--------|---|
| General specifications | | | | | | | | |
| F _{in} | FM Input Frequency Range | Adjust BAND Register | | 50 | | 115 | MHz | |
| V _{rf} | Sensitivity ^{1,2,3} | S/N=26dB | 50MHz | - | 1.4 | 1.8 | μV EMF | |
| | | | 65MHz | - | 1.2 | 1.5 | | |
| | | | 88MHz | - | 1.2 | 1.5 | | |
| | | | 98MHz | - | 1.3 | 1.5 | | |
| | | | 108MHz | - | 1.3 | 1.5 | | |
| | | | 115MHz | - | 1.3 | 1.8 | | |
| IP3 _{in} | Input IP3 ⁴ | AGCD=1 | | 80 | - | - | dBμV | |
| α _{am} | AM Suppression ^{1,2} | m=0.3 | | 60 | - | - | dB | |
| S ₂₀₀ | Adjacent Channel Selectivity | ±200KHz | | 50 | 70 | - | dB | |
| S ₄₀₀ | 400KHz Selectivity | ±400KHz | | 60 | 85 | - | dB | |
| V _{AFL} ; V _{AFR} | Audio L/R Output Voltage ^{1,2} (Pins LOUT and ROUT) | Volume [3:0] =1111 | | - | 360 | - | mV | |
| S/N | Maximum Signal to Noise Ratio ^{1,2,3,5} | | Mono ² | 55 | 57 | - | dB | |
| | | | Stereo ⁶ | 53 | 55 | - | | |
| α _{SCS} | Stereo Channel Separation | | | 35 | - | - | dB | |
| R _L | Audio Output Loading Resistance | Single-ended | | 32 | - | - | Ω | |
| THD | Audio Total Harmonic Distortion ^{1,3,6} | Volume[3:0] =1111 | R _{load} =1K Ω | - | 0.15 | 0.2 | % | |
| | | | R _{load} =32 Ω | - | 0.2 | - | | |
| α _{AOI} | Audio Output L/R Imbalance ^{1,6} | | | - | - | 0.05 | dB | |
| R _{mute} | Mute Attenuation Ratio ¹ | Volume[3:0]=0000 | | 60 | - | - | dB | |
| BW _{audio} | Audio Response ¹ | 1KHz=0dB ±3dB point | Low Freq ⁹ | - | 100 | - | Hz | |
| | | | High Freq | - | 14 | - | | |
| Pins L _{NAN} , L _{NAP} , L _{OUT} , R _{OUT} and NC(22,23) | | | | | | | | |
| V _{com_rfin} | Pins L _{NAN} /L _{NAP} Input Common Mode Voltage | | | | 0 | | V | |
| V _{com} | Audio Output Common Mode Voltage ⁸ | | | | 1.0 | 1.05 | 1.1 | V |
| V _{com_nc} | Pins NC (22,23) Common Mode Voltage | | | | | Floating | | V |

Notes: 1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;

2. Δf=22.5KHz; 3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz;

5. P_{RF}=60dBμV; 6. Δf=75KHz, fpilot=10%

8. At LOUT and ROUT pins

4. |f₂-f₁|>1MHz, f₀=2xf₁-f₂, AGC disable, F_{in}=76 to 108MHz;

7. Measured at V_{EMF} = 1 mV, f_{RF} = 65 to 108MHz

9. Adjustable

5 Serial Interface

5.1 I²C Interface Timing

Table 5-1 I²C Interface Timing Characteristics

(VDD = 3 V, VIO=3 V, T_A = 25 °C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---------------------------------|---------------------------------------|----------------|----------------------|-----|-----|------|
| SCLK Frequency | f _{scl} | | 0 | - | 400 | KHz |
| SCLK High Time | t _{high} | | 0.6 | - | - | μs |
| SCLK Low Time | t _{low} | | 1.3 | - | - | μs |
| Setup Time for START Condition | t _{su:sta} | | 0.6 | - | - | μs |
| Hold Time for START Condition | t _{hd:sta} | | 0.6 | - | - | μs |
| Setup Time for STOP Condition | t _{su:sto} | | 0.6 | - | - | μs |
| SDIO Input to SCLK↑ Setup | t _{su:dat} | | 100 | - | - | ns |
| SDIO Input to SCLK↓ Hold | t _{hd:dat} | | 0 | - | 900 | ns |
| STOP to START Time | t _{buf} | | 1.3 | - | - | μs |
| SDIO Output Fall Time | t _{f,out} | | 20+0.1C _b | - | 250 | ns |
| SDIO Input, SCLK Rise/Fall Time | t _{r,in} / t _{f,in} | | 20+0.1C _b | - | 300 | ns |
| Input Spike Suppression | t _{sp} | | - | - | 50 | ns |
| SCLK, SDIO Capacitive Loading | C _b | | - | - | 50 | pF |
| Digital Input Pin Capacitance | | | | | 5 | pF |

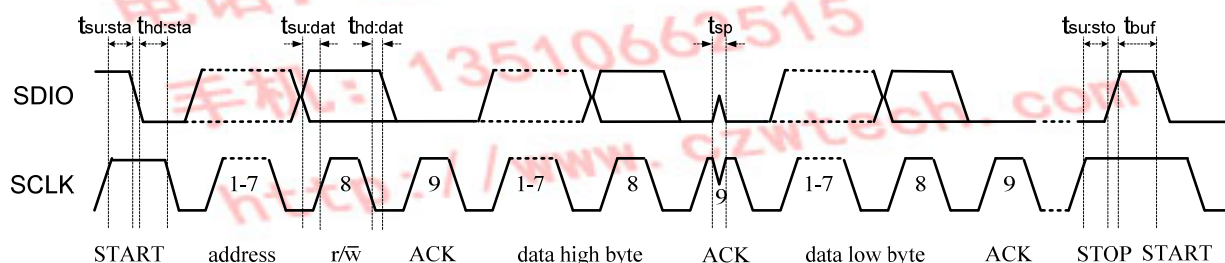


Figure 5-1. I²C Interface Write Timing Diagram

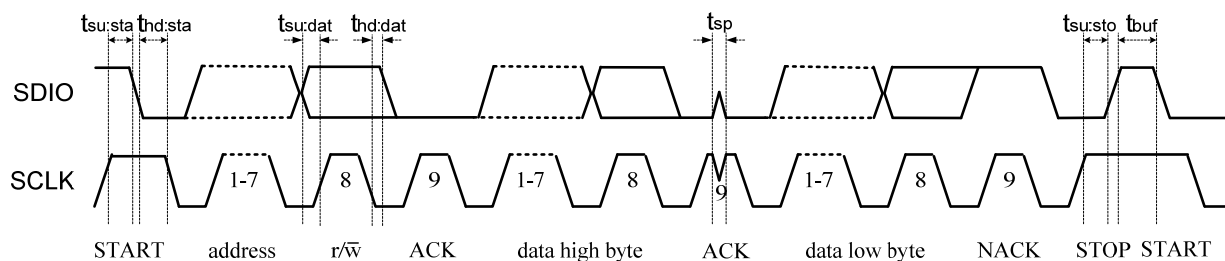


Figure 5-2. I²C Interface Read Timing Diagram

6 Register Definition

| REG | BITS | NAME | FUNCTION | DEFAULT |
|-----|------|-------------------------|---|---------|
| 00H | 15:8 | CHIPID[7:0] | Chip ID. | 0x58 |
| 02H | 15 | DHIZ | Audio Output High-Z Disable. <i>0 = High impedance; 1 = Normal operation</i> | 0 |
| | 14 | DMUTE | Mute Disable. <i>0 = Mute; 1 = Normal operation</i> | 0 |
| | 13 | MONO | Mono Select. <i>0 = Stereo; 1 = Force mono</i> | 0 |
| | 12 | BASS | Bass Boost. <i>0 = Disabled; 1 = Bass boost enabled</i> | 0 |
| | 11 | RCLK NON-CALIBRATE MODE | 0=RCLK clock is always supply 1=RCLK clock is not always supply when FM work (when 1, RDA5802N can't directly support -20 °C ~70 °C temperature. Only supply $\pm 20^{\circ}\text{C}$ temperature swing from tune point) | 0 |
| | 10 | RCLK DIRECT INPUT MODE | 1=RCLK clock use the directly input mode | 0 |
| | 9 | SEEKUP | Seek Up. <i>0 = Seek down; 1 = Seek up</i> | 0 |
| | 8 | SEEK | Seek. <i>0 = Disable stop seek; 1 = Enable</i> Seek begins in the direction specified by SEEKUP and ends when a channel is found, or the entire band has been searched. The SEEK bit is set low and the STC bit is set high when the seek operation completes. | 0 |
| | 7 | SKMODE | Seek Mode 0 = wrap at the upper or lower band limit and continue seeking 1 = stop seeking at the upper or lower band limit | 0 |
| | 6:4 | CLK_MODE[2:0] | 000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz | 000 |
| | 3 | RDS_EN | RDS/RBDS enable If 1, rds/rbds enable | 0 |
| | 2 | NEW_METHOD | New Demodulate Method Enable, can improve the receive sensitivity about 1dB. | 0 |
| | 1 | SOFT_RESET | Soft reset. If 0, not reset; If 1, reset. | 0 |
| | 0 | ENABLE | Power Up Enable. <i>0 = Disabled; 1 = Enabled</i> | 0 |

| REG | BITS | NAME | FUNCTION | DEFAULT |
|-----|------|-------------|--|---------|
| 03H | 15:6 | CHAN[9:0] | Channel Select. BAND = 0 Frequency = Channel Spacing (kHz) x CHAN+ 87.0 MHz BAND = 1 or 2 Frequency = Channel Spacing (kHz) x CHAN + 76.0 MHz BAND = 3 Frequency = Channel Spacing (kHz) x CHAN + 65.0 MHz CHAN is updated after a seek operation. | 0x00 |
| | 5 | DIRECT MODE | Directly Control Mode, Only used when test. | 0 |
| | 4 | TUNE | Tune 0 = Disable 1 = Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The tune bit is reset to low automatically when the tune operation completes.. | 0 |
| | 3:2 | BAND[1:0] | Band Select. 00 = 87–108 MHz (US/Europe) 01 = 76–91 MHz (Japan) 10 = 76–108 MHz (world wide) 11 ¹ = 65 –76 MHz (East Europe) or 50-65MHz | 00 |
| | 1:0 | SPACE[1:0] | Channel Spacing. 00 = 100 kHz 01 = 200 kHz 10 = 50kHz 11 = 25KHz | 00 |
| 04H | 15 | RDSIEN | RDS ready Interrupt Enable. 0 = Disable Interrupt 1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs. | 0 |
| | 14 | STCIEN | Seek/Tune Complete Interrupt Enable. 0 = Disable Interrupt 1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs. | 0 |
| | 13 | RBDS | 1 = RBDS mode enable 0 = RDS mode only | 0 |
| | 12 | RDS_FIFO_EN | 1 = RDS fifo mode enable. | 0 |
| | 11 | DE | De-emphasis. 0 = 75 μ s; 1 = 50 μ s | 0 |
| | 10 | RSVD | Reserved | |

¹ If 0x07h_bit[9](band)=1, 65-76MHz; =0, 50-76MHz

| REG | BITS | NAME | FUNCTION | DEFAULT |
|-----|-------|--------------------------|---|---------|
| | 9 | SOFTMUTE_EN | If 1, softmute enable | 1 |
| | 8 | AFCD | AFC disable. If 0, afc work; If 1, afc disabled. | 0 |
| | 7 | RSVD | Reserved | |
| | 6 | I2S_ENABLED | I2S bus enable If 0, disabled; If 1, enabled. | 0 |
| | 5:4 | GPIO3[1:0] | General Purpose I/O 3. 00 = High impedance 01 = Mono/Stereo indicator (ST) 10 = Low 11 = High | 00 |
| | 3:2 | GPIO2[1:0] | General Purpose I/O 2. 00 = High impedance 01 = Interrupt (INT) 10 = Low 11 = High | 00 |
| | 1:0 | GPIO1[1:0] | General Purpose I/O 1. 00 = High impedance 01 = Reserved 10 = Low 11 = High | 00 |
| 05H | 15 | INT_MODE | If 0, generate 5ms interrupt; If 1, interrupt last until read reg0CH action occurs. | 1 |
| | 14:13 | SEEK_MODE[1:0] | RDA5802N Seek Mode Select | 00 |
| | 12 | RSVD | Reserved | 0 |
| | 11:8 | SEEKTH[3:0] ² | Seek SNR threshold value: Noise_th(dB) = 79 – seek_th | 1000 |
| | 7:6 | LNA_PORT_SEL[1:0] | LNA input port selection bit: 00: no input 01: LNAN 10: LNAP 11: dual port input | 10 |
| | 5:4 | RSVD | Reserved | 00 |
| | 3:0 | VOLUME[3:0] | DAC Gain Control Bits (Volume). 0000=min; 1111=max Volume scale is logarithmic When 0000, output mute and output impedance is very large | 1111 |
| 06H | 15 | RSVD | reserved | 0 |
| | 14:13 | OPEN_MODE[1:0] | Open reserved register mode. 11=open behind registers writing function others: only open behind registers reading function | 00 |
| | 12 | I2S_MODE ³ | If 0, master mode; If 1, slave mode. | 0 |

² The default noise threshold is 71dB

³ This function is open when I2S_Enabled=1.

| REG | BITS | NAME | FUNCTION | DEFAULT |
|-----|-------|--|--|---------|
| | 11 | SW_LR ³ | Ws relation to l/r channel. If 0, ws=0 ->r, ws=1 ->l; If 1, ws=0 ->l, ws=1 ->r. | 10 |
| | 10 | SCLK_I_EDGE ³ | When I2S enable If 0, use normal sclk internally; If 1, invert sclk internally. | 0 |
| | 9 | DATA_SIGNED ³ | If 0, I2S output unsigned 16-bit audio data. If 1, I2S output signed 16-bit audio data. | 0 |
| | 8 | WS_I_EDGE ³ | If 0, use normal ws internally; If 1, invert ws internally. | 0 |
| | 7:4 | I2S_SW_CNT[4:0] ³ Only valid in master mode | 4'b1000: WS_STEP_48; 4'b0111: WS_STEP=44.1kbps; 4'b0110: WS_STEP=32kbps; 4'b0101: WS_STEP=24kbps; 4'b0100: WS_STEP=22.05kbps; 4'b0011: WS_STEP=16kbps; 4'b0010: WS_STEP=12kbps; 4'b0001: WS_STEP=11.025kbps; 4'b0000: WS_STEP=8kbps; | 0000 |
| | 3 | SW_O_EDGE ³ | If 1, invert ws output when as master. | 0 |
| | 2 | SCLK_O_EDGE ³ | If 1, invert sclk output when as master. | 0 |
| | 1 | L_DELY ³ | If 1, L channel data delay 1T. | 0 |
| | 0 | R_DELY ³ | If 1, R channel data delay 1T. | 0 |
| 07H | 15 | RSVD | Reserved | 0 |
| | 14:10 | TH_SOFRBLEND[5:0] | Threshold for noise soft blend setting, unit 2dB | 10000 |
| | 9 | 65M_50M MODE | Valid when band[1:0] = 2'b11 (0x03H_bit<3:2>) 1 = 65~76 MHz; 0 = 50~76 MHz. | 1 |
| | 8 | RSVD | Reserved | 0 |
| | 7:2 | SEEK_TH_OLD ⁴ | Seek threshold for old seek mode, Valid when Seek_Mode=01 | 000000 |
| | 1 | SOFTBLEND_EN | If 1, Softblend enable | 1 |
| | 0 | FREQ_MODE | If 1, then freq setting changed. Freq = 76000(or 87000) kHz + freq_direct (08H) kHz. | 0 |
| 0AH | 15 | RDSR | RDS ready 0 = No RDS/RBDS group ready(default) 1 = New RDS/RBDS group ready | 0 |
| | 14 | STC | Seek/Tune Complete. 0 = Not complete 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes. | 0 |
| | 13 | SF | Seek Fail. 0 = Seek successful; 1 = Seek failure The seek fail flag is set when the seek operation fails to find a channel with an RSSI level greater than SEEKTH[5:0]. | 0 |
| | 12 | RDSS | RDS Synchronization | 0 |

⁴ 0x05H_bit[14:13], SEEK_MODE register. Default value is 00; When = 01, will add the 5802E seek mode.

| REG | BITS | NAME | FUNCTION | DEFAULT |
|-----|------|---------------|---|---------|
| | | | 0 = RDS decoder not synchronized(default) 1 = RDS decoder synchronized Available only in RDS Verbose mode | |
| | 11 | BLK_E | When RDS enable: 1 = Block E has been found 0 = no Block E has been found | 0 |
| | 10 | ST | Stereo Indicator. 0 = Mono; 1 = Stereo Stereo indication is available on GPIO3 by setting GPIO3[1:0] = 01. | 1 |
| | 9:0 | READCHAN[9:0] | Read Channel. BAND = 0 Frequency = Channel Spacing (kHz) x READCHAN[9:0] + 87.0 MHz BAND = 1 or 2 Frequency = Channel Spacing (kHz) x READCHAN[9:0] + 76.0 MHz BAND = 3 Frequency = Channel Spacing (kHz) x READCHAN[9:0] + 65.0 MHz READCHAN[9:0] is updated after a tune or seek operation. | 8'h00 |
| 0BH | 15:9 | RSSI[6:0] | RSSI. 000000 = min 111111 = max RSSI scale is logarithmic. | 0 |
| | 8 | FM TRUE | 1 = the current channel is a station 0 = the current channel is not a station | 0 |
| | 7 | FM_READY | 1=ready 0=not ready | 0 |
| | 6:5 | RSVD | Reserved | 00 |
| | 4 | ABCD_E | 1= the block id of register 0cH, 0dH, 0eH, 0fH is E 0= the block id of register 0cH, 0dH, 0eH, 0fH is A, B, C, D | 0 |
| | 3:2 | BLERA[1:0] | Block Errors Level of RDS_DATA_0, and is always read as Errors Level of RDS BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1) 00= 0 errors requiring correction 01= 1~2 errors requiring correction 10= 3~5 errors requiring correction 11= 6+ errors or error in checkword, correction not possible. Available only in RDS Verbose mode | 00 |
| | 1:0 | BLERB[1:0] | Block Errors Level of RDS_DATA_1, and is always read as Errors Level of RDS BLOCK B (in RDS mode) or E (in RBDS mode when ABCD_E flag is 1). 00= 0 errors requiring correction 01= 1~2 errors requiring correction | 00 |

| REG | BITS | NAME | FUNCTION | DEFAULT |
|-----|------|------------|---|----------|
| | | | 10= 3~5 errors requiring correction 11= 6+ errors or error in checkword, correction not possible. Available only in RDS Verbose mode | |
| 0CH | 15:0 | RDSA[15:0] | BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1) | 16'h5803 |
| 0DH | 15:0 | RDSB[15:0] | BLOCK B (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1) | 16'h5804 |
| 0EH | 15:0 | RDSC[15:0] | BLOCK C (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1) | 16'h5808 |
| 0FH | 15:0 | RDSD[15:0] | BLOCK D (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1) | 16'h5804 |

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8 Pins Description

8.1 RDA5802N Pins Description

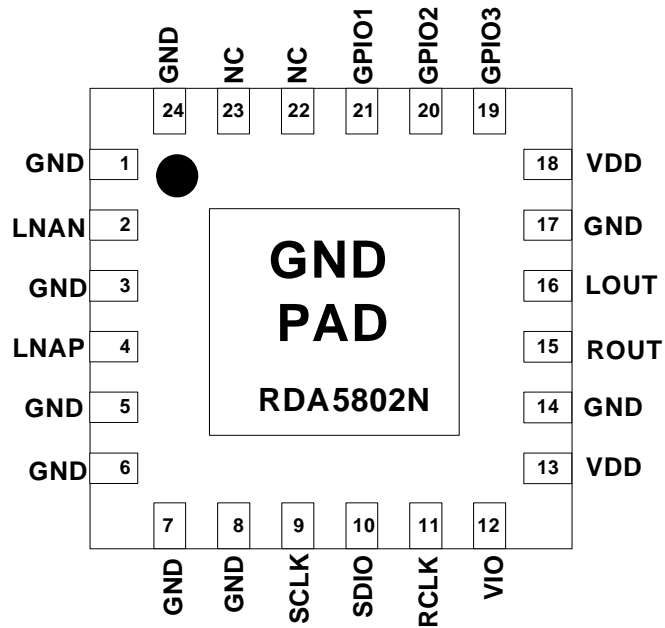


Figure 8-1. RDA5802N Top View

Table 8-1 RDA5802N Pins Description

| SYMBOL | PIN | DESCRIPTION |
|---------------------|-------------------------|--|
| GND | 1,3,5,6,7,8,14,17,24,25 | Ground. Connect to ground plane on PCB |
| LNAN, LNAP | 2,4 | LNA dual input port. |
| SCLK | 9 | Clock input for serial control bus |
| SDIO | 10 | Data input/output for serial control bus |
| RCLK | 11 | 32.768KHz crystal oscillator and reference clock input |
| VIO | 12 | Power supply for I/O |
| VDD | 13,18 | Power supply |
| ROUT, LOUT | 15,16 | Right/Left audio output |
| GPIO1, GPIO2, GPIO3 | 21,20,19 | General purpose input/output |
| NC | 22,23 | No Connect |

8.2 RDA5802NS Pins Description

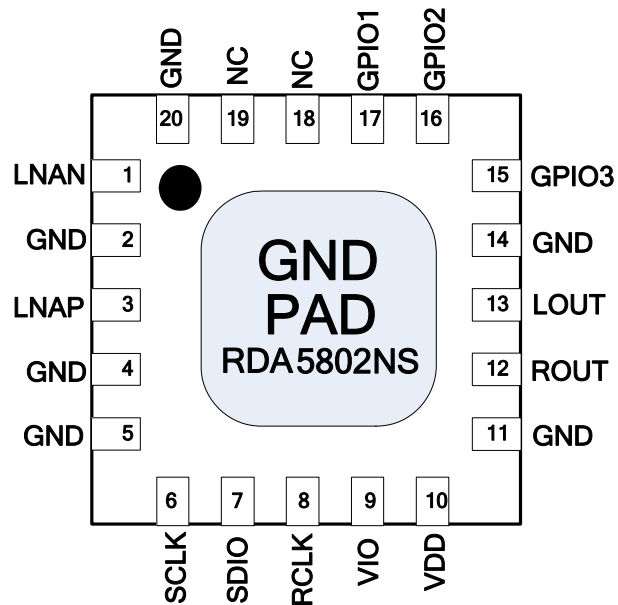


Figure 8-2. RDA5802NS Top View

Table 8-2 RDA5802NS Pins Description

| SYMBOL | PIN | DESCRIPTION |
|---------------------|-------------------|--|
| GND | 2,4,5,11,14,20,21 | Ground. Connect to ground plane on PCB |
| LNAN, LNAP | 1,3 | LNA dual input port. |
| SCLK | 6 | Clock input for serial control bus |
| SDIO | 7 | Data input/output for serial control bus |
| RCLK | 8 | 32.768KHz crystal oscillator and reference clock input |
| VIO | 9 | Power supply for I/O |
| VDD | 10 | Power supply |
| ROUT, LOUT | 12,13 | Right/Left audio output |
| GPIO1, GPIO2, GPIO3 | 15,16,17 | General purpose input/output |
| NC | 18,19 | No Connect |

8.3 RDA5802NM Pins Description

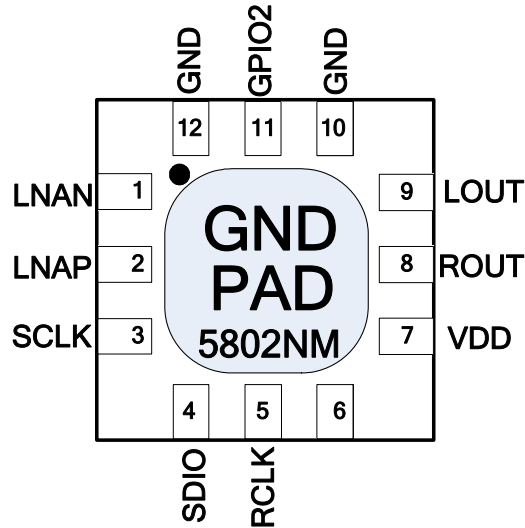


Figure 8-3. RDA5802NM Top View

Table 8-3 RDA5802NM Pins Description

| SYMBOL | PIN | DESCRIPTION |
|------------|----------|--|
| GND | 10,12,13 | Ground. Connect to ground plane on PCB |
| LNAN, LNAP | 1,2 | LNA dual input port. |
| SCLK | 3 | Clock input for serial control bus |
| SDIO | 4 | Data input/output for serial control bus |
| RCLK | 5 | 32.768KHz crystal oscillator and reference clock input |
| VIO | 6 | Power supply for I/O |
| VDD | 7 | Power supply |
| ROUT, LOUT | 8,9 | Right/Left audio output |
| GPIO2 | 11 | General purpose input/output |

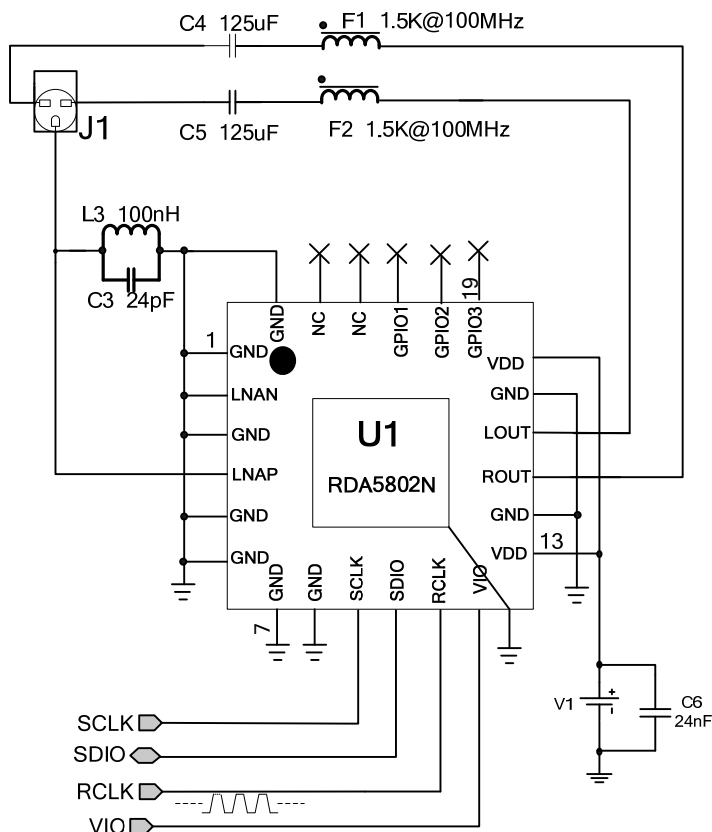
Table 8-4 Internal Pin Configuration

| SYMBOL | PIN | DESCRIPTION |
|-------------------|---|-------------|
| LNAN/LNAP | 2/4(RDA5802N) 1/3 (RDA5802NS) 1/2 (RDA5802NM) | |
| RCLK | 11 (RDA5802N) 8 (RDA5802NS) 5 (RDA5802NM) | |
| SCLK/SDIO | 9/10 (RDA5802N) 6/7 (RDA5802NS) 3/4 (RDA5802NM) | |
| GPIO1/GPIO2/GPIO3 | 21/20/19(RDA5802N) 17/16/15(RDA5802NS) 11(RDA5802NM) ⁵ | |

⁵ Only include GPIO2

9 Application Diagram

9.1 RDA5802N Common Application :



Notes:

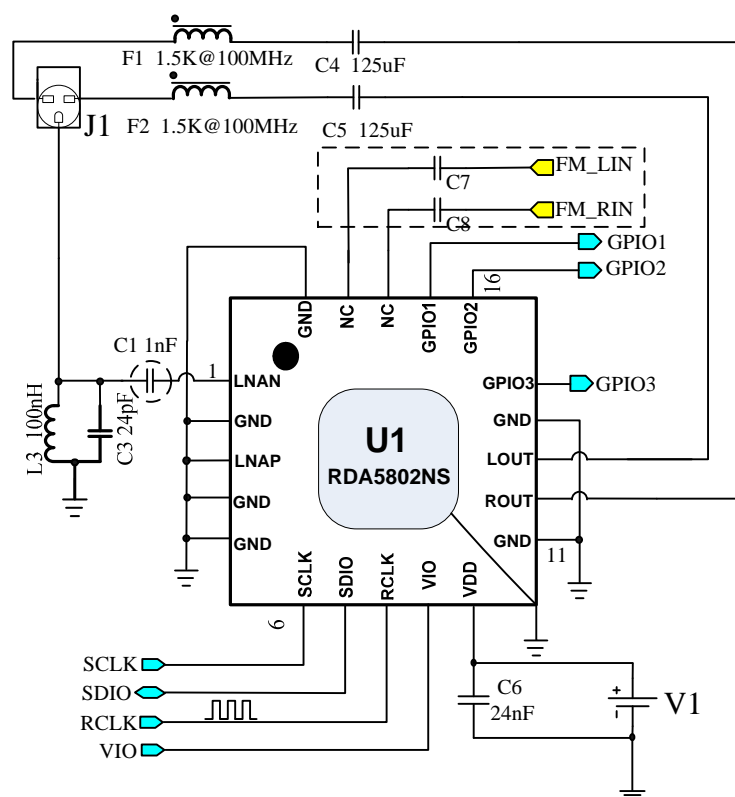
1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802N Chip;
3. V1: Power Supply (1.8~5.5V);
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
5. Pins NC(22,23) can be Leaved floating ;
6. Place C6 Close to 5802N pin13.
7. Ferrite F1/F2 should close to J1.

Figure 9-1. RDA5802N FM Tuner Application Diagram (TCXO Application)

9.1.1 Bill of Materials:

| COMPONENT | VALUE | DESCRIPTION | SUPPLIER |
|-----------|-------------|---------------------------------|----------|
| U1 | RDA5802N | Broadcast FM Radio Tuner | RDA |
| J1 | | Common 32Ω Resistance Headphone | |
| L3/C3 | 100nH/24pF | LC Chock for LNA Input | Murata |
| C4,C5 | 125μF | Audio AC Couple Capacitors | Murata |
| C6 | 22nF | Power Supply Bypass Capacitor | Murata |
| F1/F2 | 1.5K@100MHz | FM Band Ferrite | Murata |

9.2 RDA5802NS Common Application⁶:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802NS Chip;
3. V1: Power Supply (1.8~5.5V);
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
5. Pins NC(18,19), can be leaved floating or place capacitor C7/C8 ;
6. Place C6 Close to 5802NS pin10.
7. Ferrite F1/F2 should close to J1.

C1: Ac couple cap for compatible RDA5820NS

C7 & C8: Audio input couple cap for FM transmit

● PIN1 (LNA) is receive/transmit dual port for RDA5820NS

Figure 9-2. RDA5802NS FM Tuner Application Diagram (TCXO Application)

9.2.1 Bill of Materials:

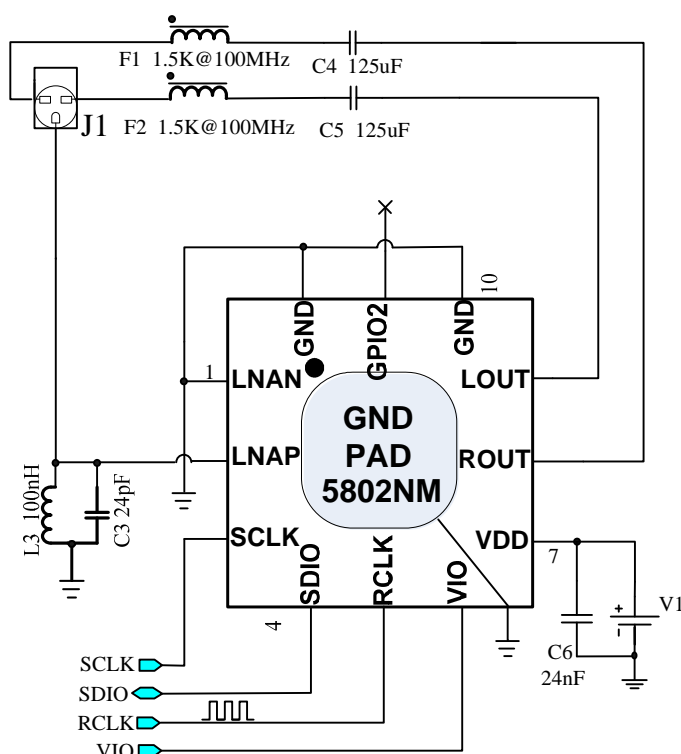
| COMPONENT | VALUE | DESCRIPTION | SUPPLIER |
|--------------------|-------------|---------------------------------|----------|
| U1 | RDA5802NS | Broadcast FM Radio Tuner | RDA |
| J1 | | Common 32Ω Resistance Headphone | |
| L3/C3 | 100nH/24pF | LC Chock for LNA Input | Murata |
| C4,C5 | 125μF | Audio AC Couple Capacitors | Murata |
| C6 | 22nF | Power Supply Bypass Capacitor | Murata |
| F1/F2 | 1.5K@100MHz | FM Band Ferrite | Murata |
| C1 ⁷ | 1nF | AC Couple Capacitor | Murata |
| C7/C8 ⁸ | 0.22uF | Audio Couple Capacitors | Murata |

⁶ Pin-to-pin compatible with RDA5820NS. RDA5820NS is the newest generation FM receive/transmit tuner.

⁷ C1 can be instead by 00hm resistor if not need compatible with RDA5802NS

⁸ C7/C8 can be floating if not need compatible with RDA5820NS

9.3 RDA5802NM Common Application:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802NM Chip;
3. V1: Power Supply (1.8~5.5V);
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
5. Place C6 Close to 5802NM pin7.
6. Ferrite F1/F2 should close to J1.

Figure 9-3. RDA5802NM FM Tuner Application Diagram (TCXO Application)

9.3.1 Bill of Materials:

| COMPONENT | VALUE | DESCRIPTION | SUPPLIER |
|-----------|-------------|---------------------------------|----------|
| U1 | RDA5802NM | Broadcast FM Radio Tuner | RDA |
| J1 | | Common 32Ω Resistance Headphone | |
| L3/C3 | 100nH/24pF | LC Chock for LNA Input | Murata |
| C4,C5 | 125μF | Audio AC Couple Capacitors | Murata |
| C6 | 22nF | Power Supply Bypass Capacitor | Murata |
| F1/F2 | 1.5K@100MHz | FM Band Ferrite | Murata |

10 Physical Dimension

10.1 RDA5802N Physical Dimension

Figure 10-1 illustrates the package details for the RDA5802N. The package is lead-free and RoHS-compliant.

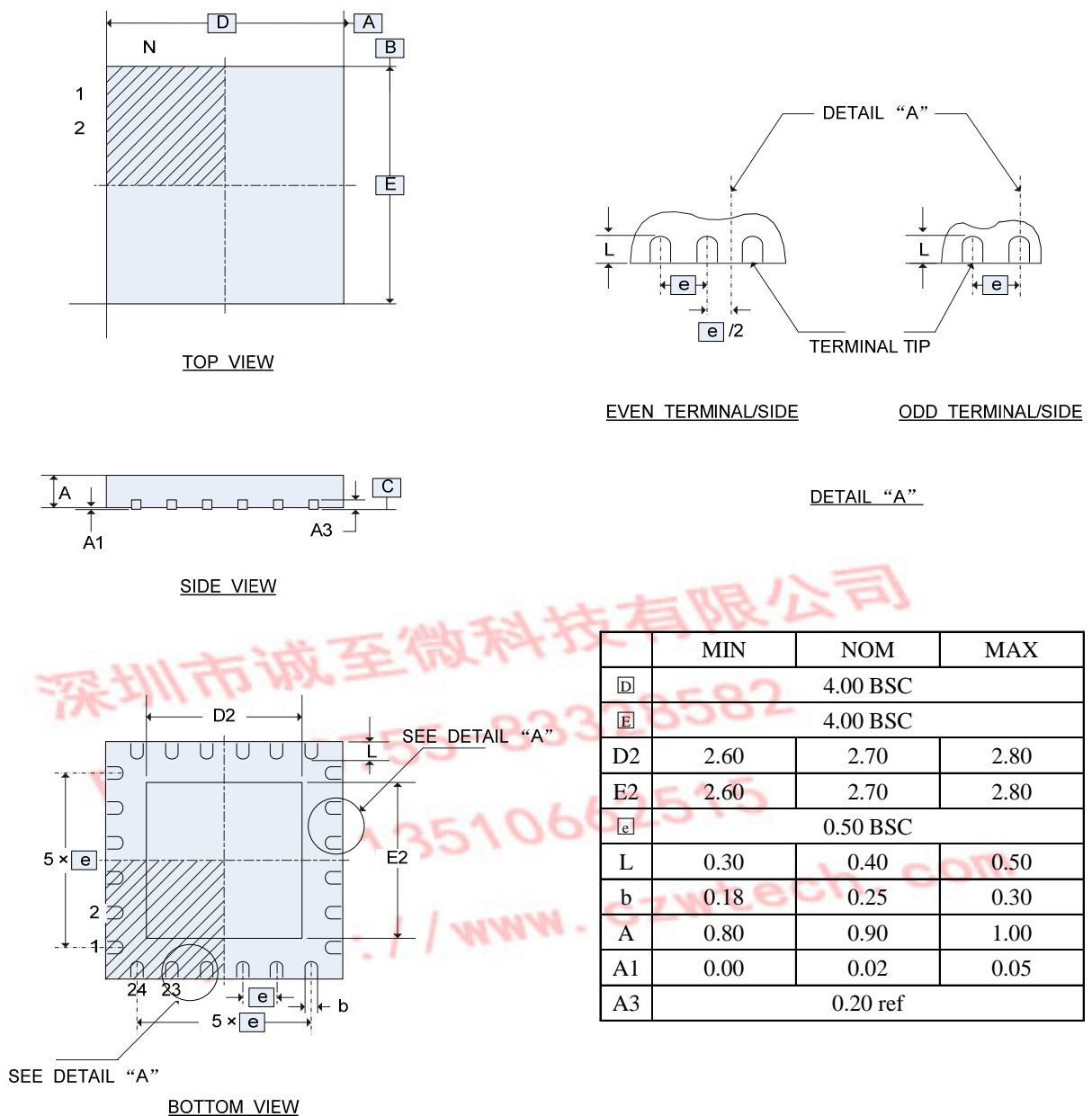


Figure 10-1. 24-Pin 4x4 Quad Flat No-Lead (QFN)

10.2 RDA5802NS Physical Dimension

Figure 10-2 illustrates the package details for the RDA5802NS. The package is lead-free and RoHS-compliant.

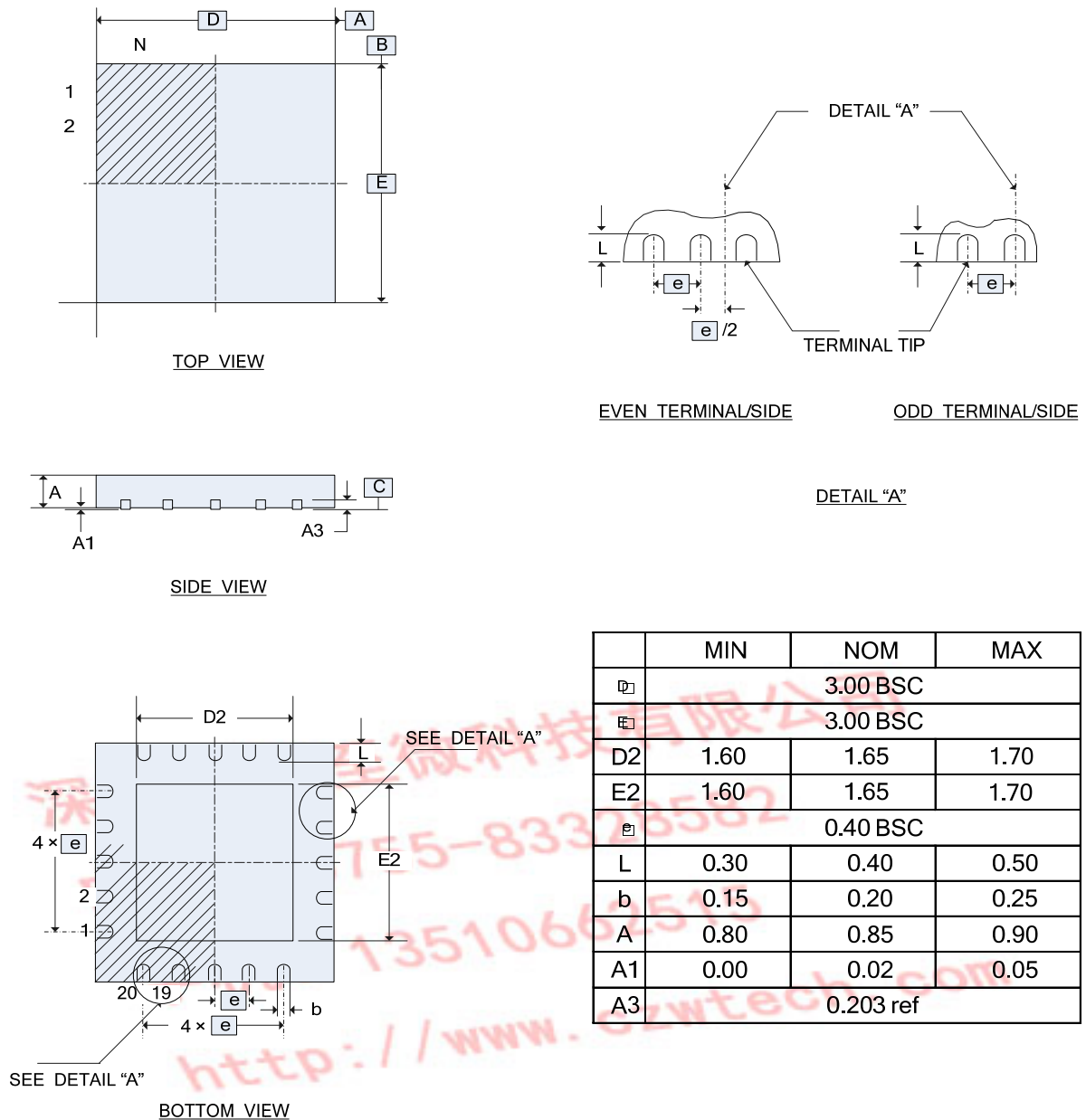
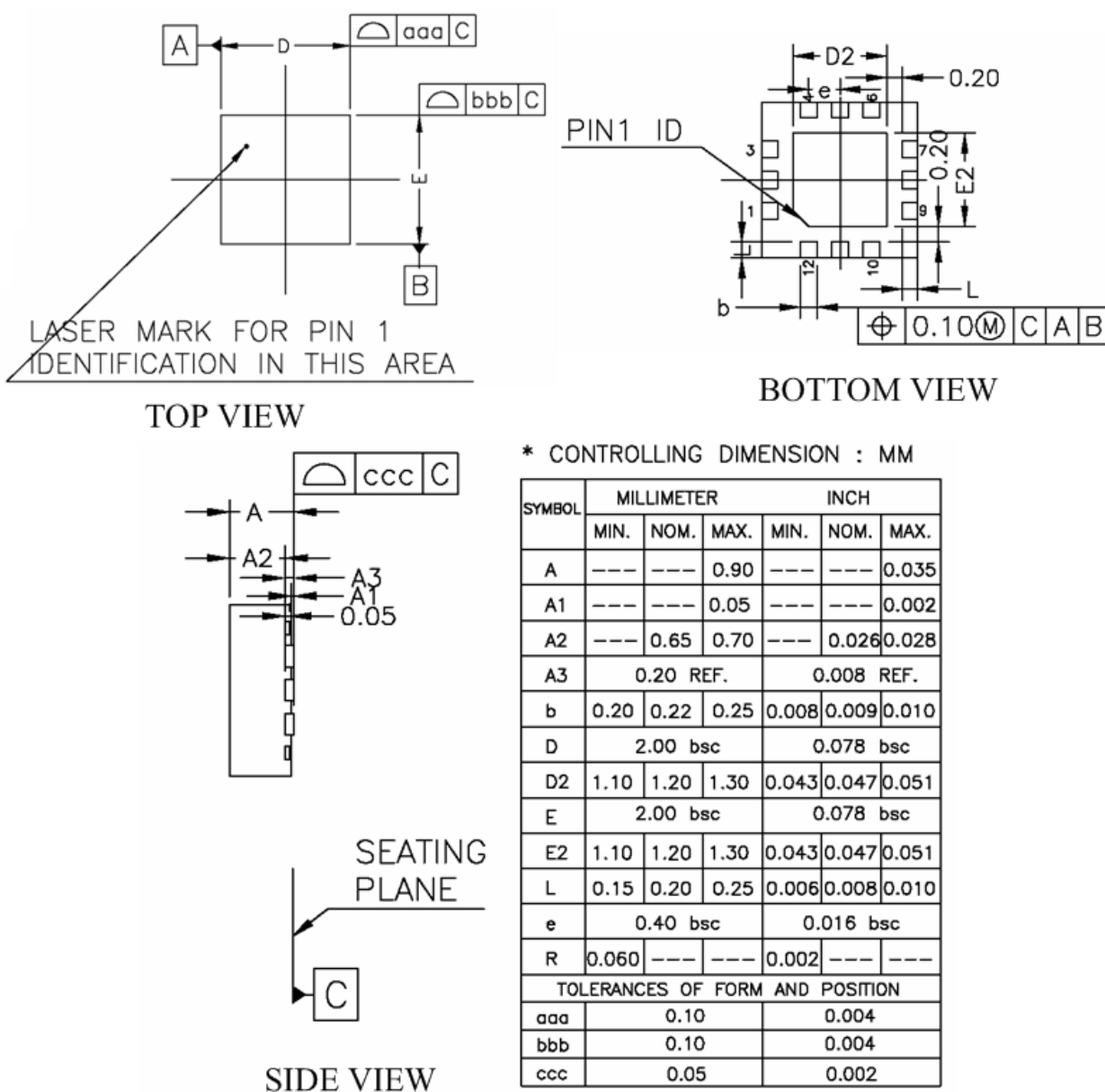


Figure 10-2. 20-Pin 3x3 Quad Flat No-Lead (QFN)

10.3 RDA5802NM Physical Dimension

Figure 10-3 illustrates the package details for the RDA5802NM. The package is lead-free and RoHS-compliant.



NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM (0.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.

Figure 10-3. 12-Pin 2x2 Quad Flat No-Lead (QFN)

11 PCB Land Pattern

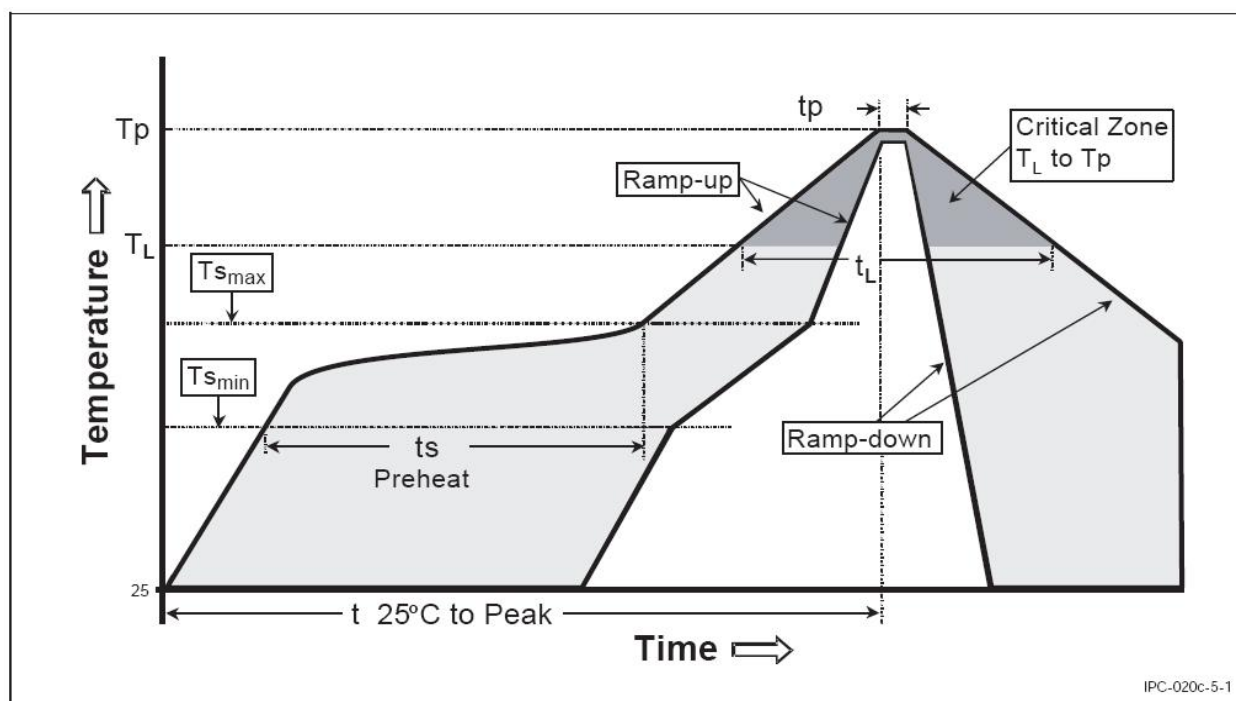


Figure 18. Classification Reflow Profile

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|--|------------------------------------|------------------------------------|
| Average Ramp-Up Rate (T_{smax} to T_p) | 3 °C/second max. | 3 °C/second max. |
| Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax}) | 100 °C 100 °C 60-120 seconds | 150 °C 200 °C 60-180 seconds |
| Time maintained above: -Temperature (T_L) -Time (t_L) | 183 °C 60-150seconds | 217°C 60-150 seconds |
| Peak /Classification Temperature(T_p) | See Table-II | See Table-III |
| Time within 5 °C of actual Peak Temperature (t_p) | 10-30 seconds | 20-40 seconds |
| Ramp-Down Rate | 6 °C/second max. | 6 °C/seconds max. |
| Time 25 °C to Peak Temperature | 6 minutes max. | 8 minutes max. |

Table-I Classification Reflow Profiles

| Package Thickness | Volume mm ³ <350 | Volume mm ³ ≥350 |
|-------------------|--------------------------------|--------------------------------|
| <2.5mm | 240 + 0/-5 °C | 225 + 0/-5 °C |
| ≥2.5mm | 225 + 0/-5 °C | 225 + 0/-5 °C |

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

| Package Thickness | Volume mm ³ <350 | Volume mm ³ 350-2000 | Volume mm ³ >2000 |
|---|--------------------------------|------------------------------------|---------------------------------|
| <1.6mm | 260 + 0 °C * | 260 + 0 °C * | 260 + 0 °C * |
| 1.6mm – 2.5mm | 260 + 0 °C * | 250 + 0 °C * | 245 + 0 °C * |
| ≥2.5mm | 250 + 0 °C * | 245 + 0 °C * | 245 + 0 °C * |
| *Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level. | | | |

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

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12 Change List

| REV | DATE | AUTHER | CHANGE DESCRIPTION |
|------|------------|----------------------|------------------------------------|
| V1.0 | 2011-02-09 | Chun Zhao, Yanan Liu | Original Draft. |
| V1.1 | 2011-03-11 | Chun Zhao, Yanan Liu | Correct Some Errors |
| V2.0 | 2011-03-24 | Chun Zhao, Kai Wang | Add QFN4X4mm and QFN2X2mm Packages |

13 Notes:

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