| Signal | Values |
|---|---|
| clk | |
| pc_out | 0104 / 0106 / 0108 / 010a / 010c / 010e / 0110 / 0110 ... |
| mem_address | 0... / 0032 / 0... / 0... / 0... / 013c / 010a / 010c / 010e |
| mem_read | |
| mem_rdata | 6... / baad / ... / 6... / ... / 2... / ... / 6... / ...5220 / ... / 16ff / 03f9 / 0fff |
| mem_write | |
| mem_byte_enable | 3 |
| mem_wdata | ...6... / baad / ... / 6... / ... / 2... / ... / 6... / ...5220 / ... / 16ff / 03f9 / 0fff |
| registers from regfile | 00b0 000d 5220 baad... / 00b0... / 00b0... / 00b0 000d 5220 600d... / 00... / 00b0 000d... |
| [7] | 00b0 |
| [6] | 000d / 60fa / 000d |
| [5] | 5220 |
| [4] | baad / 600d / baad |
| [3] | 0001 / 0000 |
| [2] | 0130 |
| [1] | 00b0 |
| [0] | 0030 |
| cache state | idle... / read_from_pmem / idle_hit / read_from_pmem / idle_hit |
| cpu state | ...s_ldr1 / ...s_ldr1 / ... |

25200 ns    25400 ns    25600 ns    25800 ns    26000 ns

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