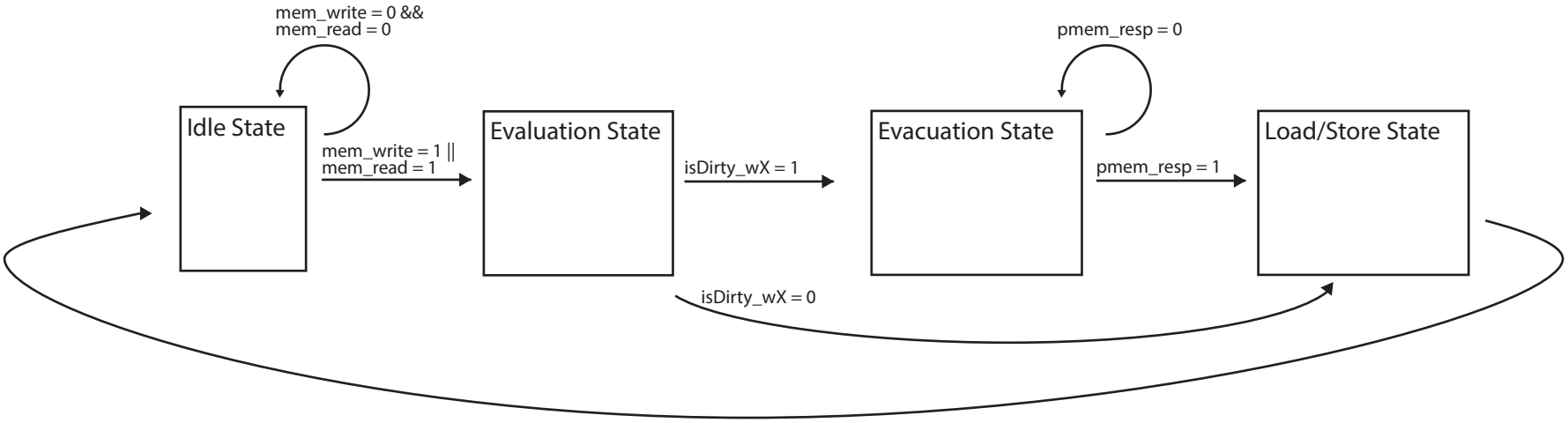

Idle State:
sits spinning setting all load signals to zero until there is a read or write signal from the CPU.

Evaluation State:
Determines the next state based on set register values and inputs from the CPU, like whether it is read/write, and the values from the address parsing. IE: TAG/SET/OFFSET

Mainly, determines if an evacuation is needed or not.

Evacuation State:

If there is a miss, when loading and the valid+dirty bits are High (for LRU way), then we need to evacuate before loading data in from mem.

If there is a miss, when storing and the valid+dirty bits are High (for LRU way), then we need to evacuate before loading data in from mem.

Load/Store:
Execute load and store operations directly with the cache data stores. No memory access in this state.

In the case of a store, we set the values in the data store and set the dirty bit to high. The next time we need to replace, we will need to evacuate (write back)

Cache Control

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MP2.1