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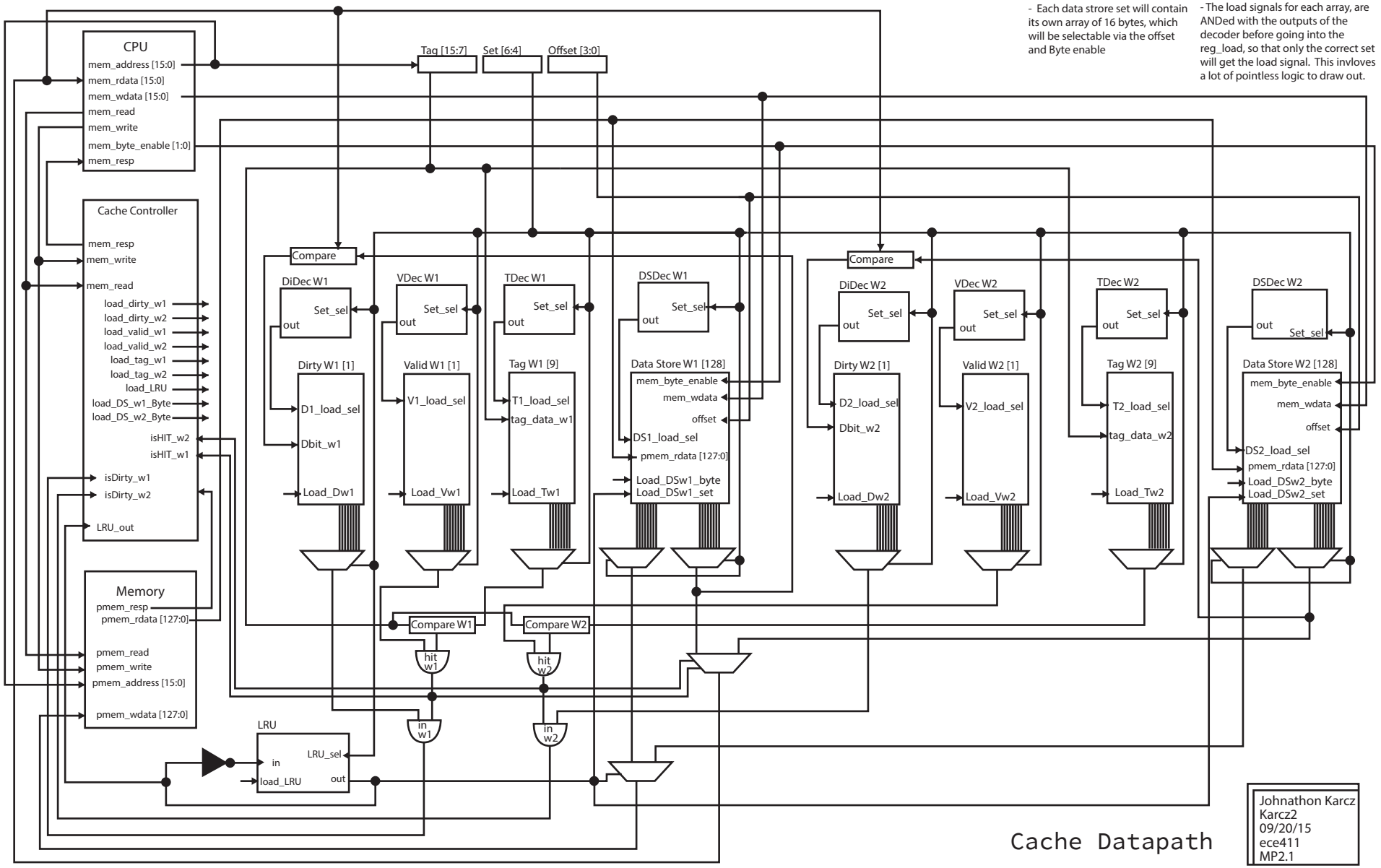
ECE411
MP2.1
09/22/2015


Notes:
- Each data strore set will contain its own array of 16 bytes, which will be selectable via the offset and Byte enable
- The load signals for each array, are ANDed with the outputs of the decoder before going into the reg_load, so that only the correct set will get the load signal. This invloves a lot of pointless logic to draw out.
CPU
mem_address [15:0]
mem_rdata [15:0]
mem_wdata [15:0]
mem_read
mem_write
mem_byte_enable [1:0]
mem_resp
Tag [15:7]
Set [6:4]
Offset [3:0]
Cache Controller
mem_resp
mem_write
mem_read
load_dirty_w1
load_dirty_w2
load_valid_w1
load_valid_w2
load_tag_w1
load_tag_w2
load_LRU
load_DS_w1_Byte
load_DS_w2_Byte
isHIT_w2
isHIT_w1
isDirty_w1
isDirty_w2
LRU_out
Memory
pmem_resp
pmem_rdata [127:0]
pmem_read
pmem_write
pmem_address [15:0]
pmem_wdata [127:0]
Compare
DiDec W1
Set_sel
out
Dirty W1 [1]
D1_load_sel
Dbit_w1
Load_Dw1
VDec W1
Valid W1 [1]
V1_load_sel
Load_Vw1
TDec W1
Tag W1 [9]
T1_load_sel
tag_data_w1
Load_Tw1
DSDec W1
Data Store W1 [128]
mem_byte_enable
mem_wdata
offset
DS1_load_sel
pmem_rdata [127:0]
Load_DSw1_byte
Load_DSw1_set
Compare
DiDec W2
Dirty W2 [1]
D2_load_sel
Dbit_w2
Load_Dw2
VDec W2
Valid W2 [1]
V2_load_sel
Load_Vw2
TDec W2
Tag W2 [9]
T2_load_sel
tag_data_w2
Load_Tw2
DSDec W2
Data Store W2 [128]
mem_byte_enable
mem_wdata
offset
DS2_load_sel
pmem_rdata [127:0]
Load_DSw2_byte
Load_DSw2_set
Compare W1
Compare W2
hit w1
hit w2
in w1
in w2
LRU
in
load_LRU
LRU_sel
out
Cache Datapath
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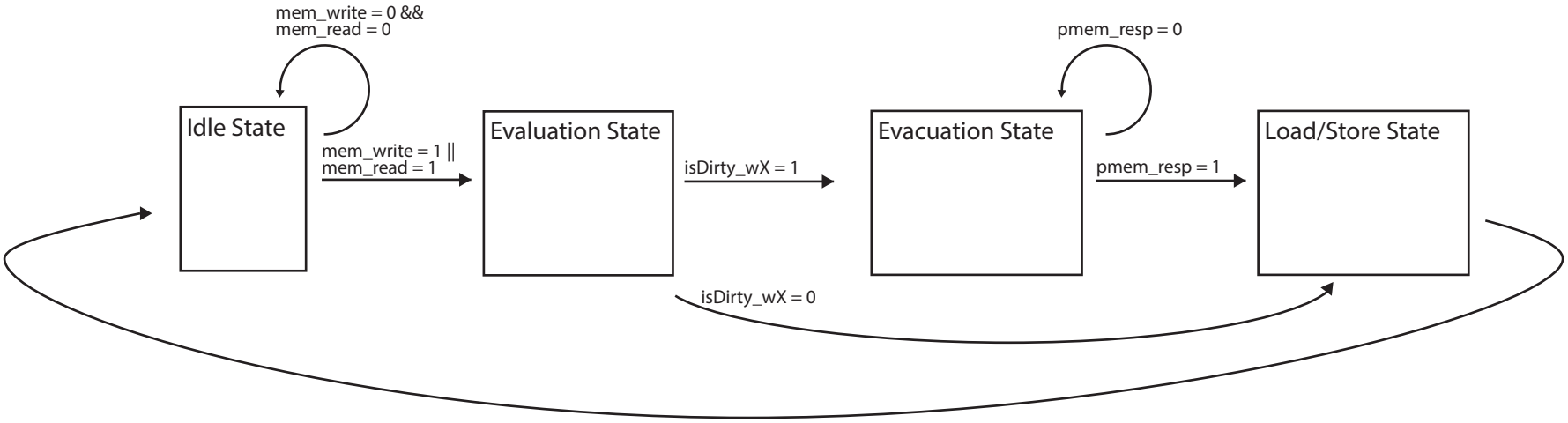

Idle State:
sits spinning setting all load signals to zero until there is a read or write signal from the CPU.

Evaluation State:
Determines the next state based on set register values and inputs from the CPU, like whether it is read/write, and the values from the address parsing. IE: TAG/SET/OFFSET

Mainly, determines if an evacuation is needed or not.

Evacuation State:

If there is a miss, when loading and the valid+dirty bits are High (for LRU way), then we need to evacuate before loading data in from mem.

If there is a miss, when storing and the valid+dirty bits are High (for LRU way), then we need to evacuate before loading data in from mem.

Load/Store:
Execute load and store operations directly with the cache data stores. No memory access in this state.

In the case of a store, we set the values in the data store and set the dirty bit to high. The next time we need to replace, we will need to evacuate (write back)

Cache Control

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