OPTi / MediaCHIPS

82C929
Multimedia Audio Controller

General Description

The OPTi 82C929 is an integrated digital sound controller for PC sound applications. 82C929 is compatible with Sound Blaster™, Ad Lib™, MPU-401, and Microsoft Windows Sound System™.

The 82C929 16-bit Sound Controller provides all of the digital functions and interfaces for the Sound Blaster-compatible and Microsoft Windows Sound System-compatible card. The 82C929 is intended to provide an integrated audio solution for business audio, educational/entertainment sound and multimedia applications.

The 82C929 includes the functions of AT Bus interface, Sound Blaster™ -compatible Digital Audio Processor, MIDI interface, Windows Sound System™ interface, FM synthesizer interface, Wave Table Synthesizer interface, Game Port timer, Codec/Mixer interface as well as interfaces to four different types of CD ROM's. All DMA and interrupt selections are software programmable. The 82C929 provides enough driving capabilities for AT-Bus interfaces and thus eliminates the need for external buffering. There is also a power-down mode for power-conscious system designs.

Features

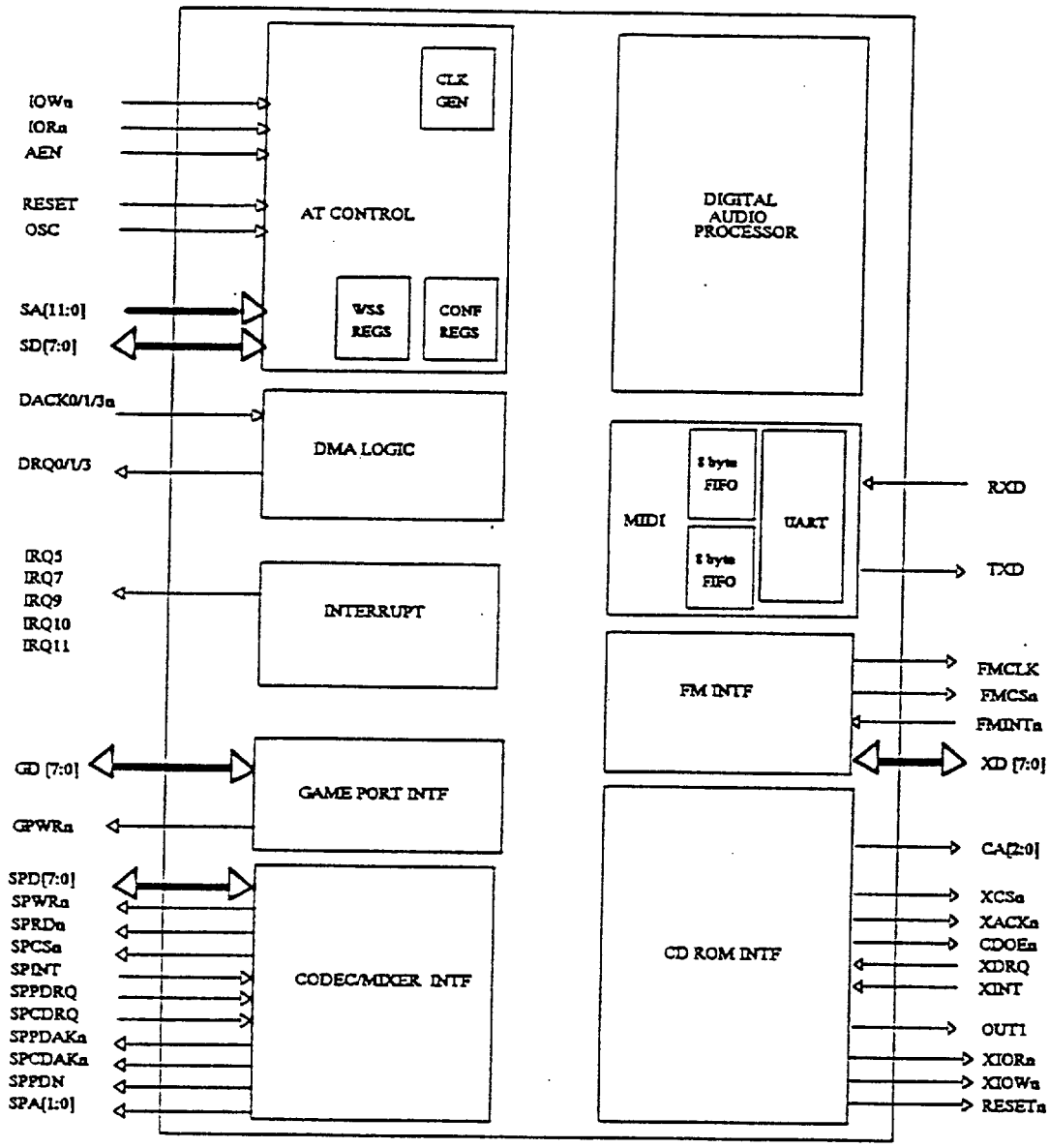
- Integrated sound controller compatible with
  - Sound Blaster,
  - Ad Lib, and
  - Microsoft Windows Sound System.
- 8 or 16-bit sound data:
  - Sound Blaster 8-bit Audio up to 44.1KHz stereo
  - Windows 8/16-bit audio up to 48KHz stereo
- Integrated MIDI UART with 8-byte FIFO for both in and out with MPU-401 interface.
- Direct OPL2/OPL3/OPL4 interface
- Built-In Game Port Timer
- CD ROM interface for
  - IDE
  - SONY
  - Mitsumi
  - Panasonic
- All interfaces are software programmable including
  - I/O Address,
  - IRQ, and
  - DRQ.
- 24mA drivers for direct AT Bus interface
- Powerdown mode
- Silence mode to turn off all audio functions

Applications

Together with the Yamaha OPL3 FM synthesis chip and a 16-bit Codec such as Crystal Semiconductor 4231 or Analog Devices 1346, 82C929 provides the integrated solution for the following applications:

- 16-bit sound quality Sound Blaster + Windows Sound System Compatible Card
- 20 Voice FM Synthesis
- 16-bit CD-quality WAVE audio up to 48KHz stereo
- four types of CD ROM interface
- Game Port
- MPU-401 and Sound Blaster MIDI interface
- OPL4 or other wave table synthesis upgrade

82C929 BLOCK DIAGRAM



PIN LIST

PIN NAME	PIN #	I/O	I/O Type	FUNCTION	To/From
AT BUS SIGNAL (36)					
IOWn	20	I	TTL-Smt 50K pull-up	IO Write Command	AT BUS
IORn	21	I	TTL-Smt 50K pull-up	IO Read Command	AT BUS
AEN	22	I	TTL-Smt	DMA Address Enable	AT BUS
RESET	34	I	TTL-Smt 50K p-d	System Reset Input	AT BUS
OSC	94	I	TTL	AT 14.318 MHz clock	AT BUS
SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0	8 7 6 5 4 3 100 99 98 97 96 95	I	TTL	System Address	AT BUS
SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0	33 32 31 30 27 26 25 24	B	TTL/ 24mA	System Data Bus	AT BUS
DACK0n DACK1n DACK3n	15 17 19	I	TTL 50Kohm pull-up	DMA Acknowledge	AT BUS
DRQ0 DRQ1 DRQ3	14 16 18	T	18mA 50Kohm pull-down	8-bit DMA Request	AT BUS
IRQ5 IRQ7 IRQ9 IRQ10 IRQ11	11 12 13 10 9	Open-Drain B	18mA 5Kohm pull-up TTL	Interrupt Request IRQ7-11 bidirectional for WSS auto interrupt determination	AT BUS
MIDI INTERFACE SIGNAL (2)					
RXD	45	I	TTL-Smt	Receive Data	MIDI Port
TXD	46	O	18mA	Transmit Data	MIDI Port

FM INTERFACE SIGNAL (11)					
FMINT	74	I	TTL 5Kohm pull-up	FM Timer Interrupt, active low	FM
FMCLK/YA2	73	O	4mA	FM Clock output high during powerdown/ OPL4 Address[2]	FM
FMCSn	72	O	4mA	FM Chip Select, Asserted for IO address SBBase + 0-3 SBBase + 8-9 388-38B	FM
XD7 XD6 XD5 XD4 XD3 XD2 XD1 XD0	75 76 77 78 81 82 83 84	B	TTL /4mA 5Kohm pull-up	Local Data Bus	FM
CD ROM INTERFACE SIGNAL (13)					
CA1	86	O	12mA	CD ROM Address 1	CD ROM
CA0	87	O	12mA	CD ROM Address 0	CD ROM
XCSn	88	O	12mA	CD ROM Chip Select	CD ROM
XACKn	89	B	TTL/12mA	CD ROM DMA Acknowledge	CD ROM
XDRQ	90	I	TTL 50Kohm pull-down	CD ROM DMA Request	CD ROM
XINT	91	I	TTL 50Kohm pull-up	CD ROM Interrupt Request	CD ROM
CA2	85	B	TTL 12mA	CD ROM Address 2	CD ROM
CMDn	92	O	12mA	Command Output	CD ROM
CDOEn	93	O	4mA	CD data buffer output enable	
CDHOEn	68	O	4mA	CD[15:8] data buffer output enable	
XIORn	69	O	12mA	Buffered IORn	CD ROM, FM
XIOWn	70	O	12mA	Buffered IOWn	CD ROM, FM
RESETn	71	O	12mA	Buffered RESET, active low	CD ROM, FM
GAME INTERFACE SIGNAL (9)					
GPWRn/ OUT0/ OPL3CSn	35	O	4mA TTL 50k pull-up	External GP Timer Mode: Game Port Write Enable Internal GP Timer Mode: OUTMX=0: OUT0 OUTMX=1: OPL3CSn	Game Port

GD7 GD6 GD5 GD4 GD3 GD2 GD1 GD0	36 37 38 39 41 42 43 44	I	TTL	Game Port Data	
CODEC/MIXER SIGNAL (19)					
SPA1 SPA0	55 54	B	TTL/4mA 50k pu	Codec address	
SPD7 SPD6 SPD5 SPD4 SPD3 SPD2 SPD1 SPD0	63 62 61 60 59 58 57 56	B	TTL/4mA 50K pu	Codec data	
SPWRn	64	O	4mA	Codec Write command	
SPRDn	65	O	4mA	Codec Read command	
SPCSn	66	O	4mA	Codec chip select	
SPINT	67	I	TTL	Codec interrupt request	
PDRQ	48	I	TTL	Playback DMA request	
CDRQ	50	I	TTL	Capture DMA request	
SPPDN	47	O	4mA	Codec Powerdown, active low	
PDAKn	49	O	4mA	Playback DMA acknowledge	
CDAKn	51	O	4mA	Capture DMA acknowledge	
POWER PINS					
Vcc	2, 29, 52, 79				
Gnd	1, 23, 28, 40, 53, 80				
TOTAL	100 (90 Signals, 4 Vcc, 6 Gnd)				

82C929 Register Map

I/O Address	*Description*	*R/W*
SBBase + 0 ALBase + 0	Left FM Status Port	R only
SBBase + 0 ALBase + 0	Left FM Register Address Port	W only
SBBase + 1 ALBase + 1	Left FM Data Port	W only
SBBase + 2 ALBase + 2	Right FM Register Address Port	W only
SBBase + 3 ALBase + 3	Right FM Data Port	W only
SBBase + 4	Mixer Address Port	W only
SBBase + 5	Mixer Data Port	R/W
SBBase + 6	Digital Audio Processor Software Reset	W only
SBBase + 8	FM Status Port	R only
SBBase + 8	FM Register Address Port	W only
SBBase + 9	FM Data Port	W only
SBBase + A	Digital Audio Processor Read Data	R only, Digital Audio ProcessorAO=0
SBBase + C	Digital Audio Processor Write Data/Cmd	W only, Digital Audio ProcessorAO=1
SBBase + C	Digital Audio Processor Write Buffer Status	R only, Digital Audio ProcessorAO=1
SBBase + E	Digital Audio Processor Output Buffer Status Reg	R only, Digital Audio ProcessorAO=1
WSBase + 0-3	Configuration	W only
WSBase + 0-3	Version	R only
WSBase + 4	Codec Index Reg	R/W, exists in Codec and shadowed in 82C929
WSBase + 5	Codec Indexed Data Reg	R/W, exists in Codec only
WSBase + 6	Codec Status Reg	R/W, exists in Codec only
WSBase + 7	Codec Direct Data	R/W, exists in Codec only
200-207	Game Port	R/W
CDBase + 0/3	CD ROM Interface Registers	R/W
MCBase+3 (SF8F)	Password Register	W only
MCBase+1 (SF8D)	MC1	R/W
MCBase+2 (SF8E)	MC2	R/W
MCBase+3 (SF8F)	MC3	R/W
MCBase+4 (SF90)	MC4	R/W
MCBase+5 (SF91)	MC5	R/W
MCBase+6 (SF92)	MC6	R/W

82C929 Register Definition

MC1(MCBase + 1) R/W with password, MC1[3:0] jumper initialized							
7	6	5	4	3	2	1	0
MOD	PDN	Sound BASE[1:0]		CDTYPE[2:0]			GPEN#
default=1	default=0	default=00		jumper pins=SPA1, SPA0, GPWRn no jumper=000			
Mode 0: SB 1: WSS	Powerdown 0: normal 1: powerdown	*WSS Base Address:* 00: WSBase=530 01: WSBase=E80 10: WSBase=F40 11: WSBase=604		000: CD is disabled 001: SONY 31A 010: Mitsumi 011: Panasonic 100: Secondary IDE 101: reserved 110: reserved 111: CHIP TEST MODE			Game Port Enable 0: enabled 1: disabled

Mode Control Register 1:

MOD: Operation Mode

0: Sound Blaster Compatible Mode, this is the default setting
1: Window Sound Compatible Mode

PDN: Powerdown Mode

When high, 82C929 enters powerdown mode. In this mode, all internal clocks are stopped and FMCLK is stopped in the high level.

Sound Base: I/O Base Address

In Window Sound System mode, MC[5:4] selects the I/O base address among the four specified addresses.

CD TYPE: Type of CD ROM Interface

Normal Setting: 00 Hex

MC2 (MCBase + 2) : R/W with password

7	6	5	4	3	2	1	0
CDSEL[1:0]		OPL4	CDIRQ[2:0]			CDDRQ[1:0]	
CD Base Address Select 00: CDBase = 340 01: CDBase = 330 10: CDBase = 360 11: CDBase = 320		OPL4 0: OPL3 1: OPL4	CD IRQ Select 000: CD IRQ = disabled 001: CD IRQ = 5 010: CD IRQ = 7 011: CD IRQ = disabled 100: CD IRQ = 9 101: CD IRQ = 10 110: CD IRQ = 11 111: CD IRQ = disabled			CD DRQ Select 00: CD DRQ = 3 01: CD DRQ = 0 10: CD DRQ = 1 11: CD DRQ is disabled	

The initial value is 03.

CDSEL: CD ROM Base Address

The Base I/O address for CD ROM interface.

OPL4: Yamaha OPL4 Synthesis Chip

When '0', the OPL3 FM synthesis chip is assumed. When '1', the OPL4 Wave Table synthesis chip is assumed. The default is OPL3.

CDIRQ: CD ROM Interrupt Select

This field selects the interrupt channel for CD ROM interface.

CDDRQ: CD ROM DMA Select

Normal Setting: 03 Hex

MC3 (MCBase + 3) R/W with password

7	6	5	4	3	2	1	0
DAIRQ[1:0]		DADRQ[1:0]		FMAP	DABASE	REV[1:0] / GPMODE	
DA IRQ Select 00: IRQ = 7 01: IRQ = 10 10: IRQ = 5 11: IRQ is disabled		DA DRQ Select 00: DRQ = 1 01: DRQ = 0 10: DRQ = 3 11: DRQ is disabled		Frequency Map 0: Normal 1: Single	DA Base Address 0: 220 1: 240	R: Chip ID Number "10" W: Bit 1 is GPMODE Game Port Timer Mode 0: External 1: Internal	

After system reset, the default value of this register is 00. This register is not jumper-initializable.

DAIRQ: Digital Audio Interrupt Request Select for Sound Blaster Mode

DADRQ: Digital Audio DMA Channel Select for Sound Blaster Mode

FMAP: Frequency Mapping Select for Sound Blaster Mode. In Normal mode, frequency is mapped to the nearest frequency using both crystals of the CODEC. In Single mode, frequency is mapped only to the 16 MHz crystal of the CODEC.

Normal Setting: 02 Hex

MC4 User Programmable General Purpose Register

7	6	5	4	3	2	1	0
reserved	GPOUT	reserved	OUTMX	FMCLK	SILENCE	SBVER	
Must be '1'	General Purpose Output	Must be '1'	see GPWRn	0: OPL3 1: OPL2	0: Audio Enabled 1: Audio Disabled	00: 2.1 01: 1.5 10: 3.2 11: 4.4	

GPOUT[1:0]: General Purpose Outputs.

SBVER: Sound Blaster version.

Default = 00

Normal Setting: A2 Hex

MC5 Diagnostic Register

7	6	5	4	3	2	1	0
reserved	reserved	SHPASS	SPACCES	CFIFO	reserved	CFIX	reserved
Must be '1'	Must be '0'	Shadow Protect 0: shadow regs are not protected 1: protected	Codec Access 0: blocked 1: enabled	Command FIFO EN (write only)	Must be '1'	'1' for CS4231 '0' for AD1848	Must be '1'

SHPASS: To protect the internal CODEC shadow registers from written.

SPACCESS: To enable access to CODEC during Sound Blaster mode.

CFIFO: To enable command FIFO in Sound Blaster mode.

CFIX: To enable fix for Crystal 4248/4231 synchronization delays.

Normal Setting: 2F Hex (for CS4231/4248)/ 25 Hex (for AD1848/1846)

MC6 MIDI Interface Register (write only)

7	6	5	4	3	2	1	0
MPU401	**MPU401 Base**		**MPU401 Interrupt**		reserved	reserved	reserved
1: Enable	00: MPUBase=330		00: IRQ9				
	01: MPUBase=320		01: IRQ10		Must be	Must be	Must be
	10: MPUBase=310		10: IRQ5		'0'	'1'	'1'
	11: MPUBase=300		11: IRQ7				

Normal Setting: 83 Hex

Digital Audio Processor Software Reset (SBBase+6) Write Only

7	6	5	4	3	2	1	0
don't care							RESET

RESET = '1' will perform a software reset on the Digital Audio Processor at the end of the IO write command. It actually sets a software reset flag. This software reset is terminated by performing another write at this location with RESET = '0'. A system reset will reset the software reset flag and thus terminates the software reset.

All other bits are don't care.

Digital Audio Processor Read Data (SBBase+A) Read Only

7	6	5	4	3	2	1	0
DATA							

This is the data output port of the Digital Audio Processor.

Digital Audio Processor Write Buffer Status (SBBase+C) Read Format

7	6	5	4	3	2	1	0
IBFULL	(SBBase+A)[6:0]						

IBFULL is '1' when the Digital Audio Processor Input Buffer is full. This flag is set when the host CPU writes data in the input data bus buffer and cleared when the data is read by the internal Digital Audio Processor.

Digital Audio Processor Data/Command Register (SBBase+C) Write Format

7	6	5	4	3	2	1	0
Command/Data							

This is the data/command write port for the Digital Audio Processor.

Digital Audio Processor Output Buffer Status (SBBase+E) Read Only							
7	6	5	4	3	2	1	0
OBFULL	Output Buffer [6:0]						

OBFULL = 1 when the Digital Audio Processor Output Buffer is full. This flag is set in the Digital Audio Processor when data is written in the output data bus buffer and cleared when the host CPU or the DMA controller reads the data in the output data bus buffer.

Reading this register will also clear the Digital Audio Processor interrupt request.

WSS Configuration Register (WSBase+0-3) Write Only							
7	6	5	4	3	2	1	0
reserved	ISS	WSIRQ			WSDRQ		
	0: normal 1: auto interrupt selection	000: disabled 001: IRQ7 010: IRQ9 011: IRQ10 100: IRQ11 101,110,111: reserved			Playback 000: disabled 001: DRQ0 010: DRQ1 011: DRQ3 100: disabled 101: DRQ0 110: DRQ1 111: DRQ3	Capture disabled disabled disabled disabled DRQ1 DRQ1 DRQ0 DRQ0	

ISS: IRQ Sense Source

WSS Version Register (WSBase+0-3) Read Only		
7	6	5:0
Channel Available	IrqSense	Version
0: DRQ0/1/3 and IRQ7/9/10/11 available 1: DRQ1/3 and IRQ7/9 available	0: no interrupt 1: WSS interrupt active	04h

TIMING PARAMETERS

		Min	Max	Units
AT Bus Timing				
OSC (14.318 MHz) Frequency	t_{OSCP}	14.000	14.500	MHz
OSC High Width	t_{OSCH}	32	40	ns
OSC Low Width	t_{OSCL}	32	40	ns
RESET to RSTn	t_{RST}	40	80	ns
IORn/IOWn Command Width	t_{CMDW}	120		ns
Write Data Setup to IOWn Rising	t_{WDSU}	30		ns
Write Data Hold from IOWn Rising	t_{WDHD}	15		ns
Read Access Time	t_{RAC}	20	50	ns
Address Setup to IORn/IOWn Falling	t_{ASU}	50		ns
Address Hold from IORn/IOWn Rising	t_{AHD}	30		ns
DACKn Setup to IORn/IOWn Falling	t_{DKSU}	40		ns
DACKn Hold from IORn/IOWn Rising	t_{DKHD}	160		ns
SD Hold from IORn Rising	t_{DHR}	0	20	ns
DRQ Hold from IORn/IOWn Falling	t_{DRHD}	0	25	ns
CD ROM/FM/Mixer/Game Port Interface Timing				
SA to CA Delay	t_{CA}	3	20	ns
SA to XCSn/FMCSn/MIXCSn	t_{XCS}	5	20	ns
SD to XD Delay	t_{XD}	5	30	ns
XD to SD Delay	t_{XSD}	5	30	ns
XD Read Data Hold	t_{XDH}	5		ns
IORn/IOWn to XIORn/XIOWn Delay IORn/IOWn to GPRn/GPWn Delay	t_{CMDD}	3	20	ns
IOWn to XD Enable Delay	t_{XDE}	5	20	ns
XDRQ to DRQn Delay	t_{DRQ}	5	20	ns
DACKn to XDAKn Delay	t_{XDAK}	5	20	ns
AD1848 Interface Timing				
SA to SPCSn Delay	t_{SPCS}	5	20	ns
SD to SPD Delay	t_{SPD}	5	25	ns

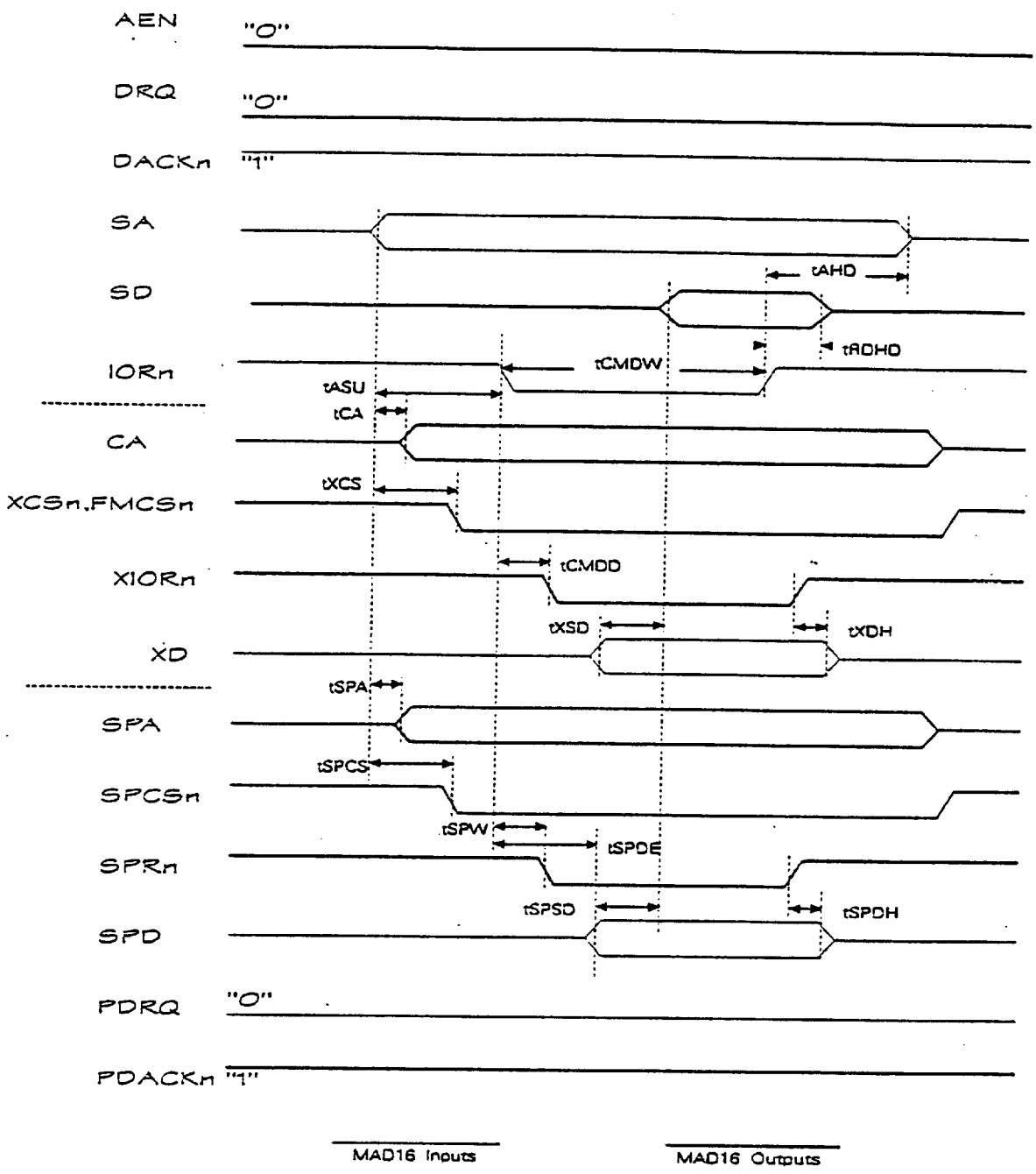
SPD to SD Delay	t_{SPSD}	5	20	ns
SPD Read Data Hold	t_{SPDH}	5		ns
IORn/IOWn to SPRn/SPWn Delay	t_{SPW}	3	20	ns
IOWn to SPD Enable Delay	t_{SPDE}	5	20	ns
IOWn rising to SPD Disable Delay	t_{SPDN}	10	40	ns
DACKn to PDAKn/CDAKn Delay	t_{XDAK}	5	20	ns

DC Electrical Characteristics

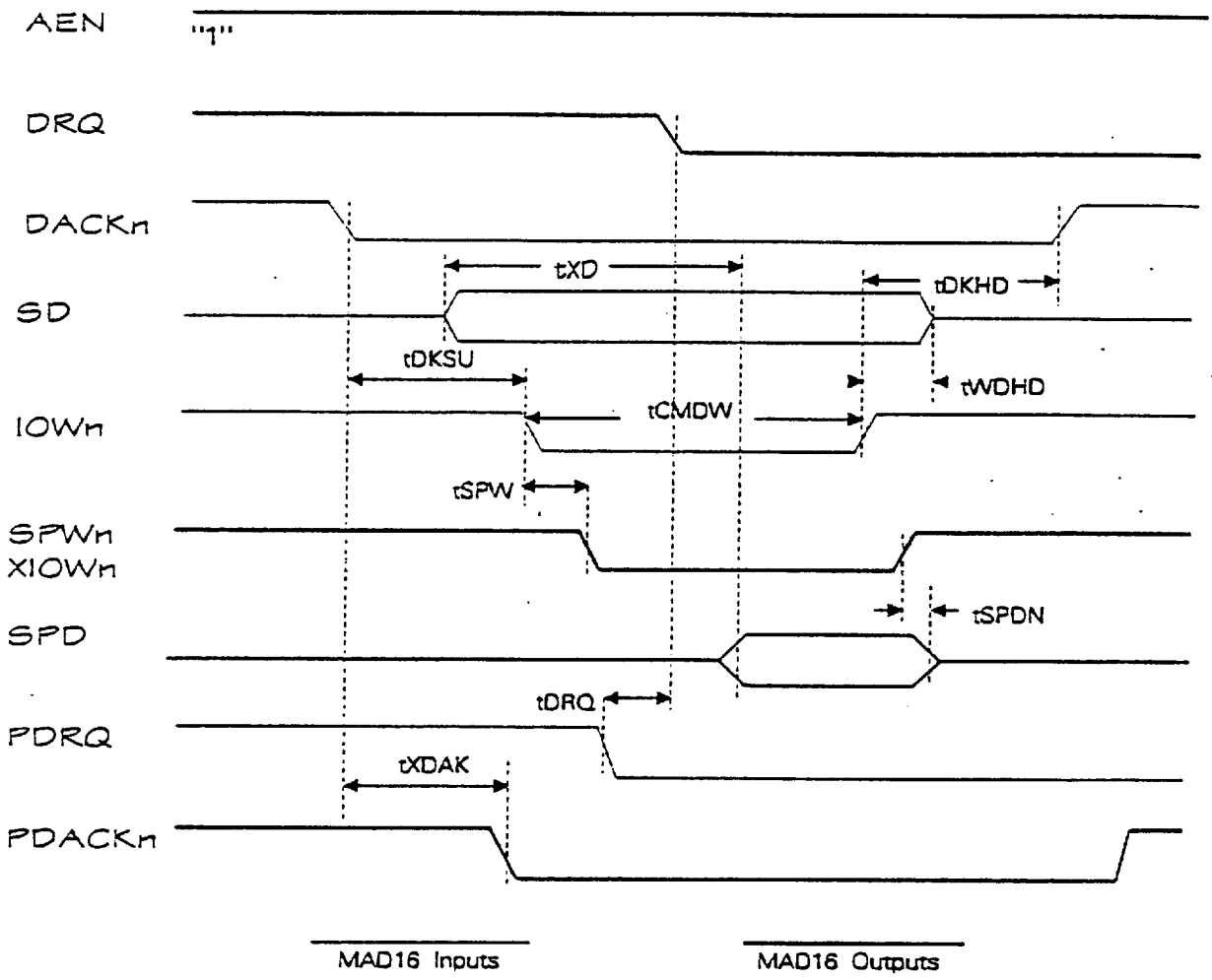
		Min	Max	Units	Conditions
Operating Supply Voltage	Vcc	4.5	5.5	V	
High Level Input Voltage	V_{IH}	2.4	Vcc + 0.3	V	Vcc=min
High Level Input Voltage for RESET	V_{IHa}	3.5	Vcc + 0.3	V	Vcc=min
Low Level Input Voltage	V_{IL}	-0.3	0.8	V	Vcc=max
High Level Output Voltage	V_{OH}	Vcc-0.5	Vcc	V	IOH=-4mA Vcc= max
Low Level Output Voltage	V_{OL}		0.2	V	IOL=4MA Vcc=min
Input Leakage Current	I_{IL}		10	uA	VVcc=ma
Input Leakage Current with 5K pull-up resistor	I_{ILa}	-100	-500	uA	Vin=0V
Input Leakage Current with 50K pull-up resistor	I_{ILb}	-10	-50	uA	Vin=0V
Output Leakage Current	I_{OL}		10	uA	Vcc=max
Static or Powerdown Mode Current	I_{PD}		300	uA	Vcc=max

Absolute Maximum Ratings

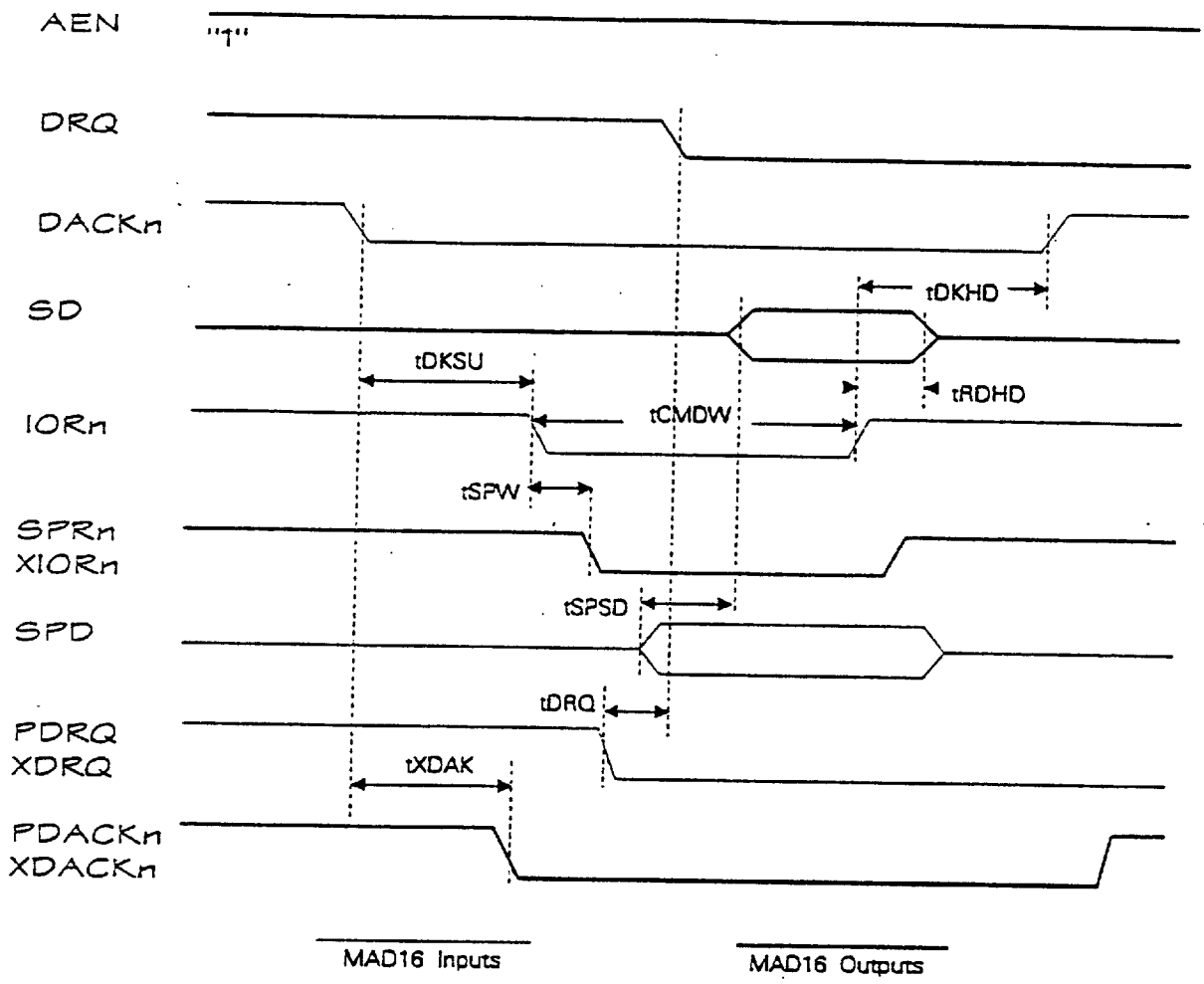
		Min	Max	Units	Conditions
Supply Voltage	Vcc	-0.3	7.0	V	
Storage Temperature	TS	-65	+125	C	
Ambient Operating Temperature	Ta	-45	+85	C	



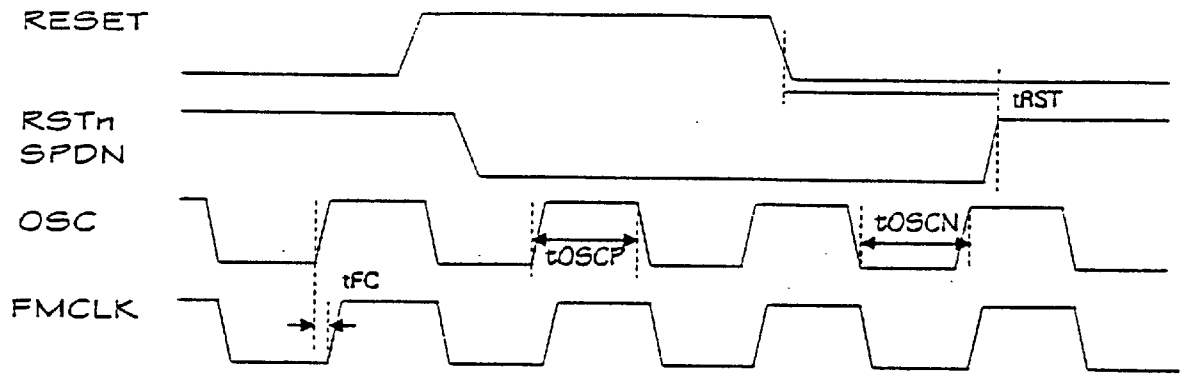
Register/CD/FM/Mixer/Sound Port IO Read Cycle



DMA Write/Playback Cycle

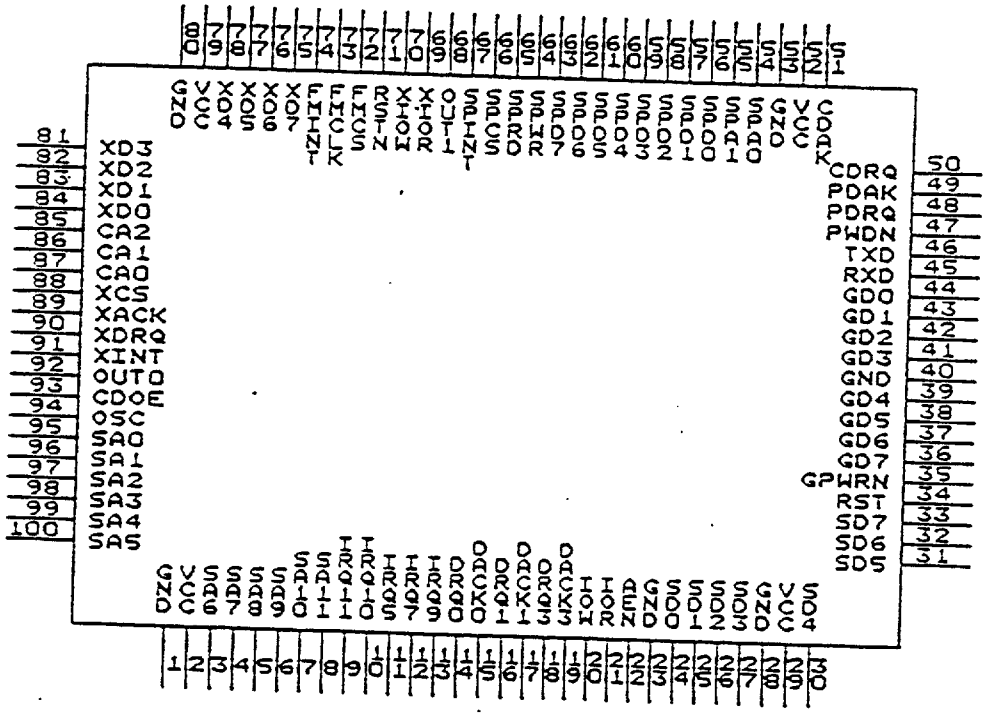


DMA Read/Capture Cycle



RESET and CLK Timing

100-Pin Plastic Quad Flat Pak Pinout



Package Dimensions

100 PIN PLASTIC QFP (14x20)