Ringing Reduction Techniques for NexFET[TM] High Performance MOSFETs

ABSTRACT

The design of switching converters with high performance MOSFET's such as those found in the NexFET[TM] product line require special attention to detail to maximize the effectiveness of the devices and optimize the overall performance of the switching function. Consideration of the challenges of working with ultra-fast power devices early in the design process will ensure the highest performing, most reliable final product.

In this Application Note, the Power Stage of the typical Non-Isolated Synchronous Buck Converter (see Figure 1) will be used as a reference for discussing practical design considerations for maximizing the performance and lifetime of NexFET products. The most common problem encountered in this scenario is parasitic *Voltage Ringing* superimposed on the rising edge of the Switch Node.

This Application Note will discuss the source of the switch node ringing, measurement techniques to accurately characterize this ringing, and methods for minimizing the effect while maintaining excellent system performance.

Bacgkound

Figure 1 shows the schematic of a typical synchronous buck converter. As the performance of power devices is improved, the control FET has the ability to switch voltages at rates greater than $10kV/\mu s$. However, the fast switching faces a common challenge of dealing with switching noise. In particular when the Control FET turns on and the Sync FET is off, the loop inductor, the loop resistor and the output capacitor of the sync FET form a series RLC loop and will resonate at a resonant frequency. This resonance will result in voltage overshoot and ringing at the switch node.
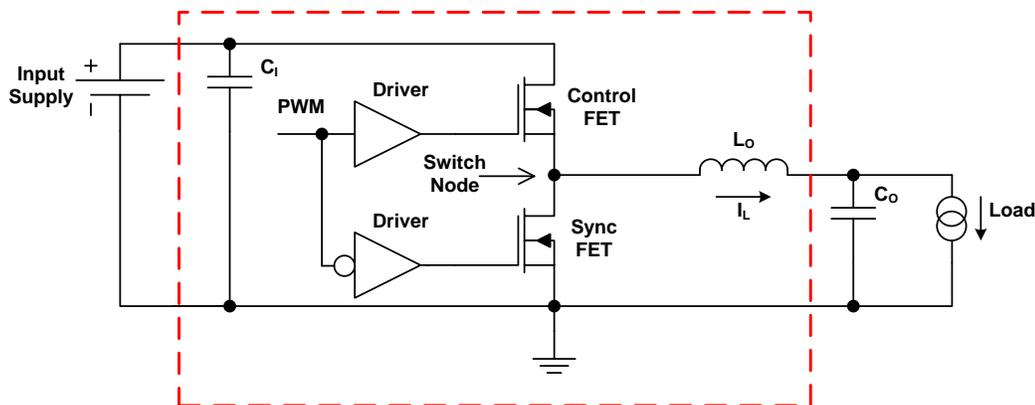
Figure 1.   Definition of Power Stage Components

To understand the source of this ringing, it is useful to make a detailed examination of the switching transient. Assume the Control FET is off, the Sync FET is on, all voltage transients have settled, but I_L continues to flow (slewing at a constant rate) (see Stage 1 in Figure2). During Stage 2, the Sync FET is turned off and a short deadtime is imposed to prevent shoot-through before the Control FET is turned on. During the deadtime the inductor current forces the body diode of the Sync FET to turn on, resulting in a slight drop in voltage at the Switch Node. Stage 3 is initiated by the turn on of the Control FET. As current builds in the Control FET (limited by parasitic inductance and the on resistance of the FET), the body diode of the Sync FET is forced off. The reverse recovery effect of the diode and the slewing of the FET capacitor voltages result in overshoot of the Control FET current.

This current overshoot is absorbed by the output capacitance of the FETs, resulting in overshoot of the Switch Node voltage. The FET capacitances and the parasitic inductance (package inductance, poor layout, etc.) create the resonant network which results in Switch Node Ringing (seen in Stage 3).
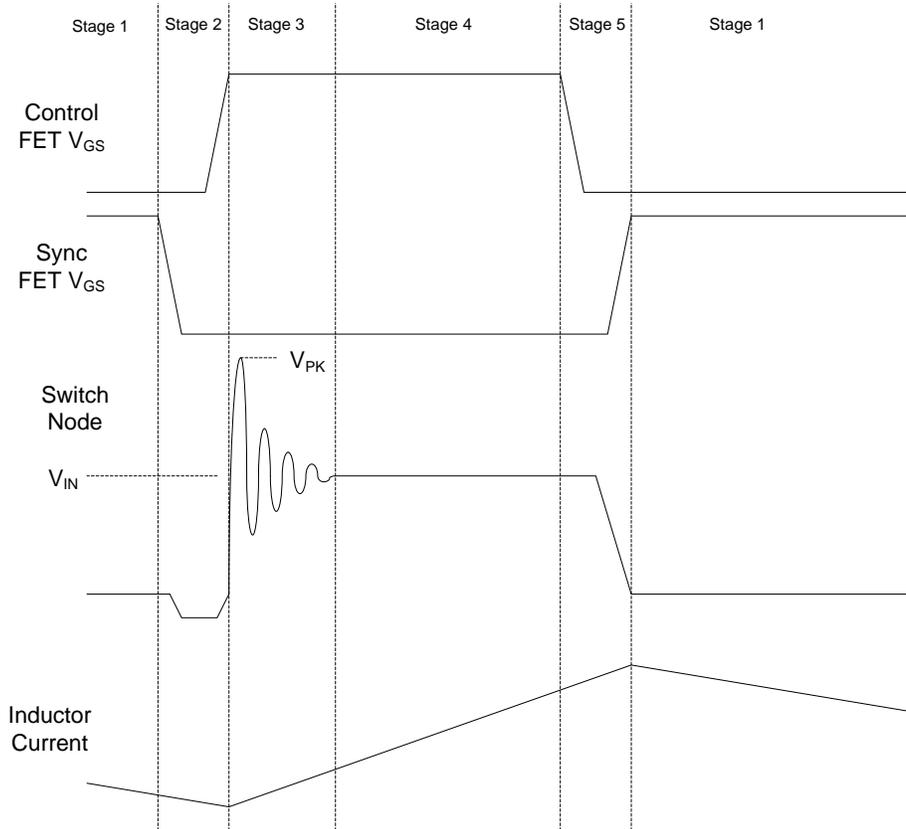
Figure 2.   Switching Waveforms with Exaggerated Switch Node Detail

There are two major industry concerns regarding this ringing commonly found to be superimposed on the Switch Node waveform:
1. Voltage Margin
   a. This is a percentage ratio which takes the magnitude of the first peak within the ringing waveform and compares it to the Breakdown Voltage of the Power MOSFET (BV_{DSS}).
2. EMI/EMC
   a. This the amount of conducted or radiated noise produced by the ringing waveform.

This Application Note will only address the topic of Voltage Margin and will not focus on the topic of EMI/EMC. The topic of EMI/EMC can be somewhat subjective and highly dependent on the overall system/chassis design. However, the enhancements outlined in this paper should somewhat improve the overall EMI/EMC performance of the system in "relative" terms. In addition, there are published (1) (2) papers that have focused on addressing the EMI/EMC effects in these applications.

In terms of Voltage Margin, customers tend to impose an 80% margin rule. This means the maximum voltage measure across the Drain to Source of any MOSFET should not exceed 80% of the MOSFET's BV_{DSS}. For example, a MOSFET with a $BV_{DSS} = 25V$ would be required to only sustain 20V applied across the device at any given time. As such, power supply designers need to have a solution to address a situation that yields ringing that may exceed their Voltage Margin requirements.

Proper Switch Node Measurement Techniques

Before voltage margin improvement techniques are discussed, it is valuable to discuss how to properly measure the switch node waveform to accurately capture the ringing transient. It is important, when taking this measurement, to probe as close as possible to the device in question. This ensures that the actual stress on the device is measured accurately. Figure 3 shows a sample layout of the power stage components using discrete FETs with some possible probe points marked.
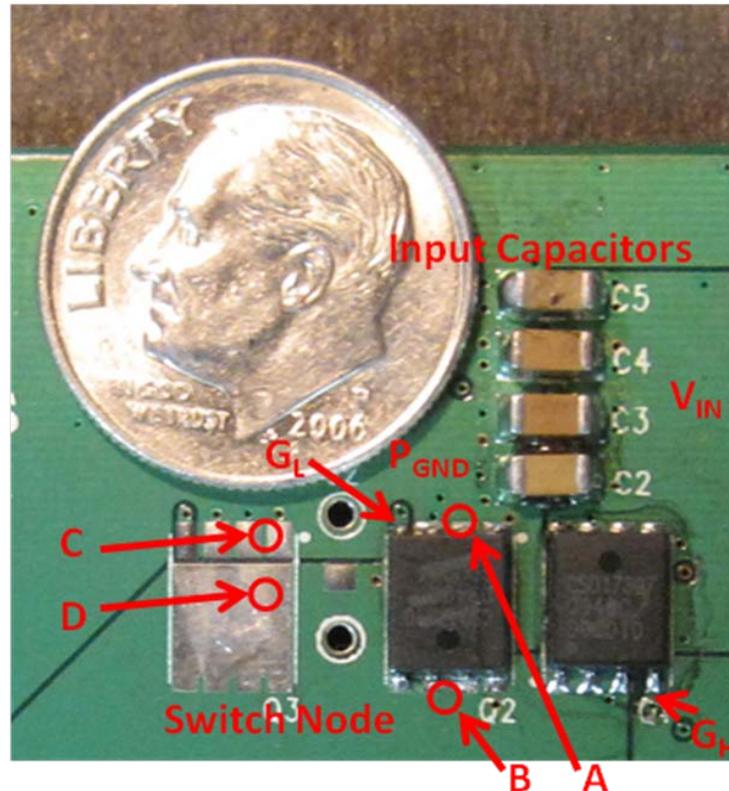
Figure 3.   Sample Power Stage Layout (Inductor and Driver Not Shown) with Potential Probe Points Marked

Figure 4 shows the effect of improper sensing. On the left, a single-ended measurement (shown in Magenta) is taken at point B and compared to the proper differential measurement (shown in blue) taken from point B to point A. The single-ended measurement reports a peak voltage 2.2V lower than the actual stress on the device. On the right side of Figure 5 the proper differential measurement (shown in yellow) is compared to a differential measurement taken a short distance away from the low-side device (point D to point C). In this case, the difference is only 1.5V.

In both cases, the problem is stray inductance between the measurement and the device. Even with a differential measurement taken on the primary pours but not directly on the device pads, a significant drop in the peak voltage is detected. Improper measurement techniques can lead to unnecessarily high margin requirements resulting in less efficient designs.
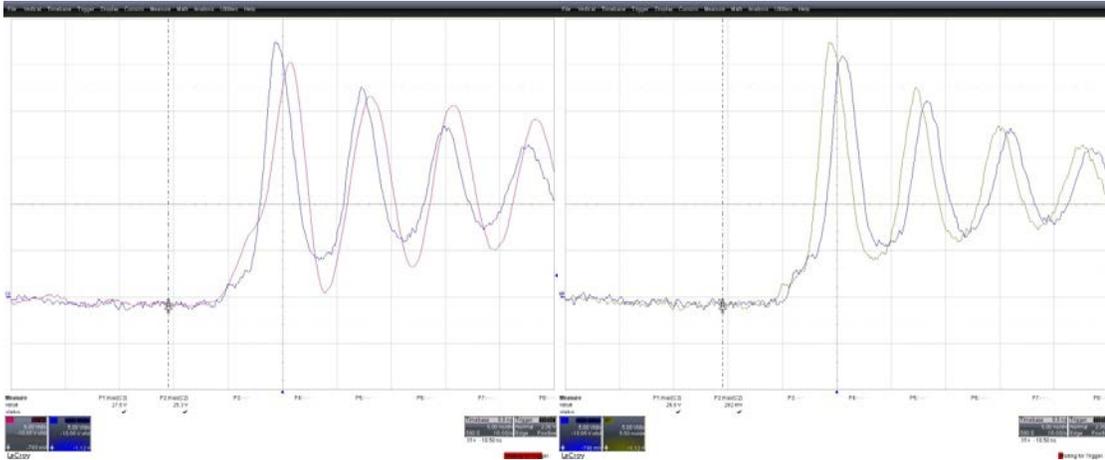
Figure 4. LEFT: Single-Ended (Magenta) Versus Differential (Blue) Measurement RIGHT: Differential Sensing near device (Yellow) and far from device (Blue)

If it is not feasible to perform differential sensing, suitable sensing can still be performed with a single-ended oscilloscope probe, however, the following tips will help to minimize the overall error.

1. The ground lead length of an oscilloscope probe is the most important item in properly capturing the peak values of the switch node voltage ringing. Do not use the standard 3-inch long ground wire supplied with the oscilloscope probe. The long wire loop will act as an antenna by picking up any radiated noise emmitted by the system board and will yield a higher value of switch node voltage ringing than what is actually seen by the device (see Figure 5 and Figure 6). Instead use a small-length ground wire that attaches to the oscilloscope probe tip end (see Figure 7).

2. Placement of the oscilloscope tip and ground must be right on the MOSFET leads (same as in the differentially sensed case). Placement anywhere else introduces higher voltage ringing induced by the PCB parasitic inductance.

3.
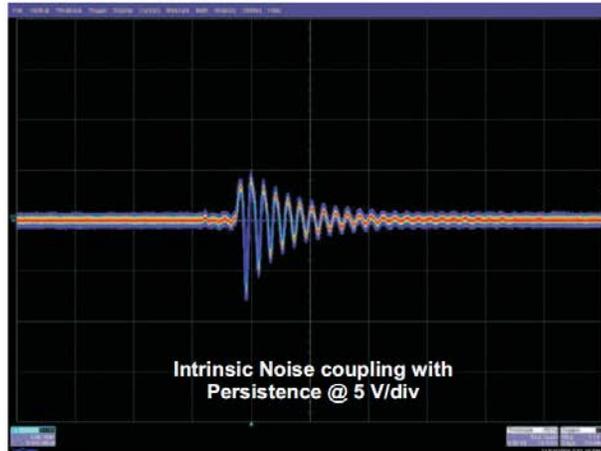
Figure 5.   Ringing Voltage Pick-up by 3-Inch Ground Wire
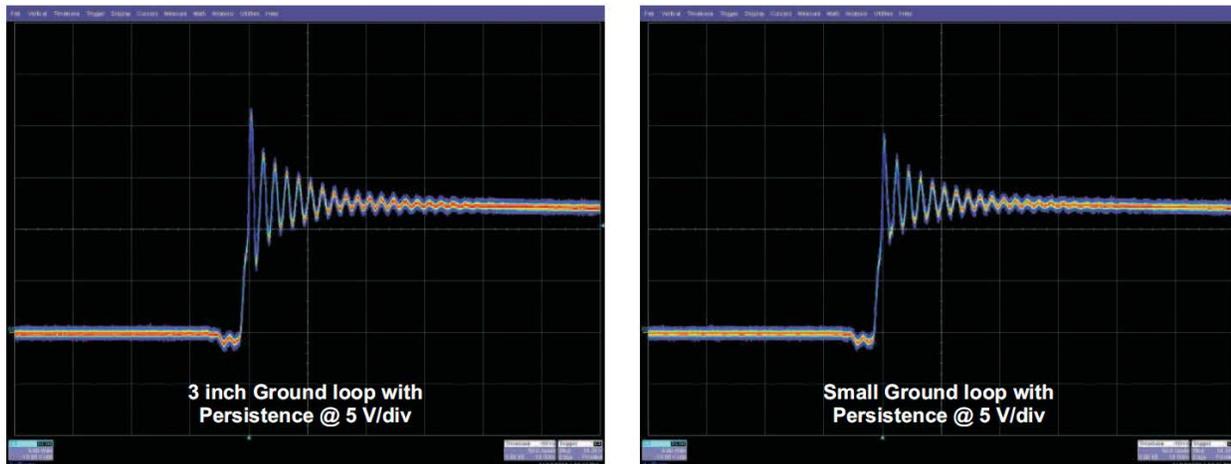
Figure 6.   Switch Node Voltage Ringing Measurements:
Typical 3-Inch Wire (Left) Versus Small Length Wire (Right)

Figure 7.   Oscilloscope Probe Comparison:
Typical 4-Inch Wire (Left) Versus Small Length Wire (Right)

Methods for Reducing Switch Node Ringing

A number of methods have been widely used to minimize the switch node ringing. These methods are listed as follows:

1. Careful PCB layout to minimize the parasitic loop inductance in circuit [1].
2. Gate resistor/ Bootstrap resistor to slow down the turn-on of the control FET.
3. RC snubber circuit to attenuate the ringing.
4. Common Source inductance to slow down the turn on of the control FET.

These methods will be discussed in the following sections respectively.

Optimized Placement of Power Stage Components

The Control FET of has the ability to switch voltages at rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the Power Stage components in order to account for the high rate of change in voltage. Of particular importance is the placement of the input capacitors relative to the Power MOSFETs. It is important to minimize the node lengths between these components.

1. Minimize the node length between the Positive terminal of the input capacitors and the Drain pin of the Control FET.
2. Minimize the node length between the Negative terminal of the input capacitors and the Source pin of the Sync FET.

Looking at a traditional placement of the Power Stage Components (see Figure 8); typically one of these two node lengths will be compromised. This will result in a relatively higher parasitic inductance between the Power MOSFETs and the input capacitors which may yield higher than expected voltage ringing on the switch node. Looking at an optimized placement of the Power Stage Components (see Figure 9); both node lengths have been minimized which in turn minimizes the parasitic inductances.
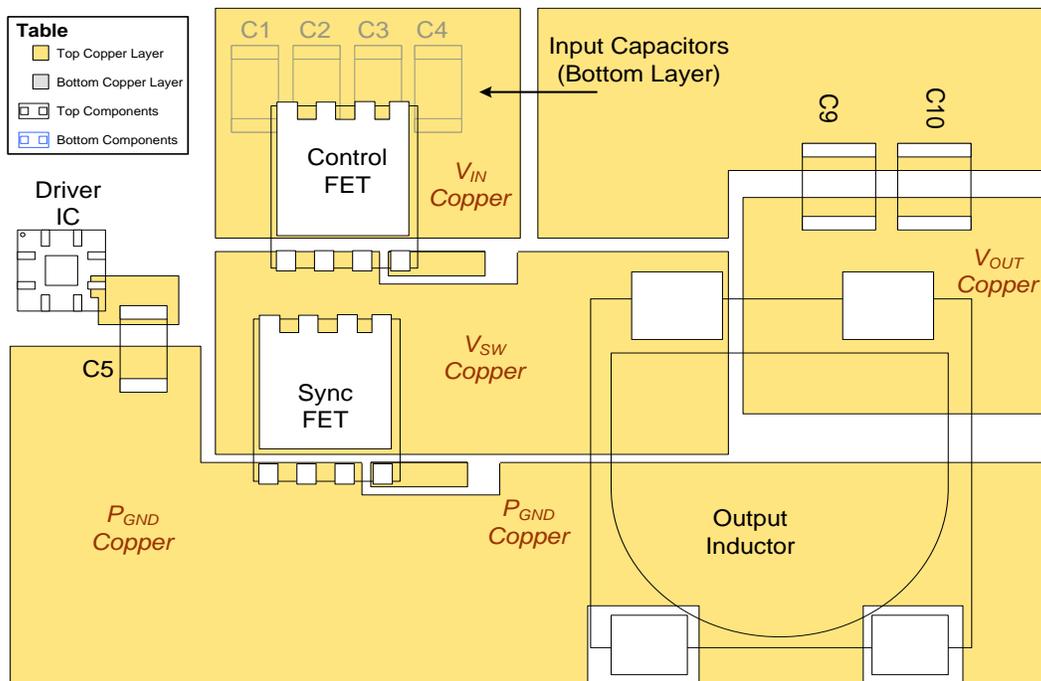
Figure 8.   Typical placement and PCB layout of the Power Stage Components
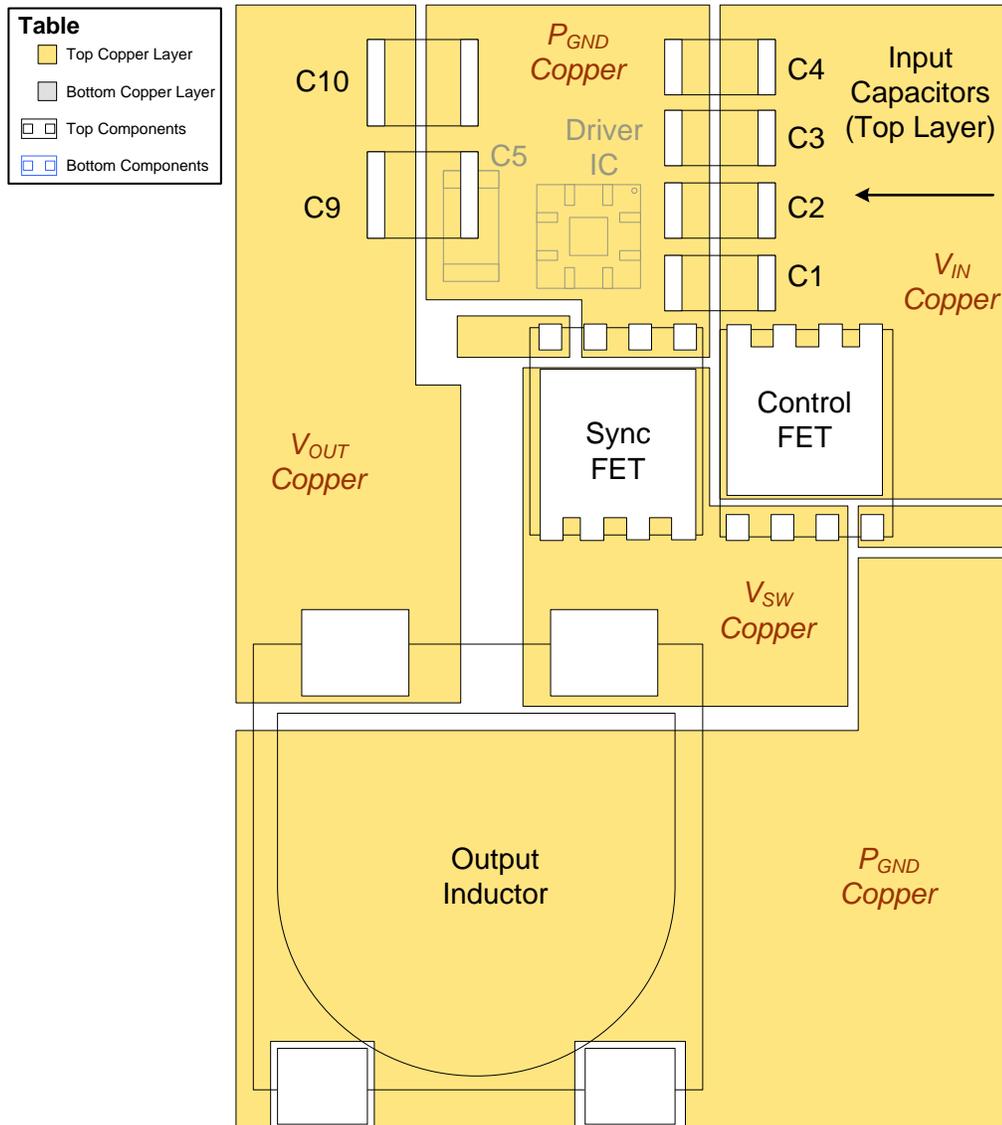
Figure 9.   Optimized placement and PCB layout of Power Stage Components

The most important difference between Figure 8 and Figure 9 is the relative distance between the input capacitors and the Power MOSFETs. In Figure 9, the Sync FET has been rotated by 180º and placed on the left side of the Control FET. The input capacitors have been moved to the top layer and placed right next to the Drain pins of the Control FET and the Source pins of the Sync FET. In both examples, ceramic input capacitors were used due to the inherently low equivalent series inductance (ESL) of these types of caps (10µF, 16V, 1206, X5R, TDK # C3216X5R1A106M). In addition, the Optimized layout allows the placement of the Driver IC to be put directly below the Power MOSFETs on the bottom layer. This will minimize the distance of Gate drive traces.

Testing of Layouts

Figure 10 shows the ringing found on the switch node of the PCB layout example depicted in Figure 8. In this example, the amplitude of the ringing reaches 25V. If the Power MOSFETs used in this example were rated for 25V (BV_{DSS}), then the amplitude of the voltage ringing would yield no design margin as outlined in item #1 in the Background section of this App Note. Figure 11 shows the ringing found on the switch node of the PCB layout example depicted in Figure 9. In this example, the amplitude of the ringing reaches 20V. By simply optimizing the placement of the Power MOSFETs and input capacitors, the voltage ringing amplitude can be reduced by 5V. In the event this design used 25V rated Power MOSFETs, the amplitude of the voltage ringing waveform would meet the typical margin requirements.

Typical Waveform at 5V/div   Zoomed-In with Persistence at 5V/div
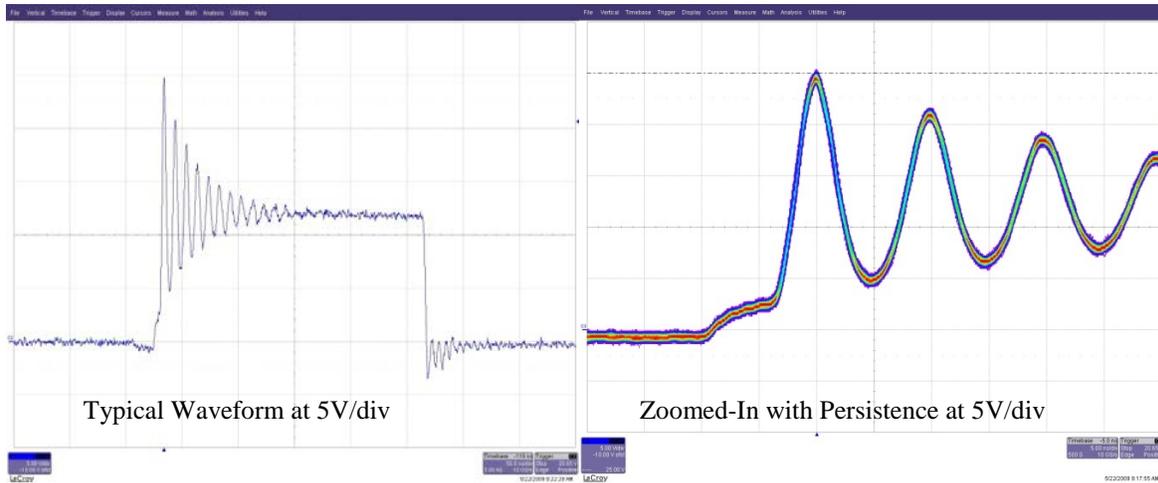
Figure 10. Switch Node (V_{SW}) Voltage Ringing on Typical Layout

Optimized Waveform at 5V/div   Zoomed-In with Persistence at 5V/div
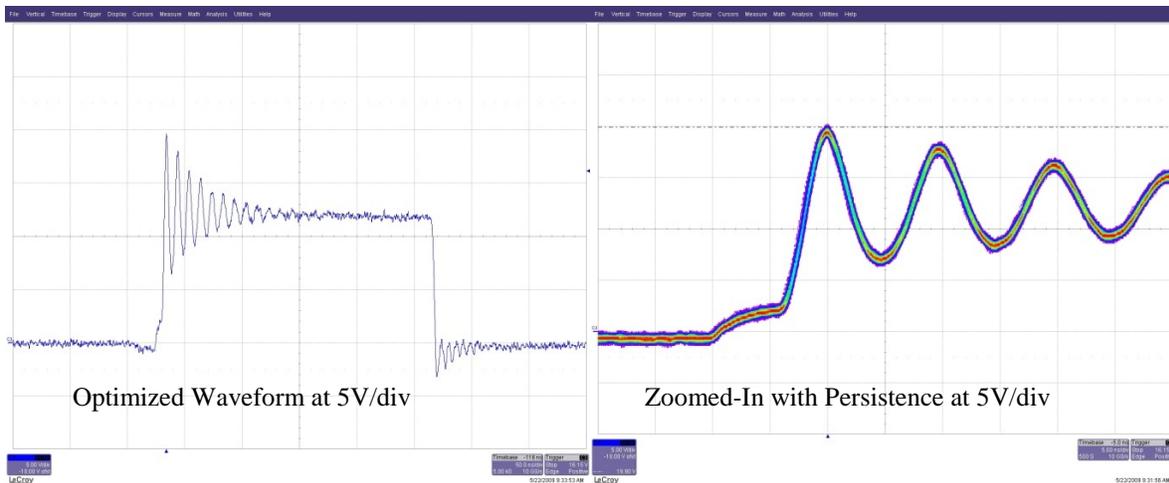
Figure 11. Switch Node (V_{SW}) Voltage Ringing on Optimized Layout

To summarize, the layout and placement of the Power Stage components in a Non-Isolated Synchronous Buck Converter requires special attention in order to optimize the overall performance of the switching function. In particular, voltage ringing commonly found to be superimposed on the switching node can be reduced by up to 5V by simply optimizing the placement and PCB layout of the Power MOSFETs and input capacitors. Optimized PCB board layout is the preferred method for ringing reduction as it does not involve power loss and can actually improve efficiency since one is minimizing the parasitic loop inductance which is one of the root causes of the ringing.

Optimized Boot Resistance

As discussed in the Background section, the fundamental problem of parasitic ringing is caused by high speed switching of the devices which injects excess energy into the parasitics during the switching transient. The two primary sources of this excess energy are fast current transients (di/dt), and fast voltage transients (dv/dt). Slowing down the turn-on of the HS FET will help reduce both of these, but at the cost of more switching power loss.

Adding a small gate resistance between the driver and the gate of the FET is the simplest way to slow down the switching edges. In the case of synchronous buck converters, the rising edge of the switch node is generally the node that must be slowed down. A gate resistor for the Control FET will accomplish this, but will also slow down the turn-off transition resulting in unnecessary power loss. This can be circumvented in two ways:

1. A reverse diode can be placed in parallel to the gate resistor to allow a fast turn-off of the Control FET but a slower turn-on (see Figure 12).
2. The resistor can be placed in the bootstrap path (when present) to slow down only the turn-on speeds (see Figure 13), this resistor is also called bootstrap resistor.

Both methods should be functionally equivalent to pure gate resistance for reducing the peak ringing, and both methods elminate the turn-off switching loss associated with pure gate resistance. However, Method 2 is preferred since it is a lower part count solution. Note that for designs where it is uncertain whether gate resistance is needed, adding a zero ohm resistor in the bootstrap path adds significant flexibilty at a small cost.
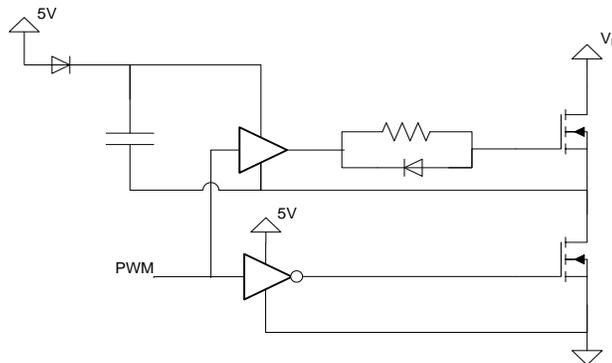
Figure 12.   Gate Resistor with Reverse Diode to Improve Switching Transient
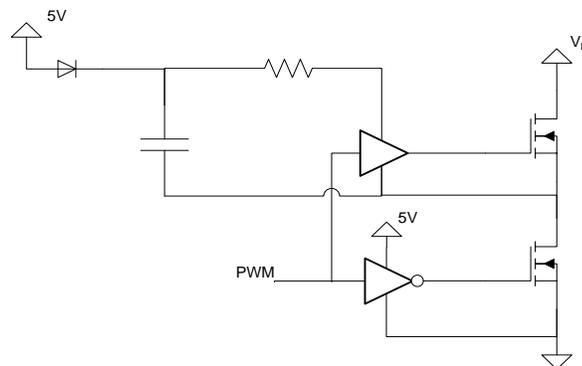
Figure 13.   Bootstrap Resistor to Improve Switching Transient

Testing of Boot Resistance

Figure 14 shows the effect that increasing the bootstrap resistance has on the peak switch node voltage. As expected, the peak voltage is sensitive to input voltage, but not switching frequency. Increasing the bootstrap resistance decreases the peak of the ringing. It can also be noted that there is a limit to the benefit that can be gained using this method.
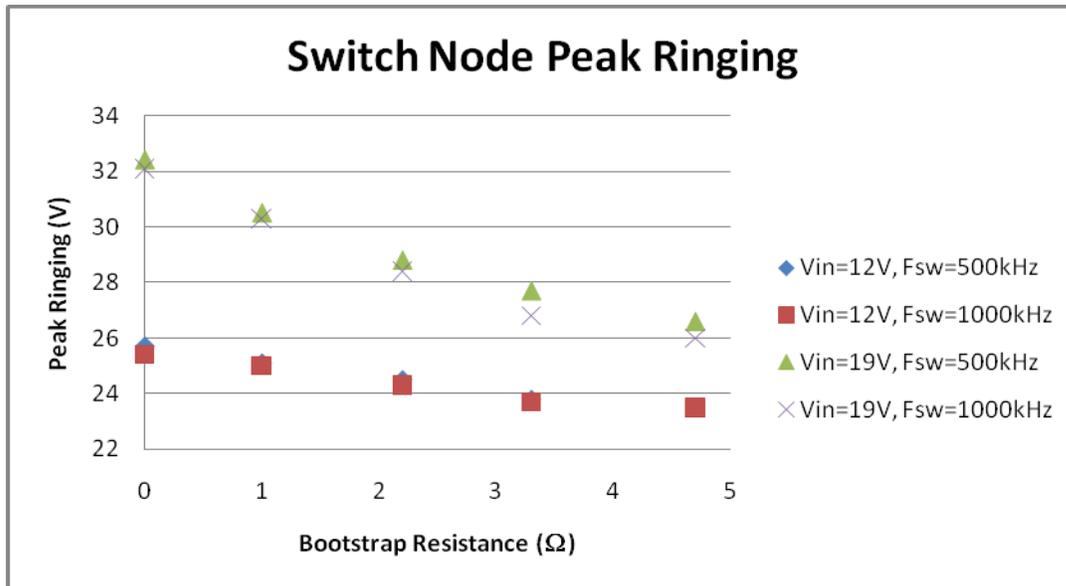
Figure 14. Effect of Adding Bootstrap Resistance on Peak Switch-Node Voltage

The power loss was also measured as a function of bootstrap resistance. The peak power loss (I_{OUT} = 40A) at each operating condition is shown in Figure 15 as a function of bootstrap resistance. Here again, the trend follows the expected trajectory of higher power loss for higher bootstrap resistance. For a given application, a balance must be found between peak ringing and the increased power loss.
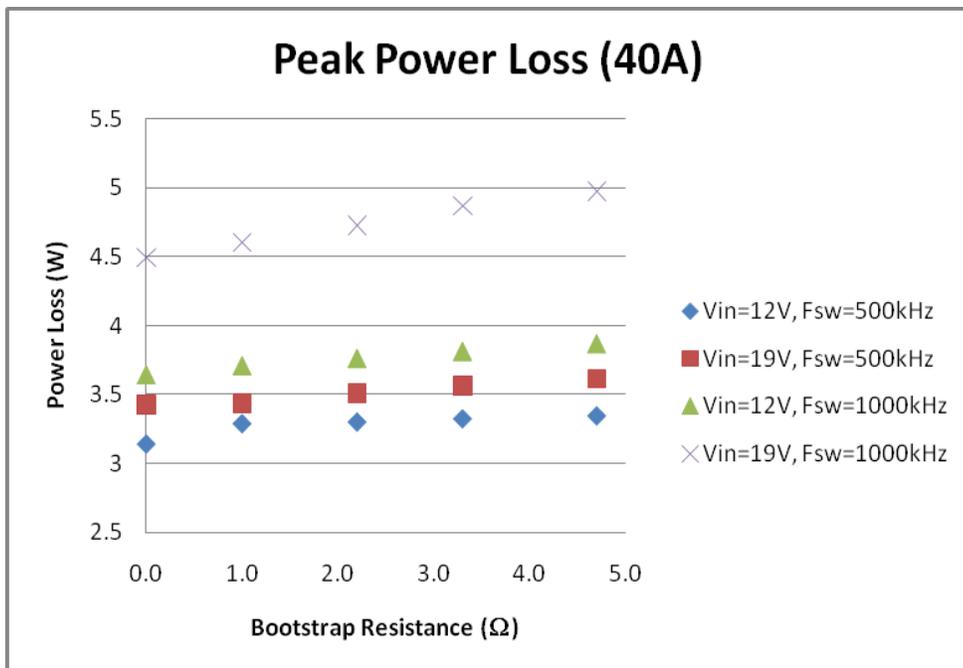
Figure 15.   Effect of Adding Bootstrap Resistance on Power Loss

Figure 16 shows two sample waveforms to illustrate the effect of bootstrap resistance. The waveform on the left was captured with no bootstrap resistance installed, while the one on the right has 4.7Ω of bootstrap resistance. Notice that bootstrap resistance only affects the amount of energy injected into the parasitic ringing, but does not significantly affect the frequency of oscillation.
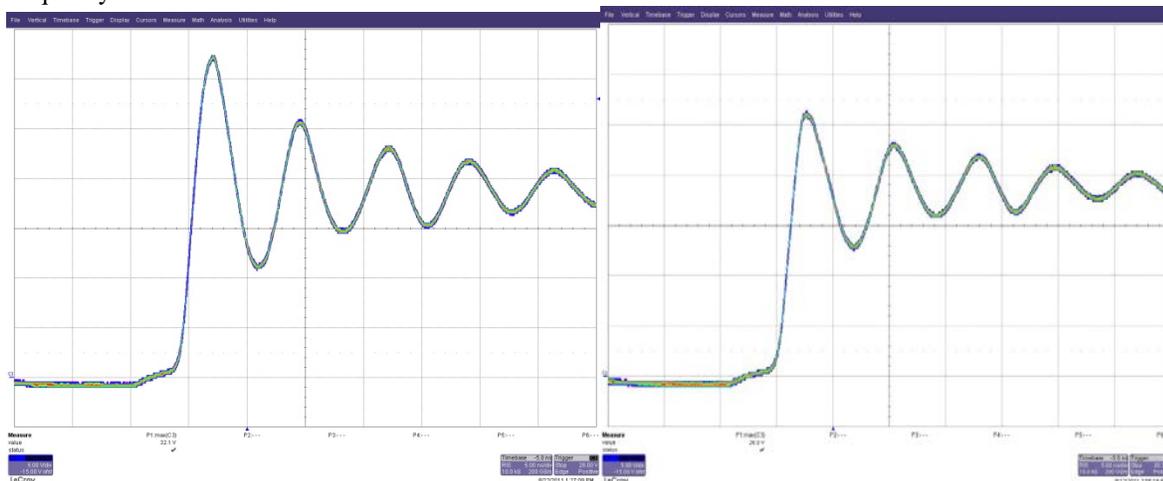
Figure 16.   Switch Node Ringing at V_{in} = 19V, V_{out} = 1.3V, F_{sw} = 1000kHz
LEFT: R_{boot} = 0Ω, RIGHT: R_{boot} = 4.7Ω

Optimized Switch-Node Snubber

The third method for minimizing the peak ringing of the switch node is to add an RC snubber. This is shown schematically in Figure 17. The snubber has the disadvantage of being a bad solution. However, a properly designed snubber can virtually eliminate the parasitic ringing, which is particularly useful if EMI is a top concern. Also, unlike the bootstrap resistor, placeholders for a snubber can be added to a design without the need to populate any parts. This can keep costs down when the snubber is not needed, but still allow for its use if necessary.
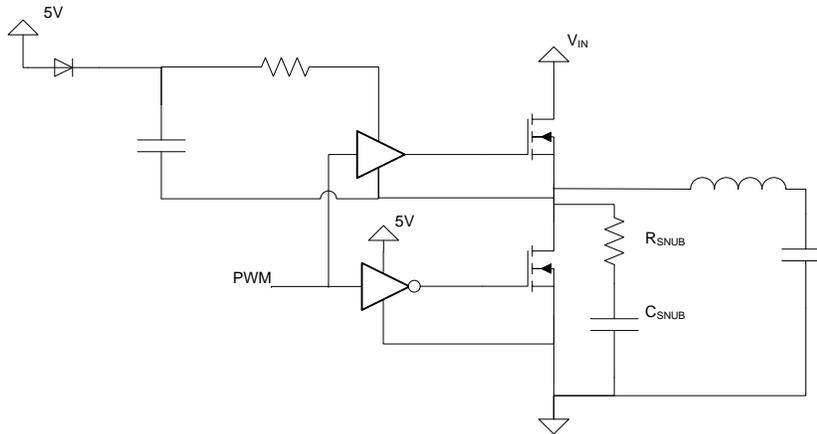
Figure 17.   RC Snubber Added at Switch-Node to Reduce Ringing

A fully optimized snubber of this type can be designed to admit a defined amount of overshoot and then settle with minimum energy loss given the overshoot requirement. However, in practice this is rarely worth the effort as board-to-board manufacturing variation and load and input variation will limit the time at which the circuit operates at the optimal deign point. Instead, a simple and quick method is described here which will usually provide acceptable results.

1. Obtain the parasitic capacitance (C_p) from the MOSFET data sheet. Since the Control FET is on during the ringing, the Sync FET output capacitance C_{OSS} is a good estimate of the total parasitic capacitance.
    When obtaining C_{OSS} off of the data sheet, keep in mind that the value it V_{DS} dependant. $V_{DS} = V_{IN}$ for the Sync FET is the appropriate choice.

2. Measure the un-snubbed ringing frequency (F_p) using an oscilloscope. $L_P = \left(\dfrac{1}{2\pi F_P \sqrt{C_P}} \right)$

3. Estimate the parasitic inductance:
4. Choose C_{snub} to be between ½ and 2 times C_p
5. Estimate the snubber resistance required for optimal damping. The snubbed circuit can be approximated as parallel LCR circuit where L is the parasitic inductance L_P, C is the parasitic capacitance C_P and R is the snubber resistance R_{snub}. The on-resistance of the Control FET and the snubber capacitance can be ignored for this calculation because the on-resistance is small compared to the snubber resistance and the snubber capacitance is designed to block lower frequencies (such as the switching frequency) but appears as a short at the ringing frequency. It is easily shown that for parallel LCR circuit the optimal damping factor (damping factor of 1) is achieved by setting

$$R_{snub} = \frac{1}{2}\sqrt{\frac{L_P}{C_P}}$$ (NOTE: steps 3 and 5 can be combined to calculate R_{snub} directly:

$$R_{snub} = \frac{1}{4\pi F_P C_P})$$

Since the amount of energy lost in the snubber is: $P_{snub} = \dfrac{1}{2} C_{snub} V^2_{snub} F_{SW}$,

,

It is important to keep C_{snub} as small as possible for small power loss. However, if it is too small the snubber won't be effective. Since step 1 ignores any parasitic contribution due to the layout, a poor layout may require a higher C_{snub} value to be effective. A properly designed board can get away with $C_{snub} = \frac{1}{2}C_p$.

The snubber resistance determines the damping of the switch node ringing. Specifically, increasing the snubber resistance speeds up damping of the ringing and decreases the number of the subsequence ringing.   However; when peak ringing is the primary concern smaller values for R_{snub} may be chosen to effectively limit the switch node peak voltage, though ringing will still be present. Examples will be given in next section. Power loss introduced by the snubber is also important for sizing the resistor. Since almost all of the snubber induced power loss is burned on the resistor, resistors with proper power rating should be chosen in RC snubber designs.

Testing of Switch-Node Snubbers

The snubber design outlined here was tested using the following conditions: An input voltage of 12V and output voltage of 1.3V. Waveforms were captured with a 25A load for measuring peak ringing, while peak power loss was reported at 40A. Figure 18 shows several sample waveforms of the switch-node ringing with different snubber resistance and fixed snubber capacitance at 0.47nF. As shown in Figure 15, when the snubber resistance increases, the damping of the ringing becomes more effective while the peak ring increases a little. Normally, the snubber power loss is determined by the snubber capacitance. Therefore, these four applications in Figure 15 have similar power loss though the ringing performances are different.
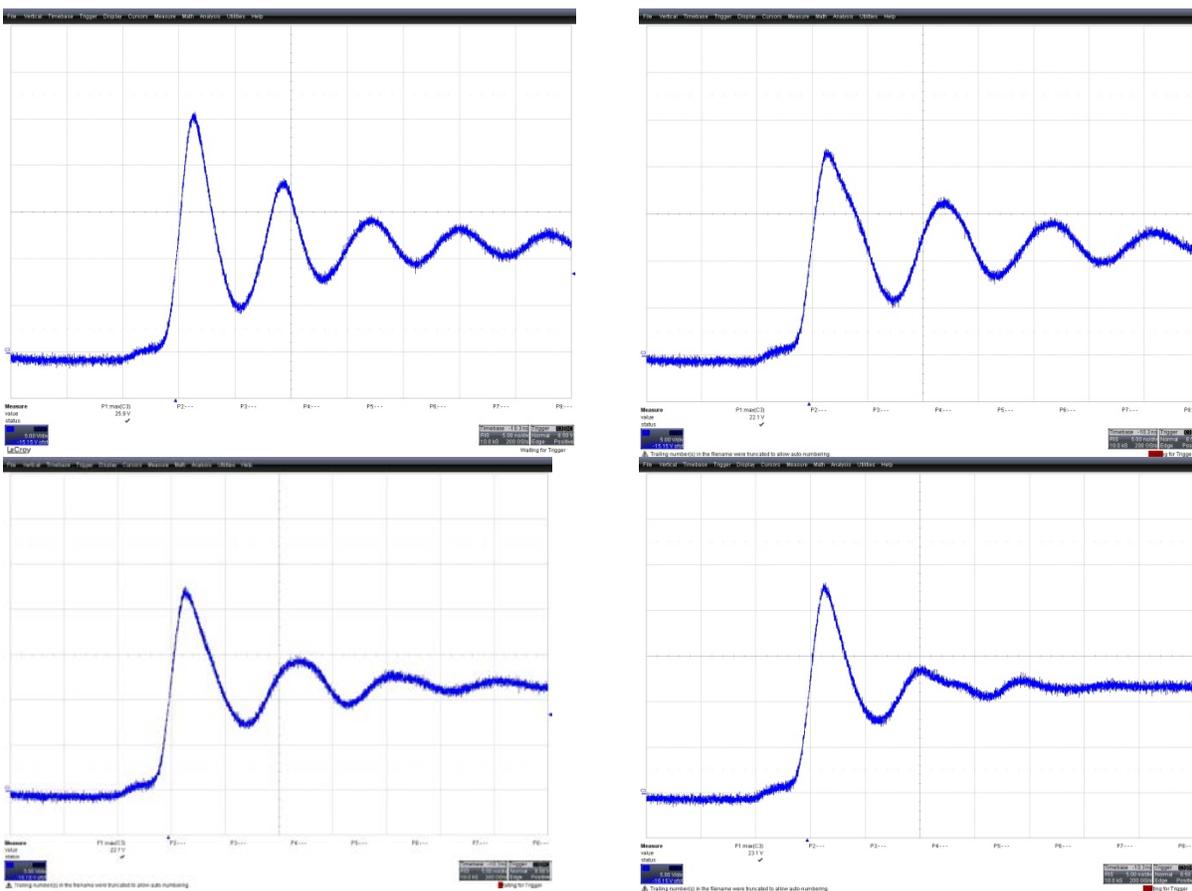
Figure 18.   Switch Node Ringing (Top Left: No Snubber, Top Right: 0.47nF, 0.56Ω, Bottom Left: 0.47nF, 1.2Ω, Bottom Right: 0.47nF, 2.4Ω)

Figure 19 summarizes the impacts of different snubber capacitances on the peak switch node ringing with the snubber resistance remaining constant at 0.33Ω. Note that the zero capacitance point is used to represent the unsnubbed case. As expected, increasing the snubber capacitance reduces the peak ringing. Keep in mind that the increased snubber capacitance will also increase power loss linearly which can be predicted by the snubber power loss equation.
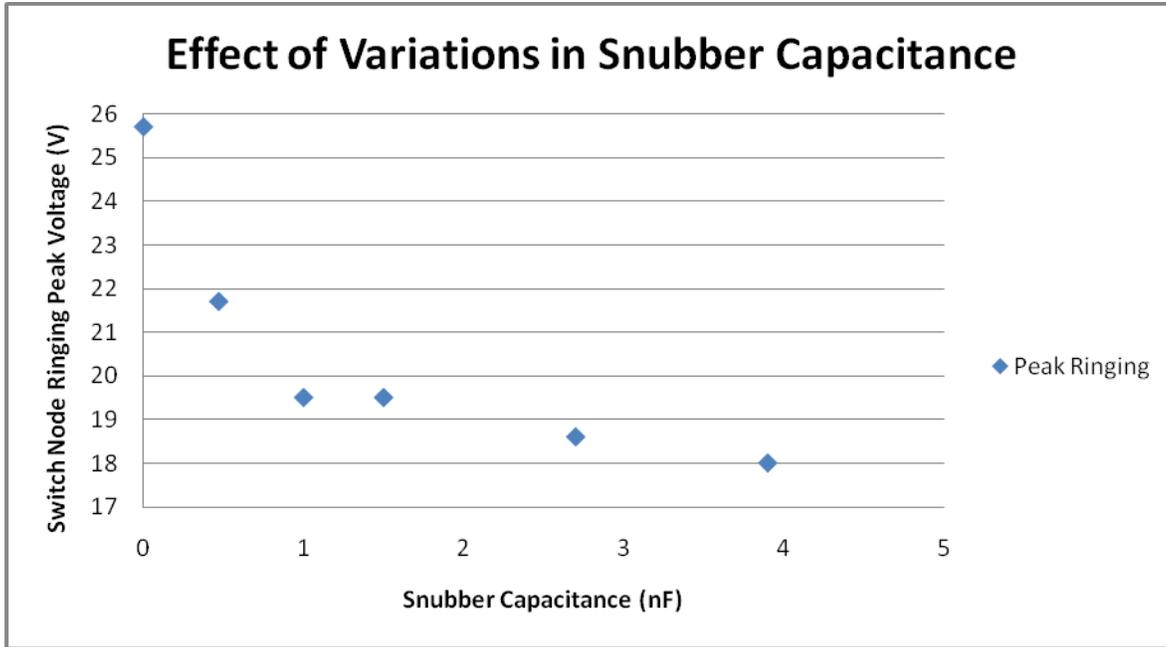
Figure 19.   Effect of Variations in Snubber Capacitance, R_{snub} = 0.33Ω
(NOTE: 0 Indicates no Subber Present, Not Zero Capacitance

Optimized HS Common Source Inductance (CSI)

Another method for switch node ringing reduction is to use CSI to slow down the turn-on of the control FETs. Common source inductance is the inductance shared by the main current path and the gate drive loop and carries the drain source current and the gate current as shown in Figure 20. Any voltage induced on common source inductance will change the effective gate-source voltage of the MOSFET and so that to affect the device switching speed. Therefore, increasing HS FET CSI will slow down the turn-on of the control FET and minimize switch node ringing. In system designs, control FET CSI can be adjusted by properly choosing the switch node pick-up point of the driver IC return path on PCB layout. Specifically, the closer the switch node pick-up point is to the source pins of HS FETs, the smaller the HS CSI will be. However; increasing CSI also introduces extra loss into the system. The adjustment of the CSI and the related impacts on switch node ringing and power loss will be discussed in details thereafter. The drawback for this method is that it is not easy to adjust the value of the inductor as long as the inductor is implemented as a PCB trace in the design. So, inductor value needs to be carefully chosen before the system is implemented in a PCB design.
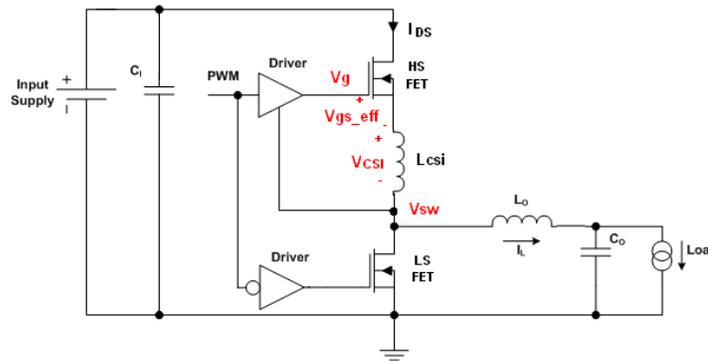
Figure 20.   Schematic of Synchronous Buck Converter with CSI considered

Testing of Source Inductance

As discussed in previous section, choosing different switch node pick-up points for the driver IC return path lead to different CSI values. In this experimental testing, four different switch node pick-up points were implemented in the PCB layout as shown in Figure 21. In Figure 21, as the switch node pick-up point moves from pick-up point 1 to 4, the Control FET CSI increases. In other words, pick-up point 1 has the smallest CSI and pick-up point 4 has the largest CSI. Figure 22 and Figure 23 show the system power loss and switch node ringing waveforms with point 1 to 4 as the driver return path Vsw pick-up point. It is clear that pick-up point 1 has the highest ringing and lowest power loss, while pick-up point 4 has the lowest ringing but highest power loss.
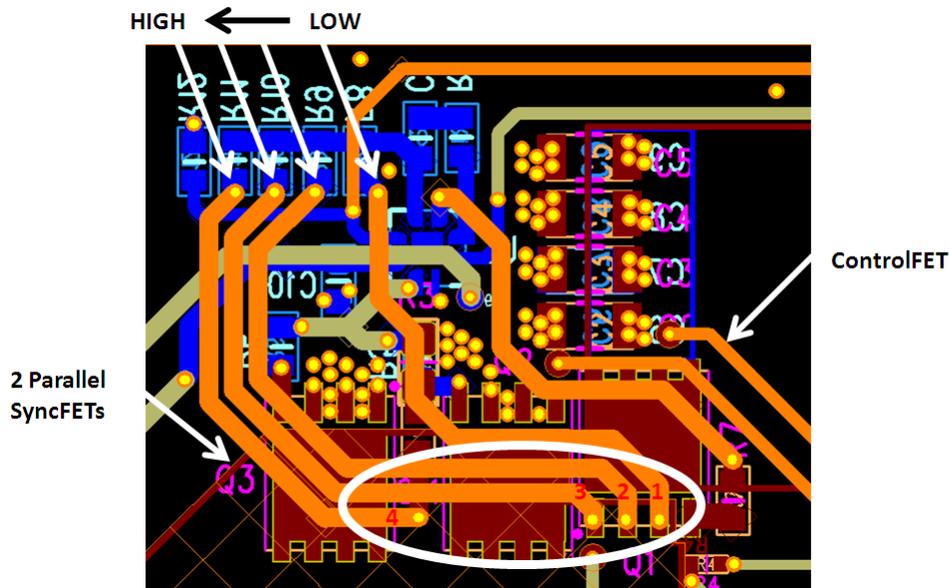
Figure 21.   Source Inductance Test Layout. Source Inductance is Selectable by Choice of Resistor R8-R11
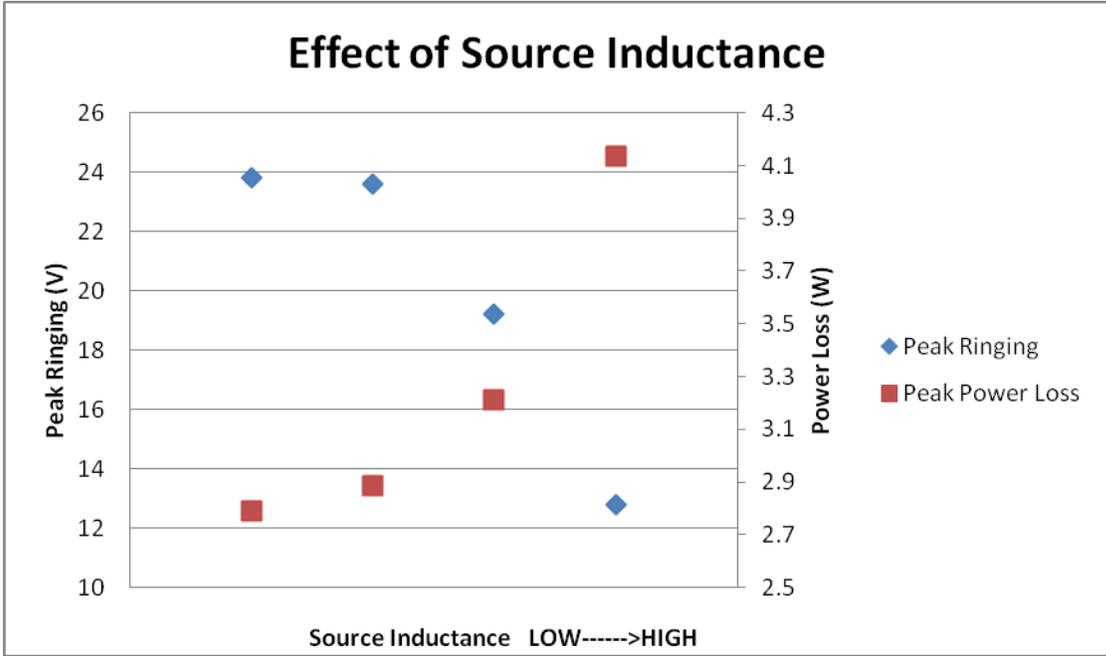
Figure 22. Effect of Adding Source Inductance on Peak Ringing and Power Loss
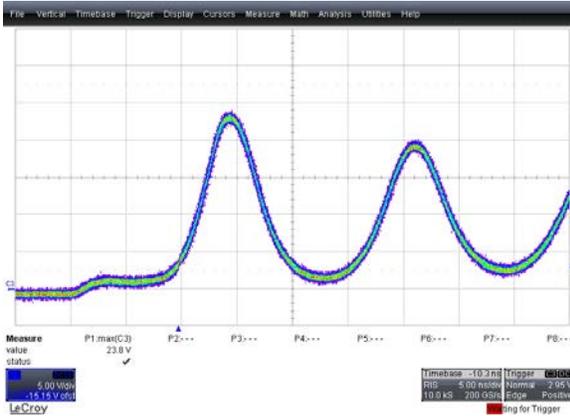
(a) Vsw at Pick-up Point 1
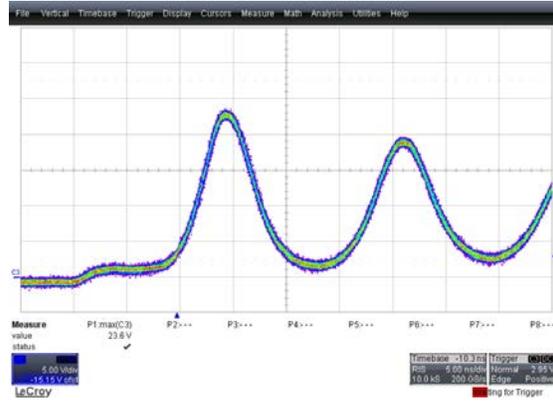
(b) Vsw at Pick-up Point 2
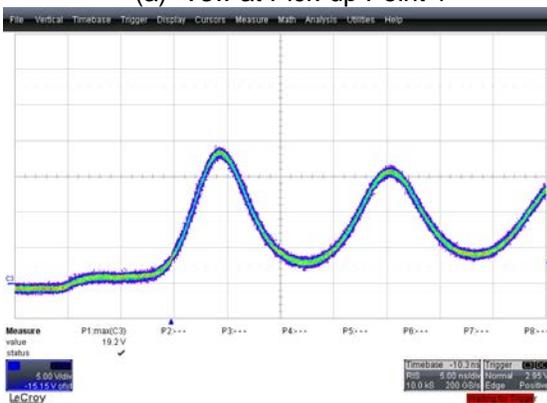
(c) Vsw at Pick-up Point 1
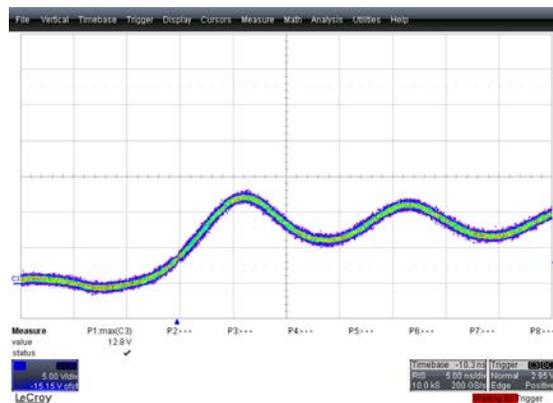
(d) Vsw at Pick-up Point 4

Figure 23.   Switch Node Ringing Waveforms.

Summary

In this note, the root cause of the switch node ringing is introduced and measurement techniques were discussed to ensure accurate characterization of the switch node ringing. Then, four techniques were examined for reducing the switch node ringing. The first and best line of defense against switch-node ringing is proper layout and sufficient input capacitance. These methods attack the root cause of the problem to minimize the ringing amplitude as well as ensure optimal efficiency. Beyond proper layout, adding bootstrap resistance/gate resistance, a switch-node RC snubber, or increasing the control FET common source inductance are potential techniques for controlling the peak switch node ringing though they will introduce extra power loss. The technique(s) employed in any given design must take into account expected operating conditions, efficiency targets, EMI design considerations and cost. The examples shown in this document can be used as guides for understanding the trade-offs associated with each technique.

References

1. *EMI Analysis Methods for Synchonous Buck Converter EMI Root Cause Analysis.* **Kam, Keong W., et al.** 2008, International Symposium on Electromagnetic Compatibility.
2. *EMC Guideline for Synchronous Buck Converter Design.* **Kam, Keong, et al.** 2009, International Symposium on Electromagnetic Compatibility.

IMPORTANT NOTICE

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		