Understanding the Requirements of ISO/IEC 14443 for Type B Proximity Contactless Identification Cards

Requirements of ISO/IEC 14443 Type B Proximity Contactless Identification Cards

Application Note

Introduction

ISO/IEC 14443 is a four-part international standard for Contactless Smart Cards operating at 13.56 MHz in close proximity with a reader antenna. Proximity Integrated Circuit Cards (PICC) are intended to operate within approximately 10cm of the reader antenna.

Part 1 [ISO/IEC 14443-1:2000(E)] defines the size and physical characteristics of the card. It also lists several environmental stresses that the card must be capable of withstanding without permanent damage to the functionality. These tests are intended to be performed at the card level and are dependent on the construction of the card and on the antenna design; most of the requirements cannot be readily translated to the die level. The operating temperature range of the card is specified in Part 1 as an ambient temperature range of 0°C to 50°C.

Part 2 [ISO/IEC 14443-2:2001(E)] defines the RF power and signal interface. Two signaling schemes, Type A and Type B, are defined in part 2. Both communication schemes are half duplex with a 106 kbit per second data rate in each direction. Data transmitted by the card is load modulated with a 847.5 kHz subcarrier. The card is powered by the RF field and no battery is required.

Part 3 [ISO/IEC 14443-3:2001(E)] defines the initialization and anticollision protocols for Type A and Type B. The anticollision commands, responses, data frame, and timing are defined in Part 3. The initialization and anticollision scheme is designed to permit the construction of multi-protocol readers capable of communication with both Type A and Type B cards. Both card types wait silently in the field for a polling command. A multi-protocol reader would poll one type of card, complete any transactions with cards responding, and then poll for the other type of card and transact with them.

Part 4 [ISO/IEC 14443-4:2001(E)] defines the high-level data transmission protocols for Type A and Type B. The protocols described in Part 4 are optional elements of the ISO/IEC 14443 standard; proximity cards may be designed with or without support for Part 4 protocols. The PICC reports to the reader if it supports the Part 4 commands in the response to the polling command (as defined in Part 3).

The protocol defined in Part 4 is also capable of transferring application protocol data units as defined in ISO/IEC 7816-4 and of application selection as defined in ISO/IEC 7816-5. Note that ISO/IEC 7816 is a Contacted Integrated Circuit Card standard.

This application note is intended to summarize the requirements of ISO/IEC 14443 that apply to Type B integrated circuits. It is not intended to describe all possible interpretations of these requirements. The requirements in Part 1 and for Type A cards will not be discussed in detail. Part 4 requirements are not discussed in detail. Recent amendments to the ISO/IEC 14443 standards are beyond the scope of this Application note. No communication rates above 106 Kbps are discussed.

Rev. 2056B–RFID–11/05

Abbreviations and Nomenclature

The nomenclature and abbreviations of ISO/IEC 14443 are used throughout this application note. A table of abbreviations used in this application note is shown below.

Term	Description
AC	Alternating Current
ACK	Positive Acknowledge (success)
ADC	Application Data Coding
AFI	Application Family Identifier
AID	Application Identifier Code (defined in ISO/IEC 7816-5)
ASK	Amplitude Shift Keying Modulation (PCD to PICC for Type B)
ATQB	Answer to Request, Type B
ATTRIB	PICC Selection Command, Type B
BPSK	Binary Phase Shift Keying Modulation, (PICC to PCD for Type B)
CID	Card Identifier
CRC_B	Cyclic Redundancy Check Error Detection Code B
D	Divisor
DC	Direct Current
EGT	Extra Guard Time
EOF	End of Frame
ETU	Elementary Time Unit = 128 Carrier Cycles (9.4395 µS) = 8 Subcarrier Units
fc	Carrier Frequency = 13.56 MHz
FO	Frame Option
fs	Subcarrier Frequency = fc/16 = 847.5 kHz
FWI	Frame Waiting Time Integer
FWT	Frame Waiting Time
HLTB	Halt Command, Type B
Hmin	Minimum Unmodulated Operating Field (1.5 A/m rms)
Hmax	Maximum Unmodulated Operating Field (7.5 A/m rms)
IC	Integrated Circuit
ID	Identification
INF	Information Field for Higher Layer Protocol (per 14443-4)
kbps	Kilobits per Second
LSB	Least Significant Bit
MSB	Most Significant Bit
MBLI	Maximum Buffer Length Index of PICC (per 14443-4)

Table 1. Terms and Abbreviations

Term	Description
N	Number of Anticollision Slots (or response probability per slot)
NAK	Negative Acknowledge (Failure)
NAD	Node Address (per 14443-4)
NRZ-L	Non-Return to Zero (L for Level) Data Encoding (for PICC data transmission)
OOK	On/Off Keying Modulation (PICC to PCD for Type A)
PCD	Proximity Coupling Device (Reader/Writer)
PICC	Proximity Integrated Circuit Card
PUPI	Pseudo Unique PICC Identifier
R	Random Number Selected by PICC during Anticollision
REQB	Request Command, Type B
RF	Radio Frequency
RFU	Reserved for Future Use by ISO/IEC
S	Slot Number (sent to PICC with Slot MARKER command)
SOF	Start of Frame
TR0	Guard Time per 14443-2
TR1	Synchronization Time per 14443-2
TR2	PICC to PCD Frame Delay Time (per 14443-3 Amendment 1)
WUPB	Wake Up Command, Type B

Table 1. Terms and Abbreviations (Continued)

Operating Principle

Contactless RF smart cards operating at 13.56 MHz are powered by and communicate with the reader via inductive coupling of the reader antenna to the card antenna. The two loop antennas effectively form a transformer (see Figure 1).

An alternating magnetic field is produced by sinusoidal current flowing through the reader antenna loop. When the card enters the alternating magnetic field, an alternating current (AC) is induced in the card loop antenna. The PICC integrated circuit (IC) contains a rectifier and power regulator to convert the AC to direct current (DC) to power the integrated circuit.

The reader amplitude modulates the RF field to send information to the card. The IC contains a demodulator to convert the amplitude modulation to digital signals. The IC also contains a clock extraction circuit that produces a 13.56 MHz digital clock for use within the IC. The data from the reader is clocked in, decoded, and processed by the integrated circuit.

The IC communicates with the reader by modulating the loading on the card antenna, which also modulates the load on reader antenna. ISO/IEC 14443 PICCs use a 847.5 kHz subcarrier for load modulation, which allows the reader to filter the subcarrier frequency off the reader antenna and decode the data.

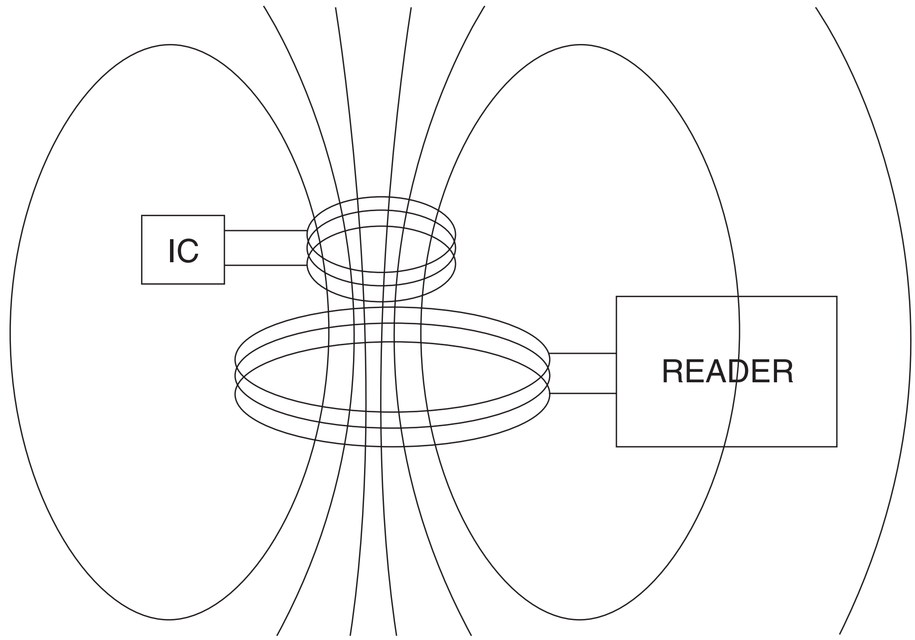


Figure 1. The IC Antenna and Reader Effectively Form a Transformer

Type A Signaling

Type A signaling utilizes 100% amplitude modulation of the RF field for communication from the reader to the card with Modified Miller encoded data (see Figure 2). Communications from card to reader utilizes OOK modulation of an 847.5 kHz subcarrier with Manchester encoded data (see Figure 3). In Type A signaling, the RF field is turned off for short periods of time when the reader is transmitting. The integrated circuit must store enough energy on internal capacitors to continue functioning while the RF field is momentarily off during field modulation.

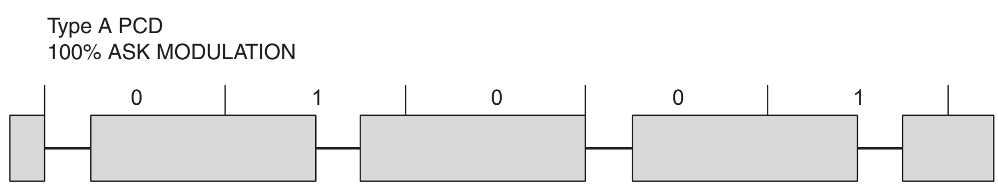


Figure 2. Modified Miller Encoding, Type A

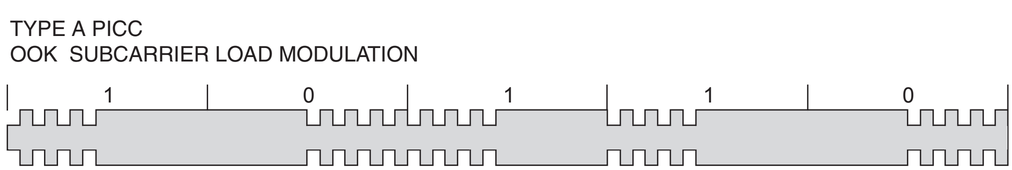


Figure 3. Manchester Encoding, Type A

Type A signaling is described here for purposes of comparison. The remainder of this application note discusses Type B only.

Type B Signaling

Type B signaling utilizes 10% amplitude modulation of the RF field for communication from the reader to the card with NRZ encoded data. Communication from card to reader utilizes BPSK modulation of an 847.5 kHz subcarrier with NRZ-L encoded data. The RF field is continuously on for Type B communications.

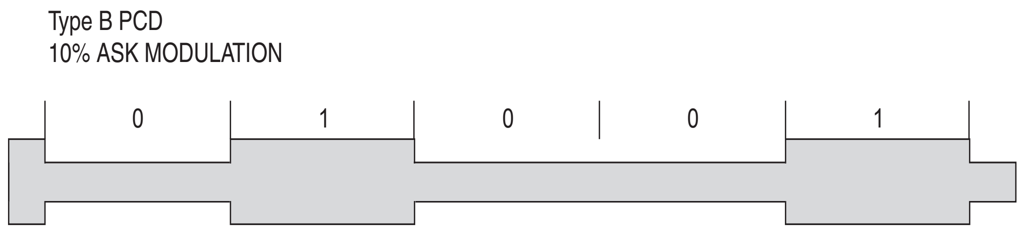


Figure 4. NRZ Encoding, Type B

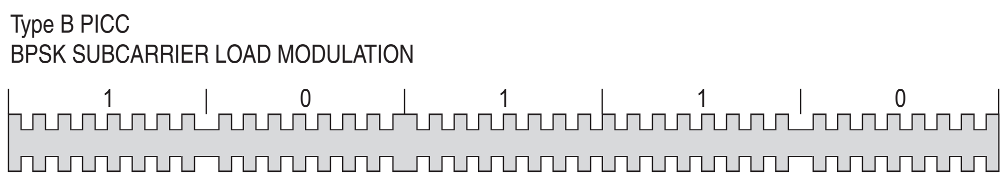
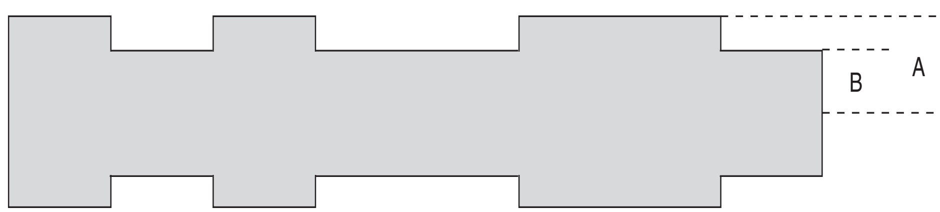


Figure 5. NRZ-L Encoding, Type B

Modulation Index

The amplitude modulation (ASK) requirements for Type B signals produced by the reader are described in Section 9 of Part 2 in terms of the Modulation Index. The “10% ASK” modulation requirement specifies that the modulation index be between 8% and 14%.



$$\text{Modulation Index} = \frac{(A - B)}{(A + B)}$$

$$\text{Modulation Depth} = \frac{B}{A}$$

where:

A = Unmodulated Signal Amplitude

B = Modulated Signal Amplitude

Figure 6. Type B Modulation Waveform and Formulas

Figure 6 shows a waveform and formula for the modulation index, as defined in ISO/IEC 14443-2. The modulation depth formula commonly used is also shown. Table 2 lists the modulation index calculation along with modulation depth calculated in the conventional manner.

Modulation Index	Modulation Depth
8%	85.2%
9%	83.5%
10%	81.8%
11%	80.2%
12%	78.6%
13%	77.0%
14%	75.4%

Table 2. Modulation Index Calculation vs. Modulation Depth

As shown in Table 2, the modulation index number is about half of what might be expected. Users designing Type B readers for the first time often misinterpret the "10% ASK" modulation index requirement and set the modulation depth to 90% (a 5% modulation index).

The rise and fall times of the modulation envelope must be 2 microseconds or less as shown in Section 9.1.2 of ISO/IEC 14443-2. The overshoot and undershoot may not exceed [0.1(A - B)] in amplitude.

Subcarrier Modulation

Type B readers continuously transmit the unmodulated 13.56 MHz RF carrier frequency when not transmitting data to the PICC. The PICC communicates with the PCD by modulating the load on the card antenna using an 847.5 kHz subcarrier and BPSK encoded data. The subcarrier may only be transmitted by the PICC when it is transmitting data. Each bit period is 8 subcarrier periods long and phase shifts can only occur at the nominal positions of rising or falling edges of the subcarrier as shown below.

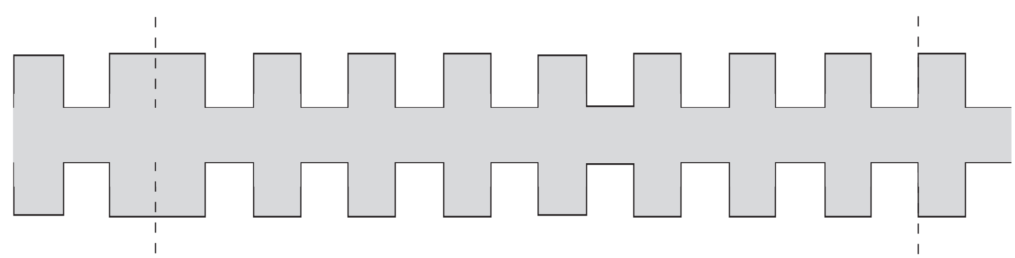


Figure 7. One Bit Period contains Eight Subcarrier Cycles

In practice there are several ways that an IC can produce load modulation. Load modulation is produced by switching either an internal resistor or capacitor in and out of the antenna circuit. The internal component is connected across the IC's antenna pins, placing it in parallel with the external antenna coil. Switching a resistor into the circuit increases the current through the card antenna. Switching a capacitor into the circuit changes the resonant frequency of the card antenna circuit. In both cases, the load on the reader antenna changes, producing a weak signal to be detected by the PCD demodulator.

The amplitude of the load-modulated signal induced in the reader antenna is specified in Section 9.2.2 of Part 2 of the ISO spec. The load modulation test is performed at both Hmin and Hmax using the procedure and hardware specified in ISO/IEC 10373-6 Section 7. Discussion of this proximity card qualification test is beyond the scope of this application note.

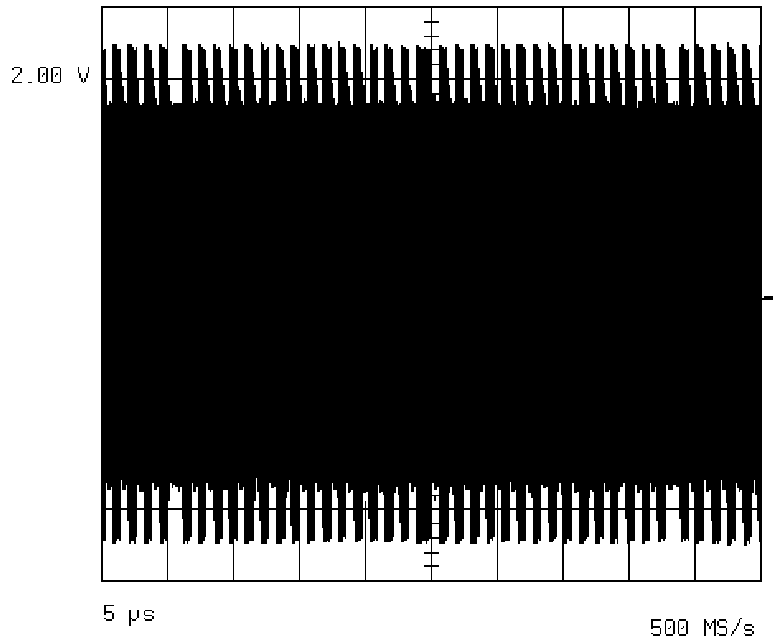


Figure 8. Load-Modulated Signal on the PICC antenna

Data Format

Data communication between the card and reader is performed using an LSB-first data format. Each byte of data is transmitted with a “0” start bit and a “1” stop bit as shown in Figure 9. The stop bit, start bit, and each data bit are one elementary time unit (ETU) in length (9.439 µS). ISO/IEC 14443 defines a character as consisting of a start bit, eight data bits (LSB-first), and a stop bit.

Each character may be separated from the next character by extra guard time (EGT). The EGT may be zero or a fraction of an ETU. EGT may not exceed 19 µS for data transmitted by the PICC, or 57 microseconds for data transmitted by the PCD. The position of each bit is measured relative to the falling edge of the start bit.

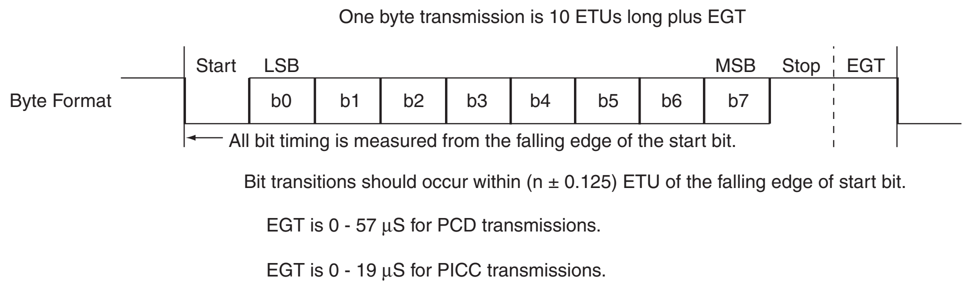


Figure 9. Format of One Byte of Data

Despite the fact that data transmissions occur LSB-first, all of the commands and data in ISO/IEC 14443 are listed in the conventional manner, with MSB on the left and LSB on the right.

Frame Format

Data transmitted by the PCD or PICC is sent as frames. The default frame consists of the Start of Frame (SOF), several characters, and the End of Frame (EOF). The SOF and EOF requirements are illustrated in Figure 10.

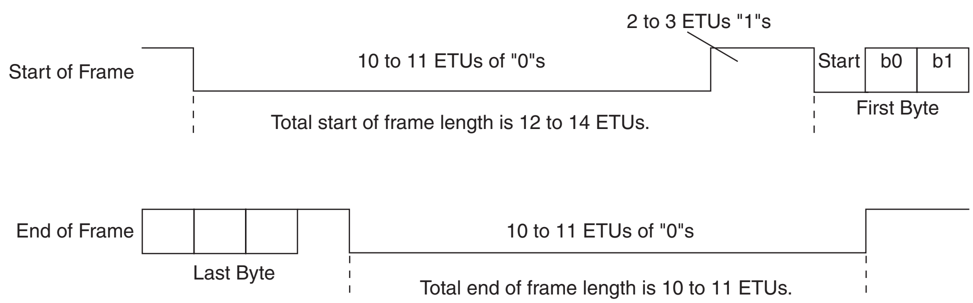


Figure 10. SOF/EOF Requirements

Reader Data Transmission

The unmodulated 13.56 MHz carrier signal amplitude that is transmitted when the reader is idle is defined as logical “1”, while the modulated signal level is defined as logical “0”. A frame transmitted by the reader consists of SOF, several characters of data followed by a two-byte CRC_B, and the EOF.

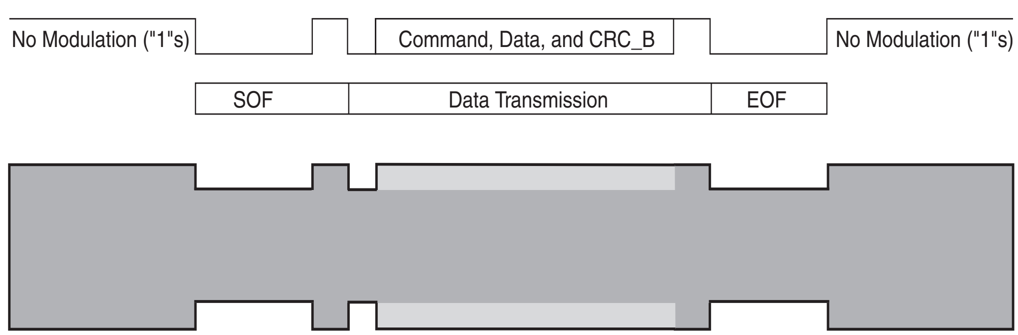


Figure 11. PCD Communication Frame

Card Data Transmission

Part 2 of ISO/IEC 14443 specifies that the PICC waits silently for a command from the PCD after being activated by the RF field. After receiving a valid command from the PCD, the PICC will turn on the subcarrier only if it intends to transmit a response. The PICC response consists of TR1, SOF, several characters of data followed by a two-byte CRC_B, and the EOF. The subcarrier must be turned off no later than 2 ETUs after the EOF.

The subcarrier is turned on and remains unmodulated for a time period known as the synchronization time (TR1). The phase of the subcarrier during TR1 defines logical “1” and permits the PCD demodulator to lock on to the subcarrier signal. The subcarrier must remain on until after the EOF transmission is complete.

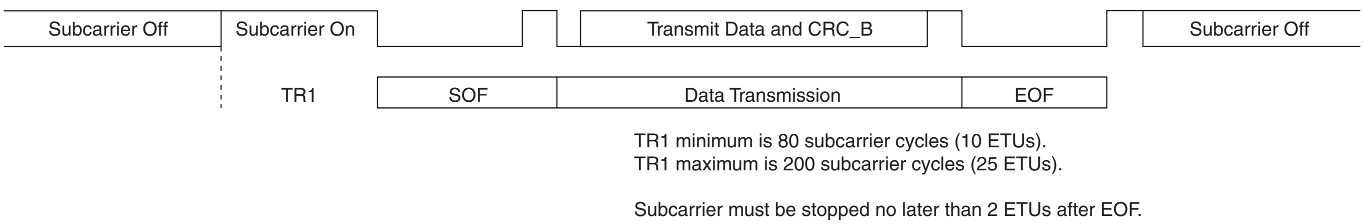


Figure 12. PICC Communication Frame

Response Timing

After the PICC receives a command from the PCD, it is not permitted to transmit a subcarrier during the guard time (TR0). The minimum guard time is eight ETUs for all command responses. The maximum guard time is defined by the frame waiting time (FWT), except for the ATQB response (the response to REQB or Slot-MARKER polling commands), which has a maximum TR0 of 32 ETUs.

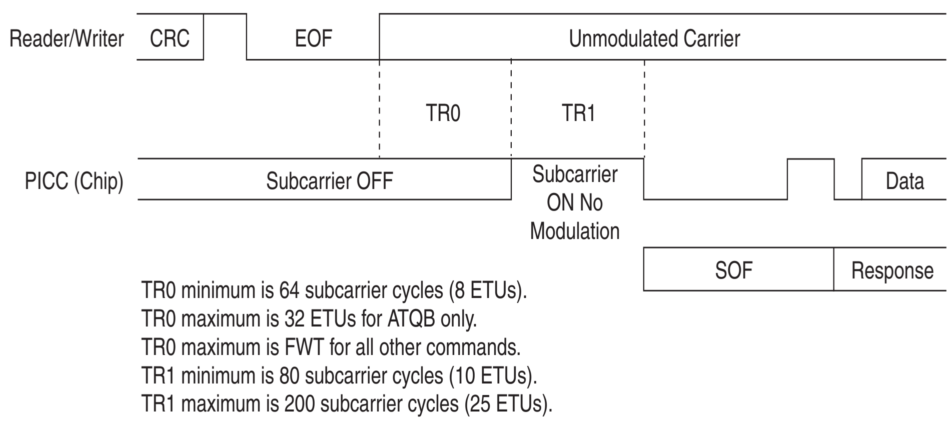


Figure 13. Guard Time TR0

The FWT is the maximum time that a PICC requires to begin a response. The PICC transmits a parameter in the ATQB response to the polling command that tells the reader the worst case FWT. See the Anticollision Commands and Responses section on page 14 for additional information on the ATQB response.

After the PICC response, the PCD is required to wait the Frame Delay Time (TR2) before transmission of the next command. The minimum frame delay time required for all commands is 14 ETUs as shown in Figure 14.

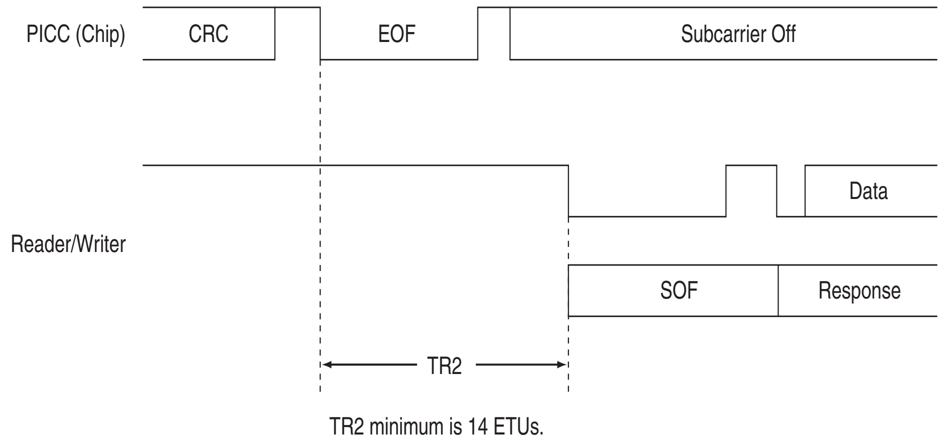


Figure 14. TR2 Frame Delay Time

CRC Error Detection

A 2-byte CRC_B is required in each frame transmitted by the PICC or PCD to permit transmission error detection. The CRC_B is calculated on all the command and data bytes in the frame. The SOF, EOF, start bits, stop bits, and EGT are not included in the CRC_B calculation. The 2-byte CRC_B follows the data bytes in the frame.

SOF	K Data Bytes	CRC1	CRC2	EOF

Figure 15. CRC_B Byte Order

The CRC computation is defined in ISO/IEC 13239. The initial value of the register used for the CRC_B calculation is all ones ($FFFF). In hardware the CRC_B encoding and decoding is carried out by a 16-stage cyclic shift register with appropriate feedback gates.

In the example shown above, the CRC_B is calculated on the K data bytes and then appended to the data. CRC1 is the least significant byte and CRC2 is the most significant byte of the CRC_B. If the CRC_B was calculated as $5A6B (hexadecimal), then CRC1 is $6B and CRC2 is $5A. Each data and CRC byte is transmitted LSB-first.

Anticollision Protocol Options

This section of the application note describes the anticollision procedures for Type B as defined in Section 7 of Part 3. ISO/IEC 14443-3 describes two anticollision options for Type B PICCs: the timeslot procedure and the probabilistic procedure. PICCs designed for the probabilistic option do not support the Slot-MARKER command.

When the PICC enters the 13.56 MHz RF field of the reader (PCD), it performs a power on reset and waits silently for a valid Type B polling command. The PICC is required to be capable of accepting a polling command within 5 mS of being activated by the field. If the reader is of a multi-protocol design, then the PICC must be capable of accepting a polling command within 5 mS after the PCD has stopped Type A modulation.

Both the timeslot and the probabilistic anticollision protocols are described below. The PCD is permitted to implement these protocols in any manner that does not conflict with the requirements of part 3 of the standard. Atmel does not currently have any products supporting the probabilistic anticollision option.

A PICC State Transition Flow Diagram is provided in Section 7.4.1 of Part 3 of the ISO spec. A simplified version of this diagram is shown in Figure 16. Refer to this diagram while reading the descriptions of the two anticollision options.

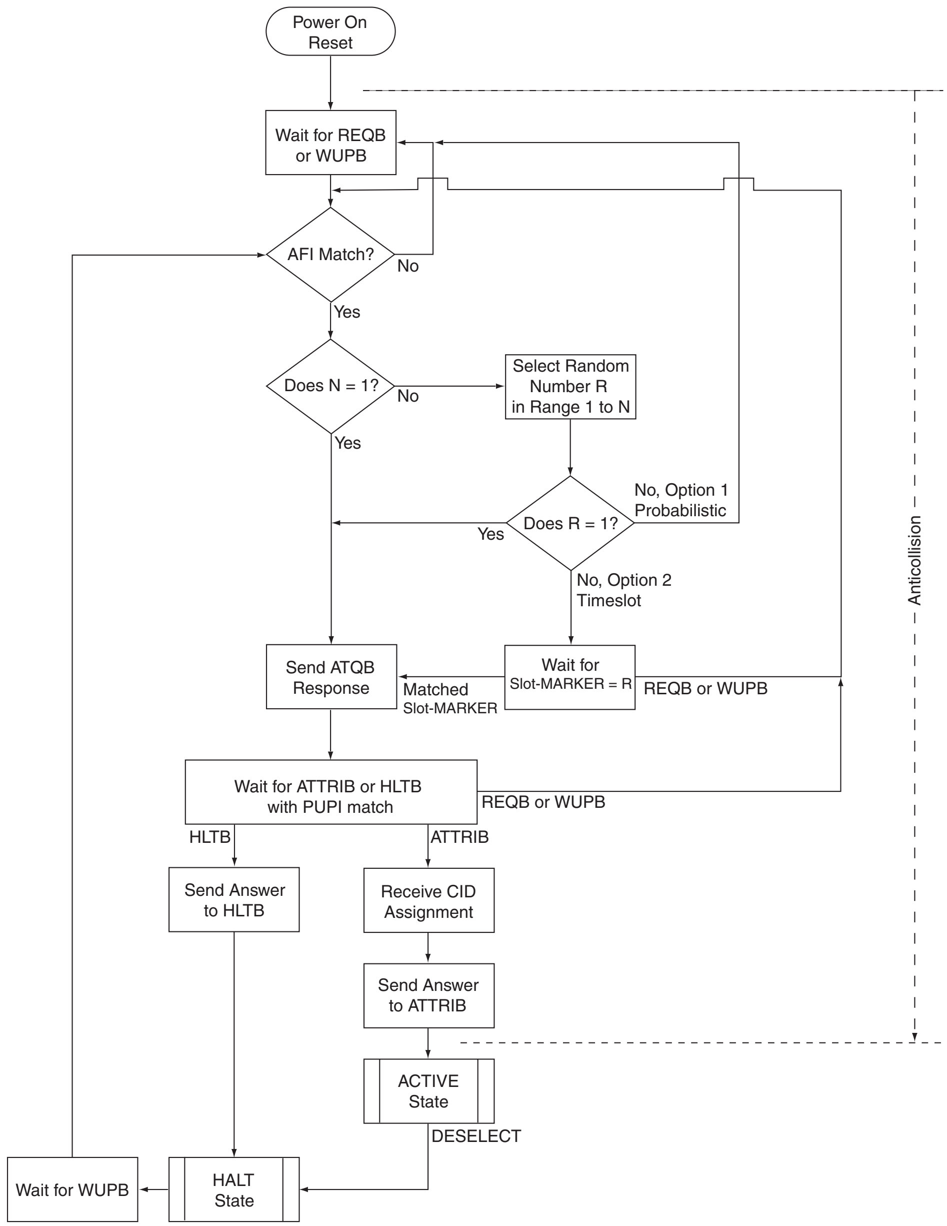


Figure 16. PICC State Transition Diagram

Timeslot Anticollision

The PCD initiates the anticollision process by issuing an REQB or WUPB polling command. The WUPB command activates any tag or card (PICC) in the field with a matching AFI code. The REQB command performs the same function, but does not affect a PICC in the Halt state. The REQB and WUPB commands contain an integer “N” indicating the number of slots assigned to the anticollision process for PICCs.

If “N” = 1 then all PICCs respond with the ATQB response. If “N” is greater than one, then the PICC selects a random number “R” in the range of 1 to “N”; if “R” = 1, then the

PICC responds with ATQB. If “R” is greater than 1, then the PICC waits silently for a Slot-MARKER command where the slot number “S” is equal to “R” and then responds with ATQB. The PCD polls all of the slots periodically to determine if any PICC is present in the field. The PICC is only permitted to respond in one slot of the “N” slots.

The ATQB response contains a PUPI card identification number that is used to direct commands to a specific PICC during the anticollision process. When the PCD receives an ATQB response, it can respond with a matching HLTB to halt the PICC, or it can respond with a matching ATTRIB command to assign a Card ID Number (CID) and place the PICC in the Active state. If the card does not support CIDs, then a CID code of $0 is sent.

Once placed in the Active state, the PICC is ready for transactions using the Active state commands. A PICC in the Active state ignores all REQB, WUPB, Slot-MARKER, ATTRIB, and HLTB commands.

A PICC in the Active state supporting CIDs ignores commands that do not contain a CID number that matches the CID assigned by the ATTRIB command. Up to 15 PICCs supporting CIDs can be active simultaneously. If the PICC does not support CIDs, then the PCD will place a single PICC in the Active state and complete the transaction with the card before placing it in the Halt state and continuing the anticollision procedure.

When the PCD receives an ATQB response with a CRC error, a collision is assumed to have occurred. Typically the PCD will complete transactions with any other PICCs in the field and then place them in the Halt State. The PCD will then issue a new REQB command, causing each PICC in the field that has not been Halted to select a new random number “R”. This procedure resolves the conflict between the previously colliding PICCs, allowing the PCD to communicate with them.

The anticollision process continues in this manner until all PICCs in the field have completed their transactions. Any command received by the PICC during the anticollision process with a CRC error or frame format error is ignored.

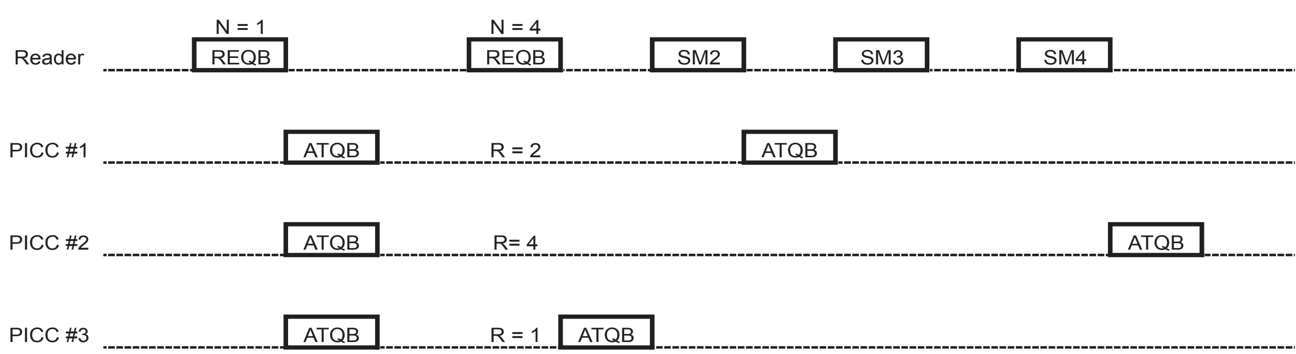


Figure 17. Timeslot Anticollision Example

An example of polling using timeslot anticollision is shown in Figure 17. After transmitting REQB with N = 1, all three PICCs in the field respond, resulting in a collision. Sending REQB with N = 4 causes each PICC to select “R” using an internal random number generator. The PICC responds only to the Slot-MARKER matching “R”. Note that the Slot-MARKER commands may be transmitted by the reader in any order.

Probabilistic Anticollision

The PCD initiates the anticollision process by issuing an REQB or WUPB polling command. The WUPB command activates any tag or card (PICC) in the field with a matching AFI code. The REQB command performs the same function but does not affect a PICC in the Halt state. The REQB and WUPB commands contain an integer "N" that is used to set the probability of response to the polling command equal to 1/"N".

If "N" = 1, then all PICCs respond with the ATQB response. If "N" is greater than one, then the PICC selects a random number "R" in the range of 1 to "N". If "R" = 1, then the PICC responds with ATQB. If "R" is greater than 1, then the PICC returns to the Idle state and waits for a polling command. Each time the PICC receives a polling command, it selects a new random number "R".

The ATQB response contains a PUPI card identification number that is used to direct commands to a specific PICC during the anticollision process. When the PCD receives an ATQB response, it can respond with a matching HLTB to Halt the PICC, or it can respond with a matching ATTRIB command to assign a Card ID Number (CID) and place the PICC in the Active state. If the card does not support CIDs, then a CID code of $0 is sent.

Once placed in the Active state the PICC is ready for transactions using the Active state commands. A PICC in the Active state ignores all REQB, WUPB, Slot-MARKER, ATTRIB, and HLTB commands.

A PICC in the Active state supporting CIDs ignores commands that do not contain a CID number that matches the CID assigned by the ATTRIB command. Up to 15 PICCs supporting CIDs can be active simultaneously. If the PICC does not support CIDs, then the PCD will place a single PICC in the Active state and complete the transaction with the card before placing it in the Halt state and continuing the anticollision procedure.

When the PCD receives an ATQB response with a CRC error, then a collision is assumed to have occurred. The PCD will then issue a new polling command, causing each PICC in the field that has not been Halted to select a new random number "R".

The anticollision process continues in this manner until all PICCs in the field have completed their transactions. Any command received by the PICC during the anticollision process with a CRC error or frame format error is ignored.

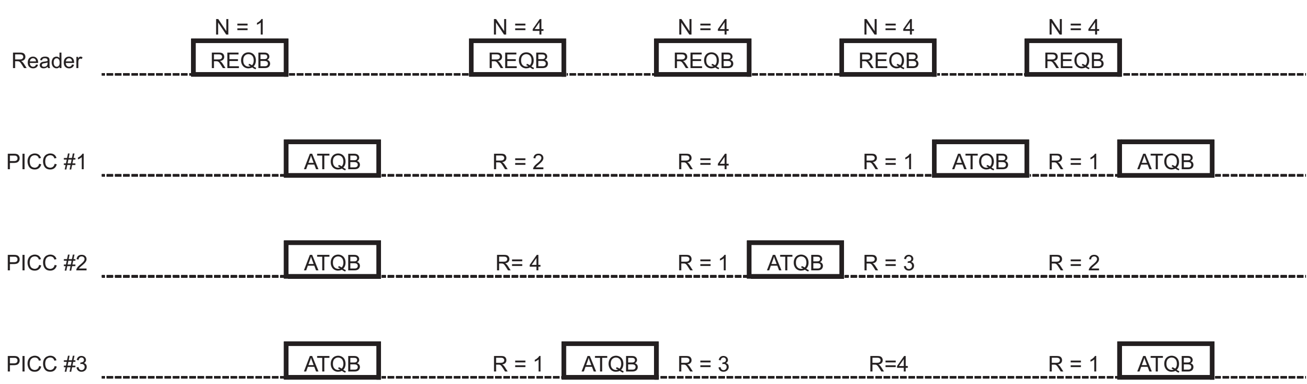


Figure 18. Example of Probabilistic Anticollision

An example of polling using probabilistic anticollision is shown in Figure 18. After transmitting REQB with N = 1, all three PICCs in the field respond, resulting in a collision. Sending REQB with N = 4 causes each PICC to select R using an internal random number generator. Only the PICC selecting R = 1 responds to the REQB command. Due to it's statistical nature, probabilistic anticollision is less likely to find every card in the field than Timeslot anticollision.

Anticollision Commands and Responses

Part 3 of the standard defines the commands and responses for initialization and anticollision of Type B cards. The coding of the first byte of the commands and responses is shown in Table 3 and Table 4. The coding of the complete command and response frames are shown in the following sections of the application note.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command Name	Hexadecimal
0	0	0	0	0	1	0	1	REQB/WUPB	$05
Slot Number				0	1	0	1	Slot-MARKER	$s5
0	0	0	1	1	1	0	1	ATTRIB	$1D
0	1	0	1	0	0	0	0	HLTB	$50

Table 3. Type B Commands

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command Name	Hexadecimal
0	1	0	1	0	0	0	0	ATQB	$50
MBLI				CID				Answer to ATTRIB	$mc
0	0	0	0	0	0	0	0	Answer to HLTB	$00

Table 4. Type B Responses

REQB/WUPB Command

The Request B (REQB) and Wake-Up B (WUPB) commands are used to probe the RF field for Type B PICCs as the first step in the anticollision process. The response to an REQB or WUPB command is the Answer to Request B (ATQB).

	Reader	PICC	
Command >	$05		
Family/Sub-family ID>	AFI		
PARAM Byte >	$0 | R/W “N”		“N” is # of Slots
	CRC1		
	CRC2		
ATQB Response >		$50	
		PUPI 0	
		PUPI 1	PUPI Identifier
		PUPI 2	
		PUPI 3	
		APP 0	
		APP 1	Application Data
		APP 2	
		APP 3	
		Protocol 1	Bit Rate Capacity
		Protocol 2	Max Frame Size/-4 Info
		Protocol 3	FWI/Coding Options
		CRC1	
		CRC2	

Figure 19. REQB/WUPB Command and Response

The Application Family Identifier (AFI) is used to select the family and subfamily of cards which the PCD is targeting. Only PICCs with a matching AFI code are permitted to answer an REQB or WUPB command. Table 5 describes the AFI matching criteria.

AFI High Bits	AFI Low Bits	REQB/WUPB Polling Produces a PICC Response From:
$0	$0	All Families and Sub-Families
X	$0	All Sub-Families of Family X
X	Y	Only Sub-Family Y of Family X
$0	Y	Proprietary Sub-Family Y only

Note: Y = $1 to $F
X = $1 to $F

Table 5. AFI Matching Criteria

Using the matching criteria, the AFI code transmitted by the PCD is compared to the PICC AFI code. For example, if the PICC AFI register contains $3B [Family 3, Subfamily B], then an AFI match would occur only if the PCD transmits an AFI of $3B, or $30, or $00. An AFI of $00 activates all Type B PICCs. The AFI code family definitions from Part 3 of the standard are shown in Table 6.

AFI High Bits	AFI Low Bits	Application Family	Examples
$0	Y	Proprietary	
$1	Y	Transport	Mass Transit, Bus, Airline
$2	Y	Financial	Banking, Retail, Electronic Purse
$3	Y	Identification	Access Control
$4	Y	Telecommunication	Telephony, GSM
$5	Y	Medical	
$6	Y	Multimedia	Internet Services
$7	Y	Gaming	
$8	Y	Data Storage	Portable Files
$9 - $F	Y	RFU	Not Currently Defined by 14443-3

Note: Y = $1 to $F

Table 6. AFI Code Family Definitions

The REQB and WUPB commands contain the parameter “N”, which assigns the number of slots available for the anticollision process. The coding of “N” is shown in Table 7. “N” values that are reserved for future use (RFU) are prohibited.

Bit 2	Bit 1	Bit 0	N
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	RFU
1	1	x	RFU

Table 7. Coding of “N” Anticollision Parameter

Selection of the REQB or WUPB command is determined by the value of Bit 3 of the PARAM byte as shown in Table 8. The REQB activates PICCs in the Idle or Ready states. The WUPB activates PICCs in the Idle or Ready states and wakes up PICCs in the Halt state.

Bit 3	
0	REQB
1	WUPB

Table 8. Coding of REQB/WUPB Selection Bit

Slot-MARKER Command

After an REQB or WUPB command with "N" greater than 1 is issued and the ATQB response (if any) is received, the PCD will transmit Slot-MARKER commands with slot values "S" of 2 to "N" to define the start of each timeslot for anticollision. If the random number "R" selected by the PICC matches "S", then the PICC responds with ATQB. The Slot-MARKER commands are not required to be issued in any particular order.

	Reader	PICC	
Command >	slot | $5		
	CRC1		
	CRC2		
ATQB Response >		$50	
		PUPI 0	
		PUPI 1	PUPI Identifier
		PUPI 2	
		PUPI 3	
		APP 0	
		APP 1	Application Data
		APP 2	
		APP 3	
		Protocol 1	Bit Rate Capacity
		Protocol 2	Max Frame Size/-4 Info
		Protocol 3	FWI/Coding Options
		CRC1	
		CRC2	

Figure 20. Slot-MARKER Command and Response

The slot number portion of the command byte is coded as shown in Table 9.

Bit 7	Bit 6	Bit 5	Bit 4	Slot
0	0	0	0	Not Supported
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 9. Coding of Slot Number

ATQB Response

The Answer to Request B (ATQB) response to the REQB, WUPB, and Slot-MARKER commands transmits the PUPI identifier and important protocol information to the reader. The format of the response is shown in Figure 21. Note that the PUPI is not required to be a fixed value; the PICC is permitted to generate random PUPI values.

$50	
PUPI 0	
PUPI 1	PUPI Identifier
PUPI 2	
PUPI 3	
APP 0	
APP 1	Application Data
APP 2	
APP 3	
Protocol 1	Bit Rate Capacity
Protocol 2	Max Frame Size/-4 Info
Protocol 3	FWI/Coding Options
CRC1	
CRC2	

Figure 21. ATQB Response Format

The three protocol bytes communicate to the reader if the PICC supports optional communication features or functionality. Protocol Byte 1 is $00 if the PICC communicates at only the standard data rate of 106 kbits per second (kbps) in each direction. Table 19 in Part 3 contains the coding of Protocol Byte 1 for PICCs supporting higher data rates.

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Protocol 1
Bit Rates Supported by PICC								

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Protocol 2
Max_Frame_Size				-4 Compliance Info				

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Protocol 3
FWI				ADC		FO		

Figure 22. ATQB Protocol Byte Field Definitions

Protocol Byte 2 contains the Part 4 compliance code and maximum frame size supported by the PICC. A value of $0 in the -4 compliance bits indicates the PICC is not compliant with ISO/IEC 14443-4, while a value of $1 indicates Part 4 compliance. The coding of the PICC maximum frame size bits is shown below.

Bit 7	Bit 6	Bit 5	Bit 4	Max Frame
0	0	0	0	16 Bytes
0	0	0	1	24 Bytes
0	0	1	0	32 Bytes
0	0	1	1	40 Bytes
0	1	0	0	48 Bytes
0	1	0	1	64 Bytes
0	1	1	0	96 Bytes
0	1	1	1	128 Bytes
1	0	0	0	256 Bytes
1	x	x	x	RFU

Table 10. Coding of PICC Maximum Frame Size Bits in ATQB Protocol Byte 2

Protocol Byte 3 contains the Frame Waiting Time Integer (FWI) bits, which defines the Frame Waiting Time (FWT), the maximum amount of time that the PCD should wait for a response from the PICC. Table 11 shows the FWI coding and FWT in terms of elementary time units and microseconds using the formula in Part 3 of the standard. Warning: The FWT formula is changed in Amendment 1 to part 3 of the standard, reducing all FWT values by TR1 (10 ETUs minimum). To guarantee backward compatibility, a PCD should calculate FWT using the formula in the unamended base standard.

Bit 7	Bit 6	Bit 5	Bit 4	FWT	FWT Time
0	0	0	0	32 ETUs	302.1 µS
0	0	0	1	64 ETUs	604.1 µS
0	0	1	0	128 ETUs	1208.3 µS
0	0	1	1	256 ETUs	2416.5 µS
0	1	0	0	512 ETUs	4833.0 µS
0	1	0	1	1024 ETUs	9666.1 µS
0	1	1	0	2048 ETUs	19332.2 µS
0	1	1	1	4096 ETUs	38664.3 µS
1	0	0	0	8192 ETUs	77328.6 µS
1	0	0	1	16384 ETUs	154657.2 µS
1	0	1	0	32768 ETUs	309314.5 µS

Table 11. Coding of FWI in ATQB Protocol Byte

Bit 7	Bit 6	Bit 5	Bit 4	FWT	FWT Time
1	0	1	1	65536 ETUs	618628.9 µS
1	1	0	0	131072 ETUs	1237257.8 µS
1	1	0	1	262144 ETUs	2474515.6 µS
1	1	1	0	524288 ETUs	4949031.3 µS
1	1	1	1	RFU	RFU

Table 11. Coding of FWI in ATQB Protocol Byte (Continued)

The Frame Option (FO) and Application Data Coding (ADC) are also defined in Protocol Byte 3. The Frame Option bits show support of the CID or NAD by the PICC. The CID is used for identification of multiple cards in the Active state. The NAD is used to define logical connections for Part 4 compliant communications.

Bit 1	Bit 0	Frame Option
1	x	NAD is supported by the PICC
x	1	CID is supported by the PICC

Table 12. Coding of FO Bits in Protocol Byte 3

Bit 3	Bit 2	Application Data Encoding
0	0	Application is proprietary
0	1	Application bytes coded per 7.9.3 of Part 3

Table 13. Coding of ADC bits in Protocol Byte 3

If the ADC bits indicate a proprietary application, then the four application data bytes in the ATQB response may contain any application data. If the application is not proprietary, then the application bytes are defined as follows: the first byte (APP 0) is the AFI of the PICC, the fourth byte (APP 3) contains the number of applications in the PICC, and the second and third bytes contain the CRC_B of the AID as defined in ISO/IEC 7816-5. The AID is a multibyte application identifier code which identifies an application provider or issuer and indicates if the application provider is registered with ISO or a national standards body.

ATTRIB Command

Sending the ATTRIB command (with a matching PUPI) after an ATQB response selects the PICC and places it in the Active State. It also assigns the CID to the PICC and sets the optional communication parameters. The ATTRIB command may also contain an embedded high layer command (in the INF bytes) if the PICC supports Part 4.

	Reader	PICC
Command >	$1D	
	PUPI 0	
PUPI of PICC >	PUPI 1	
	PUPI 2	
	PUPI 3	
Timing Settings >	PARAM 1	
PCD Max Frame Size >	PARAM 2	
PICC -4 Info >	PARAM 3	
CID Assignment	PARAM 4	
	Optional INF Bytes	
	CRC1	
	CRC2	

ATTRIB Response >	MBLI	CID
	Response to INF Bytes	
	CRC1	
	CRC2	

Figure 23. ATTRIB Command and Response

If the PICC does not support Part 4 commands, then no INF bytes may be sent. For PICCs that support Part 4, any number of INF bytes may be sent up to the limit of the maximum frame size that the PICC reported in the ATQB response. If a PICC processes a high layer command, then it should report the response in the answer to ATTRIB (any number of INF bytes).

If the PICC does not support Part 4 or the ATTRIB command did not contain INF bytes, then the answer to ATTRIB response is not permitted to contain INF bytes. The lower four bits echo back the CID value assigned by ATTRIB. The upper four bits of the ATTRIB response are the Maximum Buffer Length Index (MBLI), which communicates to the PCD how many bytes the PICC is capable of receiving as a chained frame. If the PICC does not support chained frames, then this parameter is $0.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Param 1
Min TR0		Min TR 1		EOF	SOF	0	0	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Param 2
Bit Rate Settings				PCD Max_Frame_Size				

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Param 3
0	0	0	0	Echo -4 Compliance Info				

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Param 4
0	0	0	0	CID Assigned				

Figure 24. ATTRIB Parameter Byte Field Definition

The Param 1 byte contains $00 for PICCs that support only the default settings for minimum TR0 and minimum TR1, and require both a SOF and EOF. If the PICC and PCD support shorter TR0 and TR1 times or do not require SOF or EOF, then these bits can be set as described in Section 7.10.3 of Part 3 of the ISO spec to configure the PICC to the optional settings. Bits 0 and 1 are RFU.

If the PICC supports higher than standard bit rates, then bits 4 through 7 of Param 2 can be set as described in Section 7.10.4 of Part 3 of the ISO spec. See Amendment 1 to ISO/IEC 14443-3 for details on the optional high data rates. For the standard 106 kbps data rate this parameter is $0. The PCD Maximum Frame Size bits of Param 2 are coded as shown below.

Bit 3	Bit 2	Bit 1	Bit 0	Max Frame
0	0	0	0	16 Bytes
0	0	0	1	24 Bytes
0	0	1	0	32 Bytes
0	0	1	1	40 Bytes
0	1	0	0	48 Bytes
0	1	0	1	64 Bytes
0	1	1	0	96 Bytes
0	1	1	1	128 Bytes
1	0	0	0	256 Bytes
1	x	x	x	RFU

Table 14. Coding of PCD Maximum Frame Size Bits of Param 2

The upper four bits of Param 3 are RFU. In the lower four bits, the PICC Part 4 compliance bits that were received by the PCD in the ATQB response (Protocol Byte 2) are echoed back to the PICC. A value of $0 in the -4 compliance bits indicates the PICC is not compliant with Part 4, while a value of $1 indicates compliance.

The upper four bits of Param 4 are also RFU. The lower four bits are used to assign a unique CID to the PICC. If the PICC does not support CIDs, then $0 is sent. The CID in ATTRIB Param 4 and the Answer to ATTRIB Response are coded as shown in Table 15.

Bit 3	Bit 2	Bit 1	Bit 0	CID
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	RFU

Table 15. Coding of CID in ATTRIB Param 4 and Answer to ATTRIB Response

HLTB Command

Sending the Halt B (HLTB) command (with a matching PUPI) after an ATQB response places the PICC in the Halt state. The Answer to HLTB is $00. After responding to HLTB, the PICC will ignore all commands except WUPB.

	Reader	PICC
Command >	$50	
	PUPI 0	
PUPI of PICC >	PUPI 1	
	PUPI 2	
	PUPI 3	
	CRC1	
	CRC2	
HLTB Response >		$00
		CRC1
		CRC2

Figure 25. HLTB Command and Response

Part 4 Block Transmission Protocol

Part 4 of ISO/IEC 14443 describes a half-duplex block transmission protocol that can be used when the PICC is in the Active state. The protocol is beyond the scope of this application note; however, the coding of the command bytes is shown in Table 16 and Table 17 for reference. Part 4 is supported by Atmel Secure Microcontroller products with contactless interfaces.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command Name	Hexadecimal
1	1	0	0	CID	0	1	0	DESELECT S-Block	$C2/CA
1	1	1	1	CID	0	1	0	WTX S-Block	$F2/FA
0	0	0	Chain	CID	NAD	1	Block	I-Block	$0x/1x

Table 16. Type B Commands

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command Name	Hexadecimal
1	0	1	ACK	CID	0	1	Block	R-Block ACK	$Ax
1	0	1	NAK	CID	0	1	Block	R-Block NAK	$Bx

Table 17. Type B Responses

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