

ADFP Cell-Based IC Physical Design and Verification with Innovus

Presenter : 邱奕綸

Date : 2025.11.3

Outline

1. Pre-requirement
2. Assign Problem and Change Naming Rule Script
3. Design Import
4. Initial Step
5. Floor Plan
6. Power Plan
7. Power Route
8. Placement
9. CTS
10. Route
11. Post processing
12. Post Layout Simulation
13. HomeWork Requirment

Pre-requirement

- ▶ **Gate-Level netlist(Verilog)**
- ▶ **TestBench and Pattern**
- ▶ **SDC constraints**
- ▶ **Physical Library(ADFP製程LEF)**
- ▶ **Timing Library(ADFP製程LIB)**
- ▶ **Multi Mode Multi Corner MMMC.view.stylus**

資料夾建立

- ▶ 1.pipeline版本的資料夾底下建立一個APR的資料夾
- ▶ 2.APR資料夾內建立dbs(存檔存放位置)outputs資料夾，同時把script和mmmc放入資料夾內

/home/m133040041/HDL/HW3/

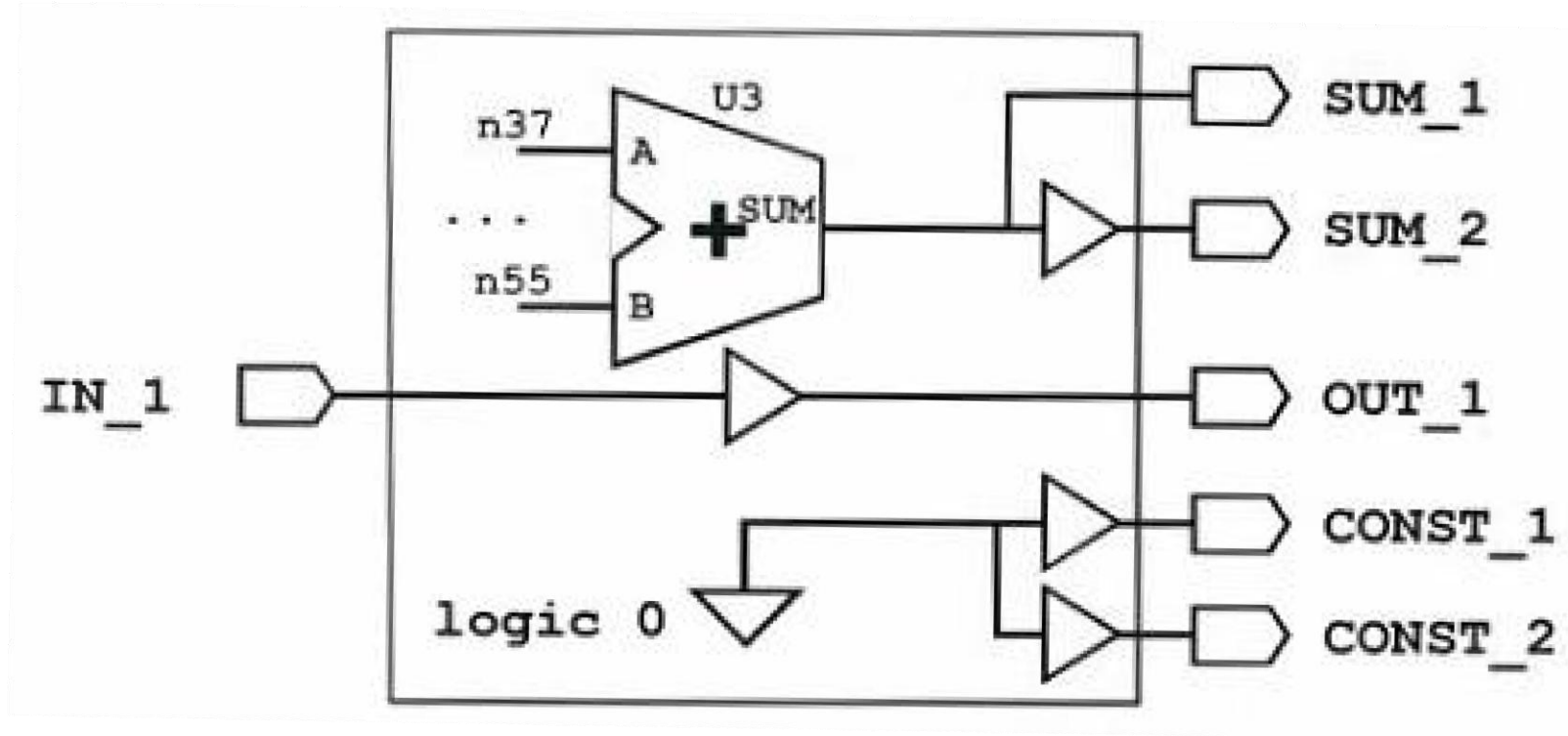
Name	Last modified	Owner
..		
APR	2025-10-30 10:41	m133040041
compile	2025-10-30 10:55	m133040041
compile_apr	2025-10-30 10:55	m133040041
gate_level	2025-10-30 10:55	m133040041
post_sim	2025-10-30 10:56	m133040041
pre_sim	2025-10-30 10:55	m133040041
pt	2025-10-30 10:55	m133040041
rtl	2025-10-30 10:55	m133040041



dbs	2025-10-02...	m133
lab_script	2025-10-02...	m133
outputs	2025-10-02...	m133
mmmc.view.stylus	2	2025-10-02... m133

Assign Problem and Change Naming Rule Script(1/2)

- ▶ The syntax of “assign” may cause problems in the LVS



- ▶ To ensure that your final netlist does not contain assign statements, separate the multiple port nets
- ▶ during compile. (一定要在合成前做以下指令在進行合成)
- ▶ `dc_shell > set_fix_multiple_port_nets -all -buffer_constants [get_designs *]`

Assign Problem and Change Naming Rule Script(2/2)

- ▶ The wrong naming rules may cause problems in the LVS
- ▶ 在合成完後加入以下指令
- ▶ `set bus_inference_style {%s[%d]}`
- ▶ `set bus_naming_style {%s[%d]}`
- ▶ `set hdlout_internal_busses true`
- ▶ `change_names -hierarchy -rule verilog`
- ▶ `define_name_rules name_rule -allowed "A-Z a-z 0-9 _" -max_length 255 -type cell`
- ▶ `define_name_rules name_rule -allowed "A-Z a-z 0-9 _[]" -max_length 255 -type net`
- ▶ `define_name_rules name_rule -map {"*cell\\"*"cell"}`
- ▶ `define_name_rules name_rule -case_insensitive`
- ▶ `change_names -hierarchy -rules name_rule`

```
assign \A[19] = A[19];  
assign \A[18] = A[18];  
assign \A[17] = A[17];  
assign \A[16] = A[16];  
assign \A[15] = A[15];  
assign ABSVAL[19] = \A[19];  
assign ABSVAL[18] = \A[18];  
assign ABSVAL[17] = \A[17];  
assign ABSVAL[16] = \A[16];  
assign ABSVAL[15] = \A[15];
```



```
BUFX1 X37X( .I(A[19]), .Z(ABSVAL[19]) );  
BUFX1 X38X( .I(A[18]), .Z(ABSVAL[18]) );  
BUFX1 X39X( .I(A[17]), .Z(ABSVAL[17]) );  
BUFX1 X40X( .I(A[16]), .Z(ABSVAL[16]) );  
BUFX1 X41X( .I(A[15]), .Z(ABSVAL[15]) );
```

Warning: Verilog 'assign' or 'tran' statements are written out. (V0-4)

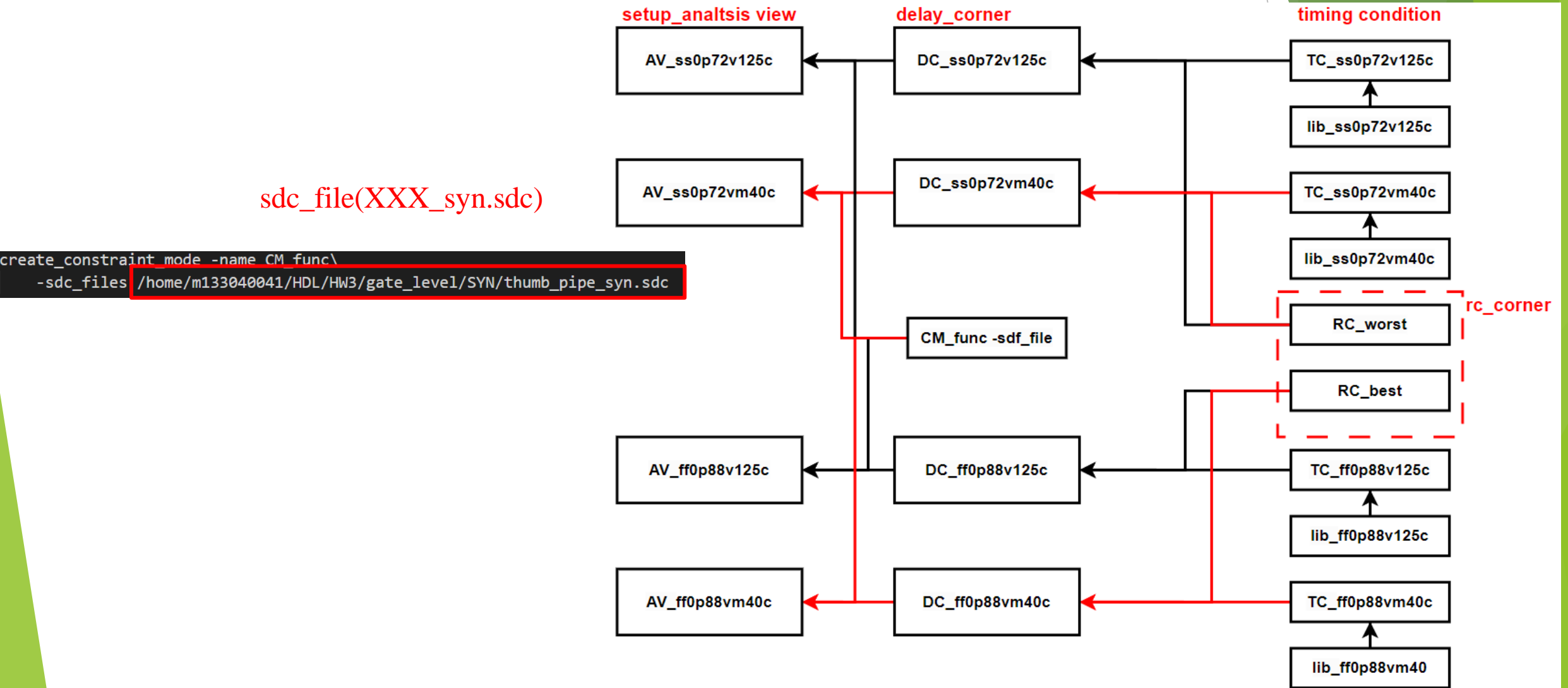
SDC File

需要將合成產生的.sdc檔案內的這幾行註解

```
set_units -time ns -resistance kOhm -capacitance pF -voltage V -current mA
set_operating_conditions -max ss0p72vm40c -max_library \
N16ADFP_StdCellss0p72vm40c_ccs\
- -min ff0p88v125c -min_library \
N16ADFP_StdCellff0p88v125c_ccs
set_wire_load_mode top
set_wire_load_model -name ZeroWireload -library N16ADFP_StdCellss0p72vm40c_ccs
set_max_area 0
set_ideal_network [get_ports clk]
```

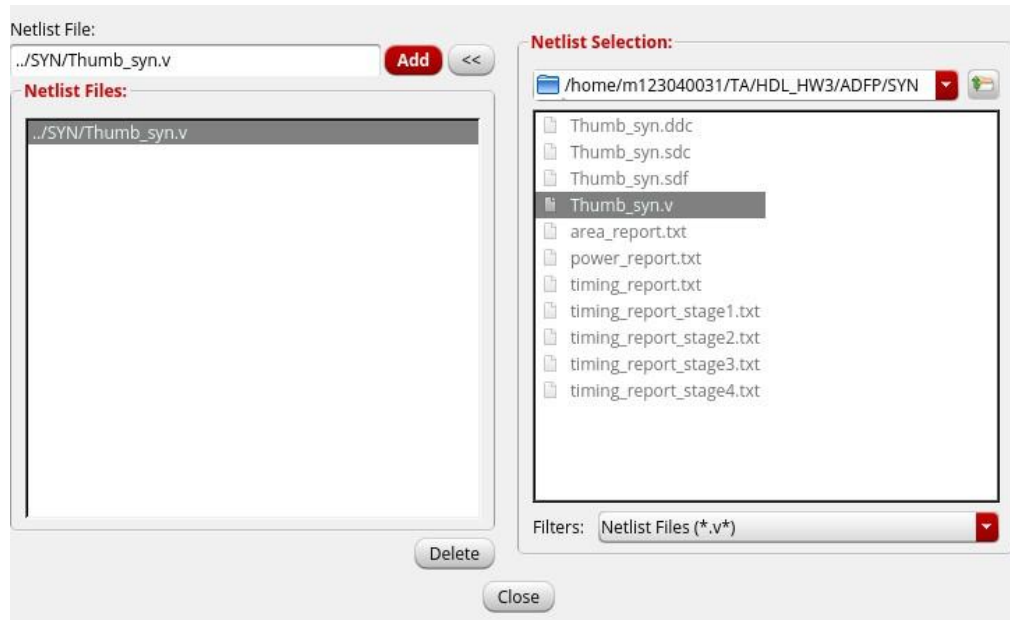
```
1 #####
2
3 # Created by write_sdc on Wed Sep 11 16:12:33 2024
4
5 #####
6 set sdc_version 2.1
7
8 #set_units -time ns -resistance kOhm -capacitance pF -voltage V -current mA
9 #set_operating_conditions -max ss0p72vm40c -max_library
10 #N16ADFP_StdCellss0p72vm40c_ccs\
11 #
12 #N16ADFP_StdCellff0p88v125c_ccs
13 #set_wire_load_mode top
14 #set_wire_load_model -name ZeroWireload -library N16ADFP_StdCellss0p72vm40c_ccs
15 #set_ideal_network [get_ports clk]
16 create_clock [get_ports clk] -period 2.5 -waveform {0 1.25}
17 set_clock_latency 0.2 [get_clocks clk]
18 set_clock_uncertainty 0.02 [get_clocks clk]
19 set_clock_transition -max -rise 0.1 [get_clocks clk]
20 set_clock_transition -max -fall 0.1 [get_clocks clk]
21 set_clock_transition -min -rise 0.1 [get_clocks clk]
22 set_clock_transition -min -fall 0.1 [get_clocks clk]
```

Multi Mode Multi Corner MMMC.view.stylus



Design import(1/4)

- ▶ **cd 進入APR資料夾，輸入tcsch**
- ▶ **Terminal 下輸入innovus -stylus**
- ▶ **1.File → Import Design → Netlist → Verilog → Files → ... →select your file and click Add**
- ▶ **2.Select By User,fill your design name**



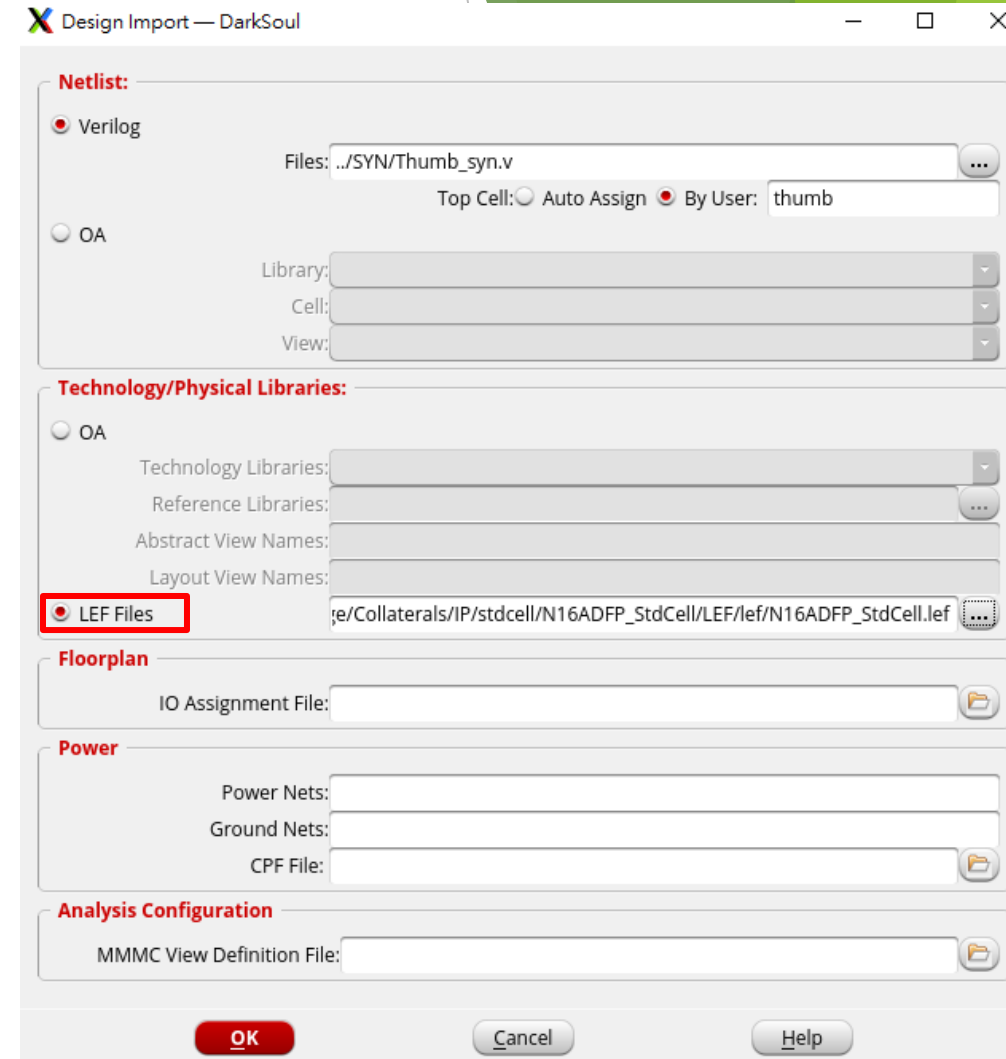
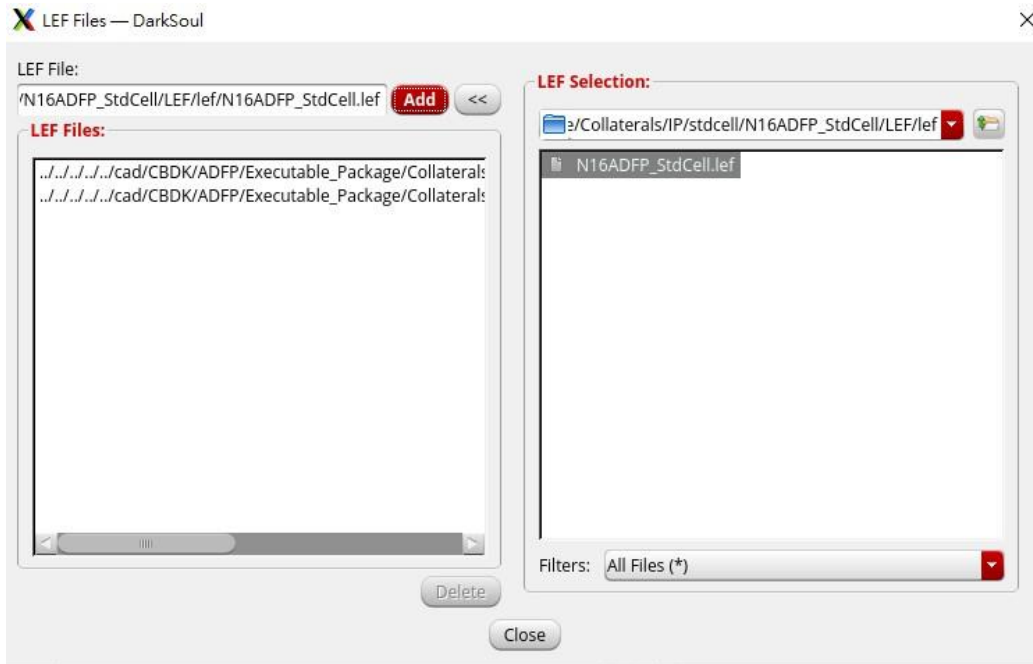
Design import(2/4)

▶ 3. Load process file

▶ LEF Files → ... → Filters : All Files(*) → add lef files

註：製程的technology lef一定要放第一個，其餘的無順序之分，不同製程有不同的名字，如果不知道的話就一個一個試，錯誤的話最後設定

完成後就會出現錯誤。(此範例為N16ADFP_APR_Innovus_11M.10a.tlef)



/cad/CBDK/ADFP/Executable_Package/Collaterals/Tech/APR/N16ADFP_APR_Innovus/N16ADFP_APR_Innovus_11M.10a.tlef
/cad/CBDK/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/LEF/lef/N16ADFP_StdCell.lef

Design import(3/4)

- ▶ 4.(Optional) IO Assignment File → add IO file
- ▶ 5.Power → Power Nets:VDD;Ground Nets:VSS

TSMC: VDD VSS
UMC: VCC GND

Design Import — DarkSoul

Netlist:

☒ Verilog

Files: .../SYN/Thumb_syn.v

Top Cell: ☐ Auto Assign ☒ By User: thumb

☐ OA

Library:

Cell:

View:

Technology/Physical Libraries:

☐ OA

Technology Libraries:

Reference Libraries:

Abstract View Names:

Layout View Names:

☒ LEF Files

.../Collaterals/IP/stdcell/N16ADFP_StdCell/LEF/lef/N16ADFP_StdCell.lef

Floorplan

IO Assignment File:

Power

Power Nets: VDD

Ground Nets: VSS

CPF File:

Analysis Configuration

MMMC View Definition File:

OK Cancel Help

如果有IO配置檔就放

Design import(4/4)

► 6. mmmc.view.stylus

Design Import — DarkSoul

Netlist:

☒ Verilog

Files: ...

Top Cell: ☐ Auto Assign ☒ By User:

☐ OA

Library:

Cell:

View:

Technology/Physical Libraries:

☐ OA

Technology Libraries:

Reference Libraries: ...

Abstract View Names:

Layout View Names:

☒ LEF Files

...

Floorplan

IO Assignment File: ...

Power

Power Nets:

Ground Nets:

CPF File: ...

Analysis Configuration

MMMC View Definition File: ...

mmmc.view.stylus

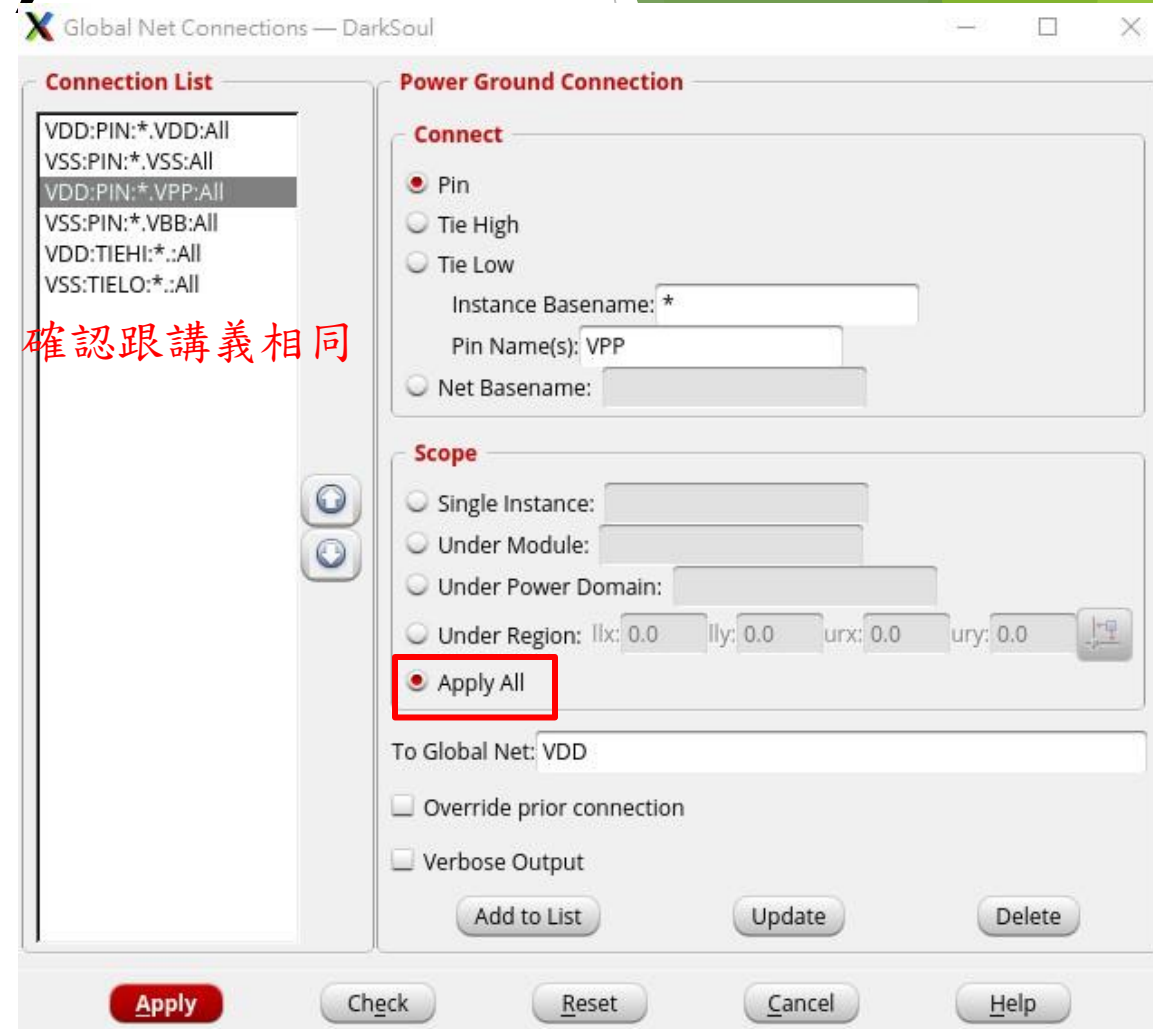
OK Cancel Help

Design import

- ▶ 如果import design 後有出現error message，1.先看是什麼地方出錯，並修正
- ▶ 2.重開innovus再 import一次

Initial Step(1/3)

- ▶ 1.Connect global power
- ▶ Power → Connect Global Nets → Connect:Pin → Pin Name(s): **VDD**;
Scope:Apply All; To Global Net: **VDD** → Add to List → Do it again but
change VDD to **VSS**
- ▶ Power → Connect Global Nets → Connect:Pin → Pin Name(s): **VPP**;
Scope:Apply All; To Global Net: VDD → Add to List
- ▶ Power → Connect Global Nets → Connect:Pin → Pin Name(s): **VBB**;
Scope:Apply All; To Global Net: VSS → Add to List
- ▶ Power → Connect Global Nets → Connect:Tie High → Scope:Apply All;
To Global Net: **VDD** → Add to List
- ▶ Power → Connect Global Nets → Connect:Tie Low → Scope: All;
To Global Net: **VSS** → Add to List→ Apply → Check → CloseApply
(Tie high Tie Low不要打Pin name)
- ▶ Apply
- ▶ Cancel



確認跟講義相同

Initial Step(2/3)

► **innovus** > source -quiet lab_script/config.tcl

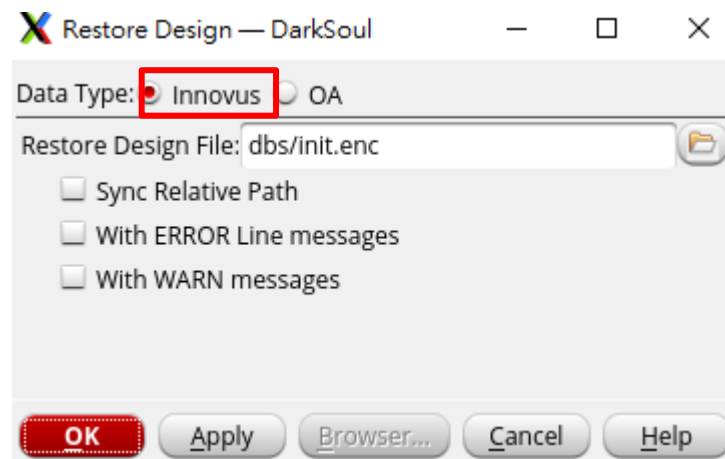
► **innovus** > source lab_script/config_cts.tcl

► **Save Design**

File → Save Design

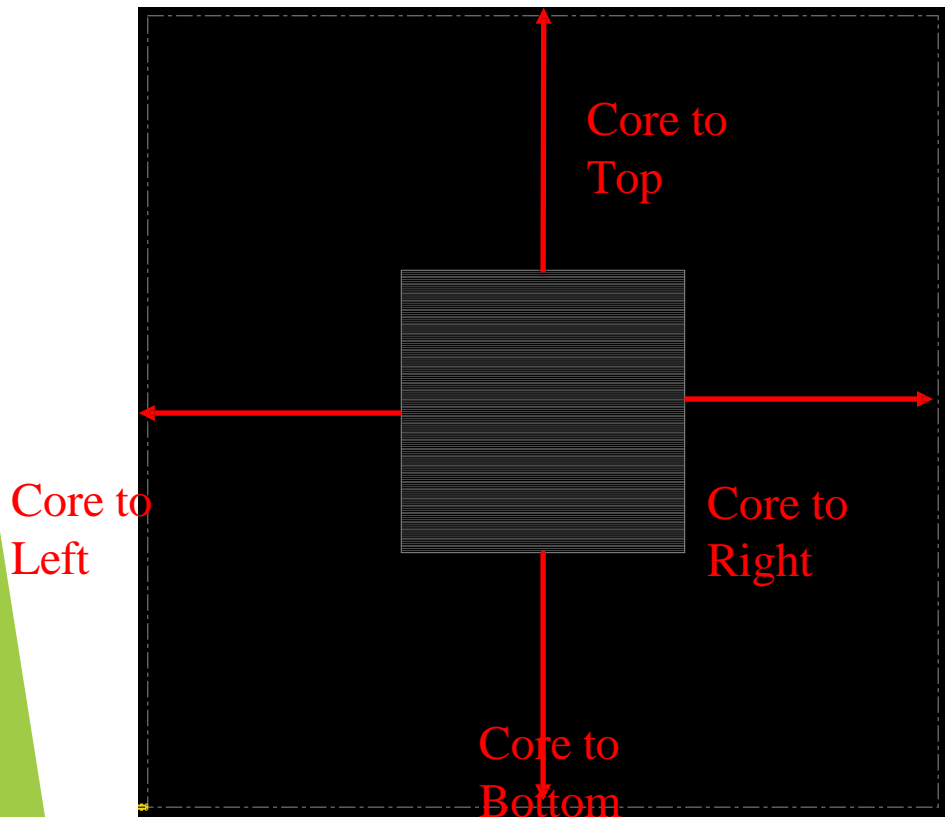
► **Restore Design**

File → Restore Design



Initial Step(3/3)

- ▶ 3. Decide the overview of your design.
- ▶ Floorplan → Specify Floorplan... → ...
- ▶ Ratio (H/W):1 ; Core Utilization:0.7 ; (建議0.6-0.8)
- ▶ Core to Left:80; Core to Right:80; Core to Top:80; Core to Bottom:80;



Shape of your design(設定為1晶片就是正方形)

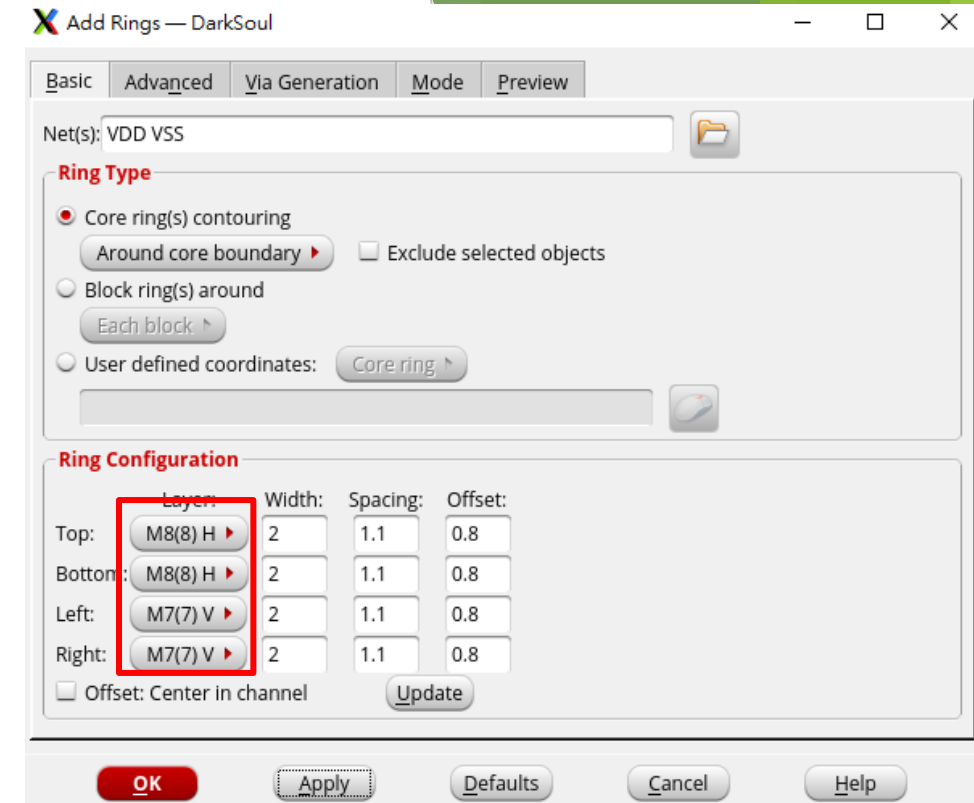
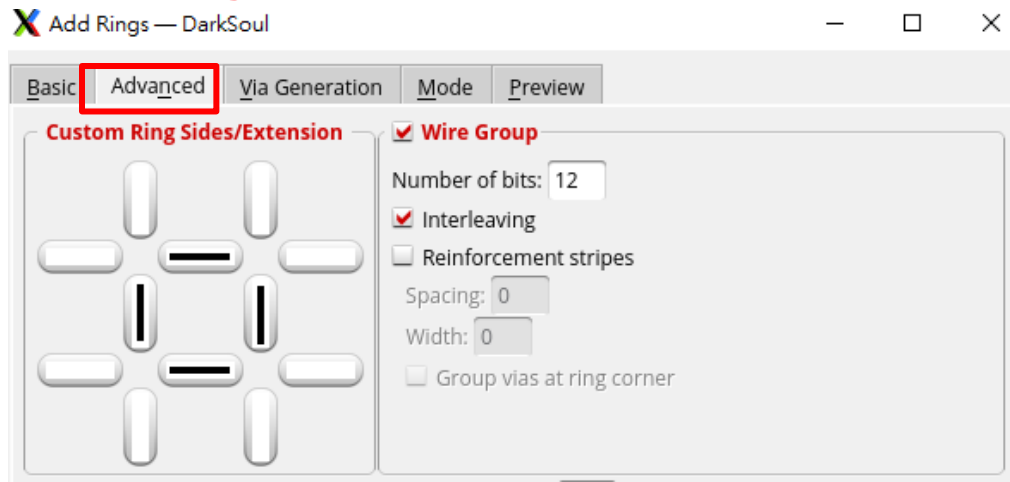
Density of your design



註：如果有PAD的話要調整適當的距離，如果Core跟PAD 太接近， 在後面接Power Ring及Route後，有可能會DRC錯誤

PowerPlan(1/9)

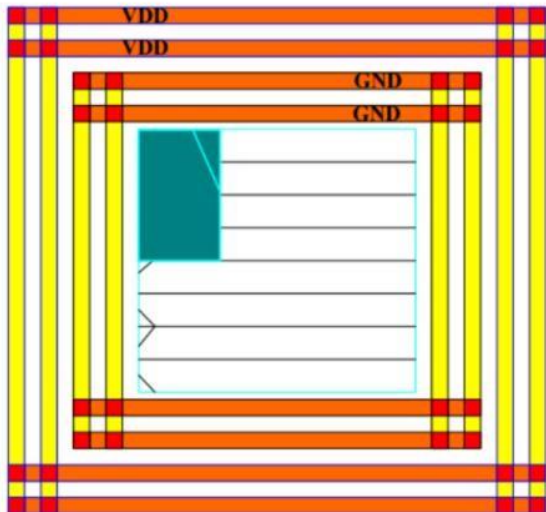
- ▶ 1. **innovus** > source lab_script/pns.tcl
- ▶ 2. Create Power Ring ---- To give Power to chip
- ▶ 3. Power → Power Planning → Add Rings → Basic
 - Nets: VDD VSS
 - In Ring Configuration, change Top & Bottom to METAL8, Left & Right to METAL7;
 - Set Width to 2 and Spacing to 1.1
- ▶ 4. Change to Advanced
 - Select Wire Group, set Numbers of Bits to **12**
 - Select **Interleaving**



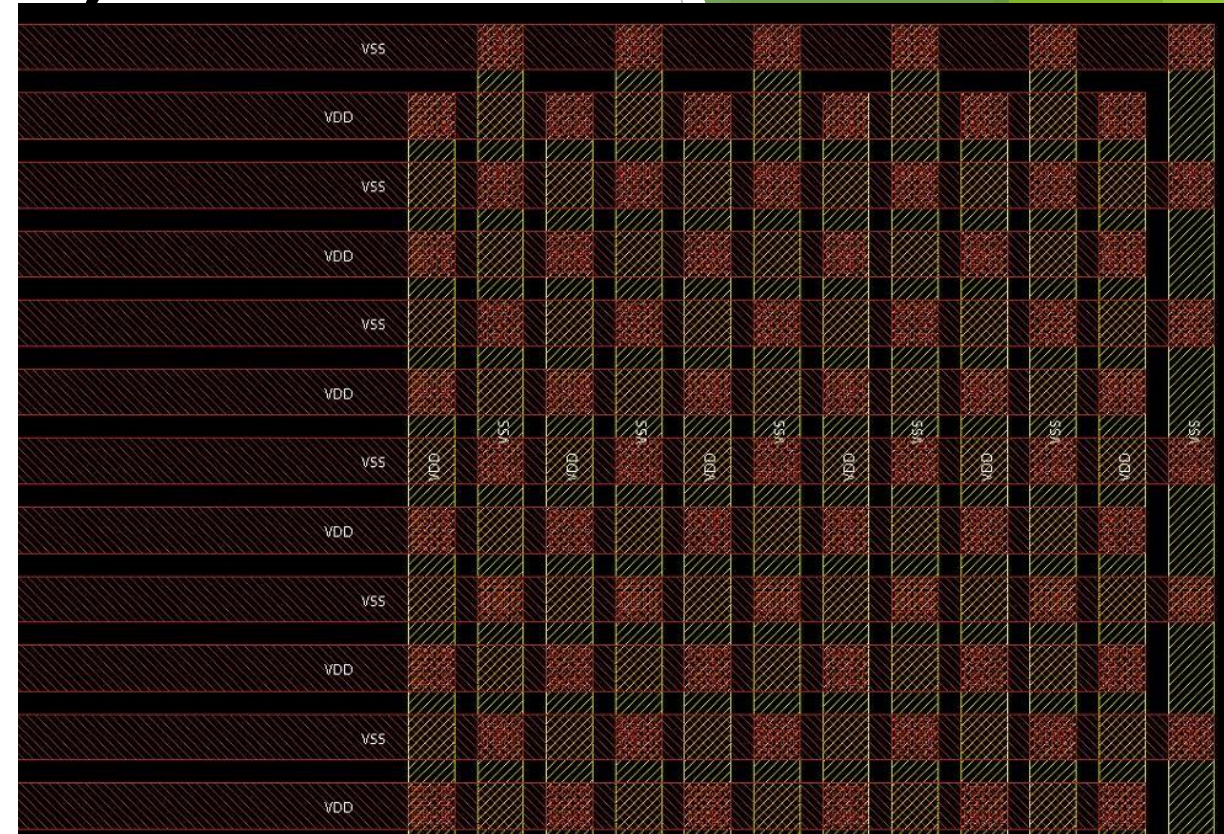
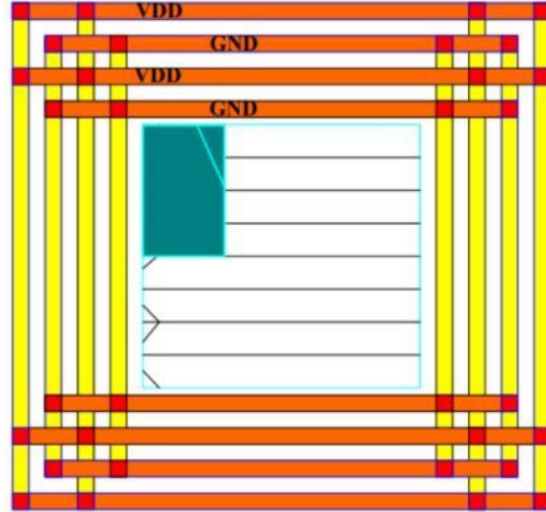
PowerPlan(2/9)

► What's Interleaving?

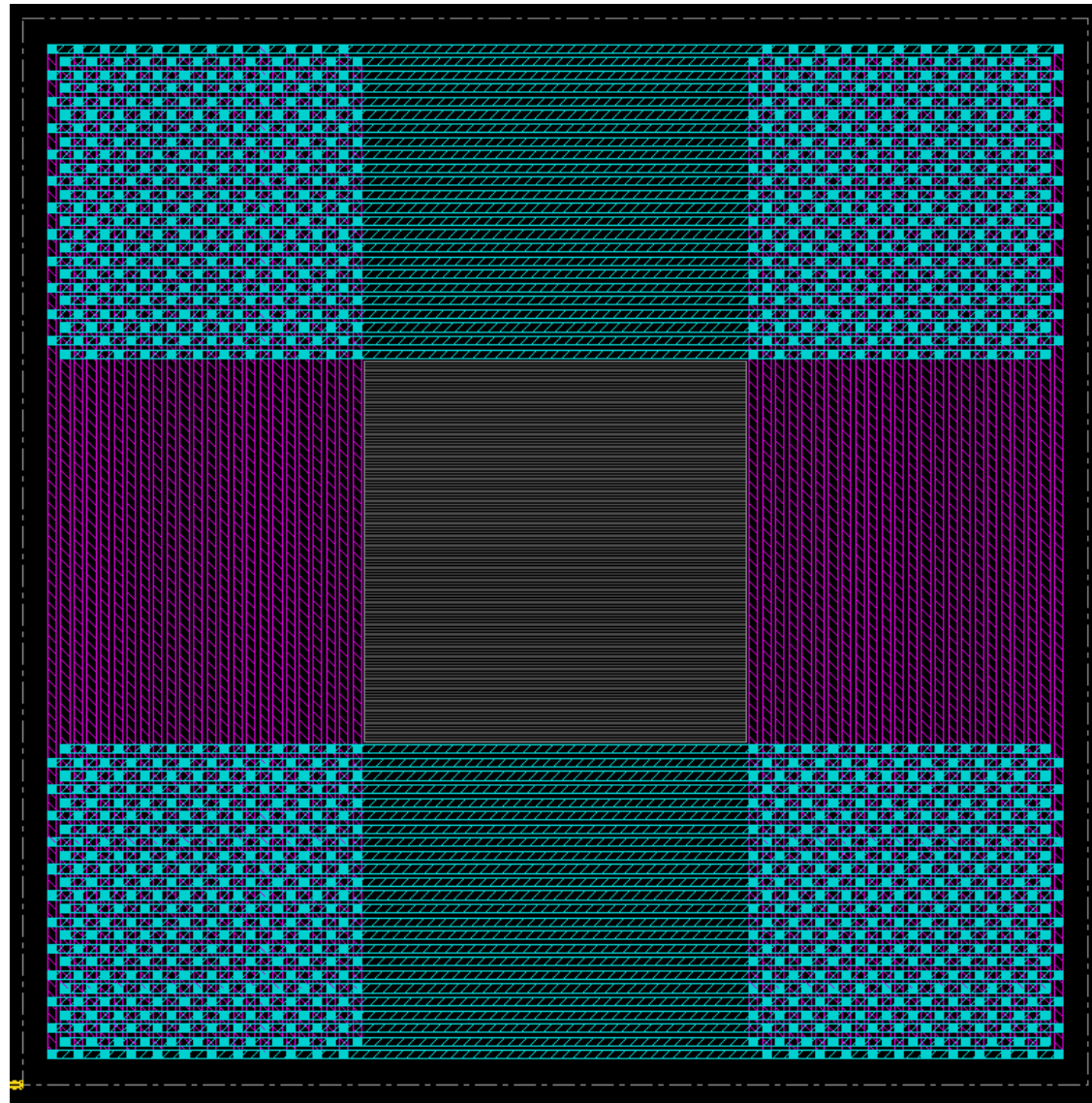
- ✓ Use wire group
- no interleaving
- ✓ number of bits = 2



- ✓ Use wire group
- ✓ interleaving
- ✓ number of bits = 2

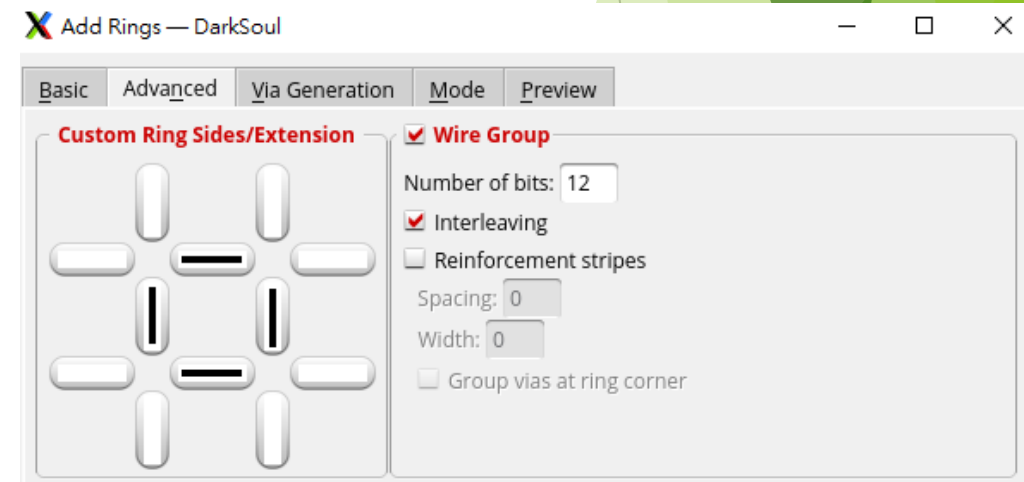
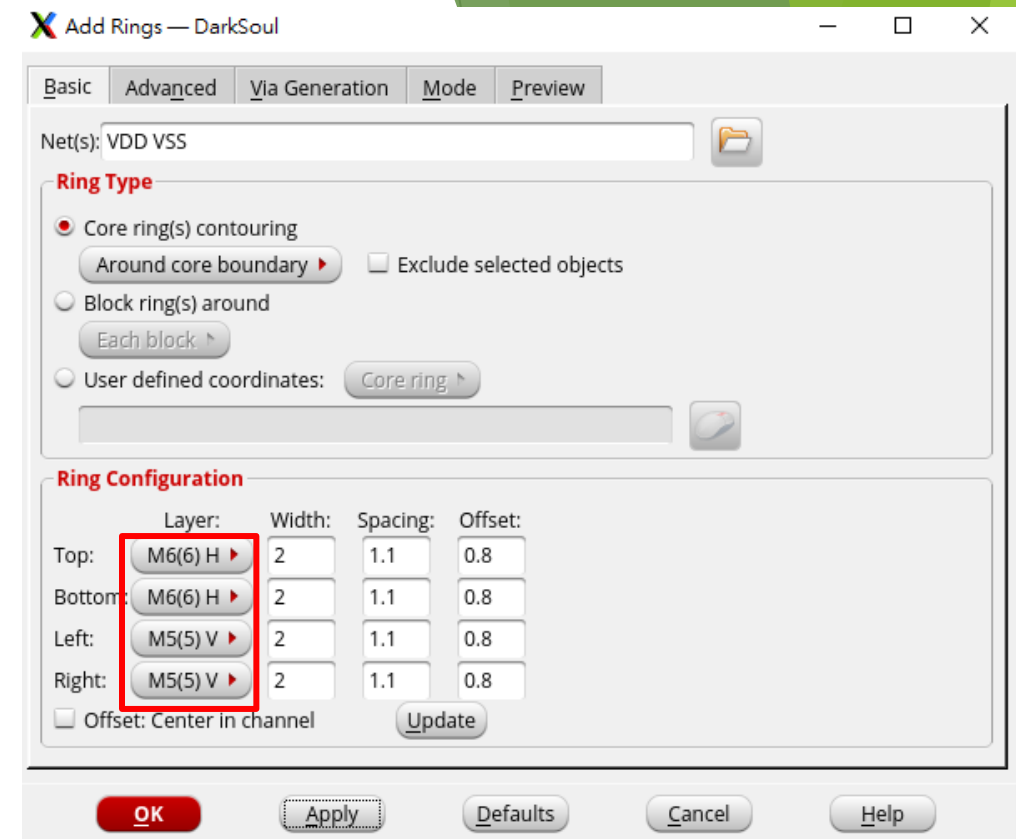


PowerPlan(3/9)

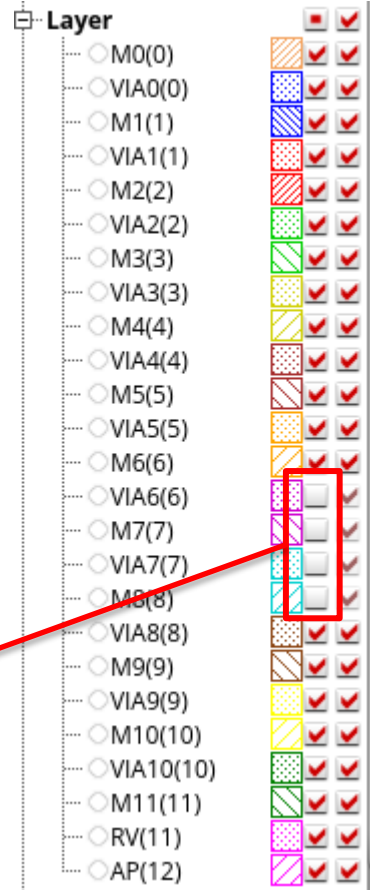


PowerPlan(4/9)

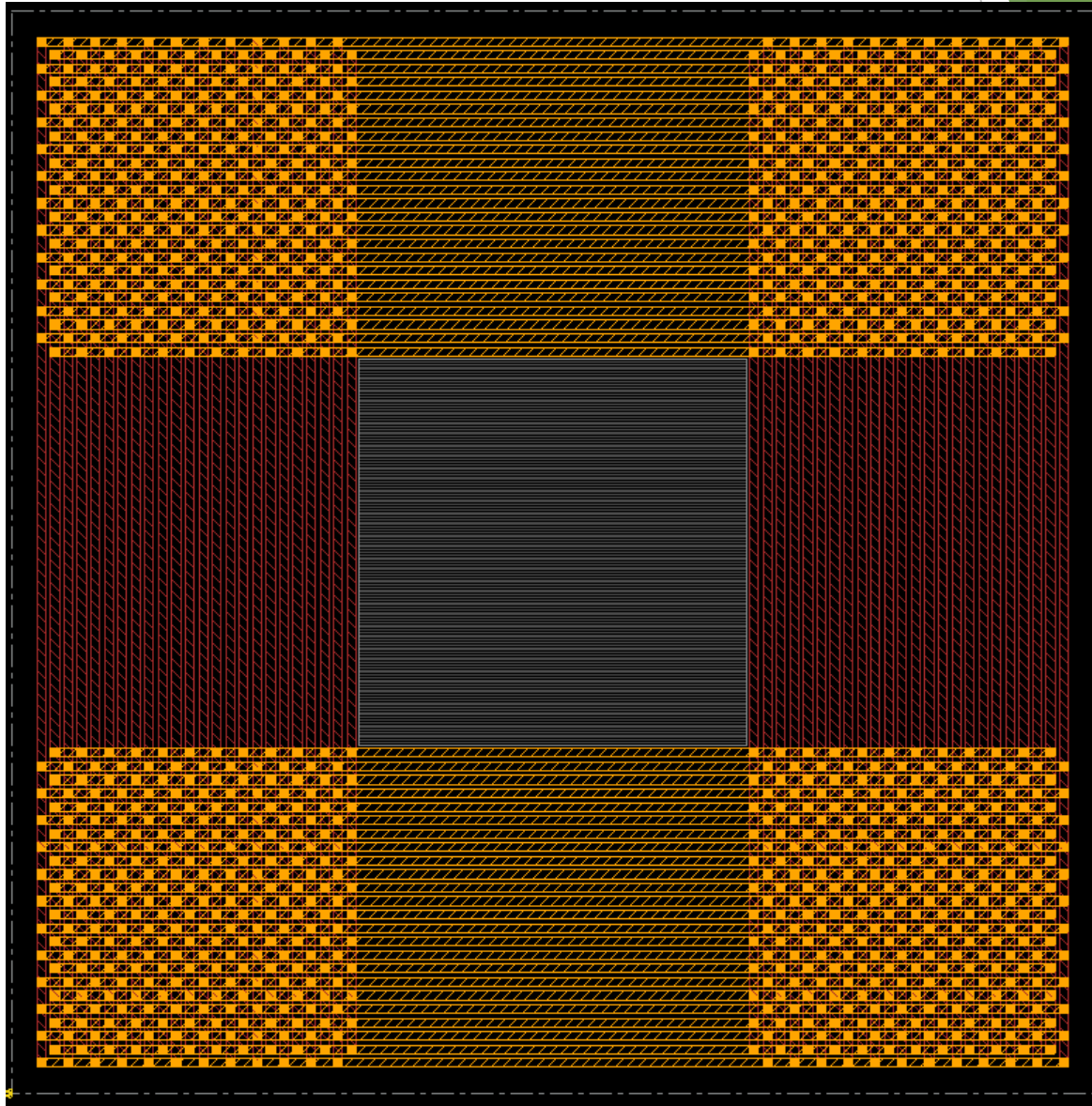
- ▶ 5. Create Power Ring ---- To give Power to chip
- ▶ 6. Power → Power Planning → Add Rings → Basic
 - Nets: VDD VSS
 - In Ring Configuration, change Top & Bottom to **METAL6**, Left & Right to **METAL5**;
 - Set Width to 2 and Spacing to 1.1
- ▶ 7. Change to Advanced
 - Select Wire Group, set Numbers of Bits to 12
 - Select Interleaving
- ▶ 8. **innovus** > edit_trim_routes -nets {VDD VSS} -layer {M8 M7 M6 M5}
會把Power Ring 多餘的部分切掉



PowerPlan(5/9)



把這4層勾選掉才能看到M5, M6



PowerPlan(6/9)

► 8. Add **stripe**

- The deeper part of your design may not have enough power from power ring, so you need to add stripe to boost the voltage.
- Vertical stripe is recommended.

► 9. Power → Power Planning → Add Stripe → Basic

- Nets: VDD VSS
- Layers: **METAL9** and select **Vertical**;
- Set Width to 1.8 and Spacing to 1.8
- In Set Pattern, select Set-to-set distance and input **7.2**
- Select Relative from core or selected area
- Start: **1.8**

► 接續下一頁

The screenshot shows the 'Add Stripes' dialog box in the DarkSoul software. The 'Basic' tab is selected, and the configuration is as follows:

- Set Configuration:**
 - Net(s): VDD VSS
 - Layer: M9(9)
 - Directions: ☒ Vertical ☐ Horizontal
 - Width: 1.8
 - Spacing: 1.8
 - Update button
- Set Pattern:**
 - ☒ Set-to-set distance: 7.2
 - ☐ Number of sets: 1
 - ☐ Bumps: Over
 - ☐ Over P/G pins: Pin layer: Top pin layer, Pin Width:
 - ☐ Master name:
 - ☐ Selected blocks
 - ☒ All blocks
 - ☐ Over Physical Pins: Pin layer: Top pin layer, Pin Width:
- Stripe Boundary:**
 - ☒ Core ring
 - ☐ Pad ring: Outer
 - ☐ All domains
 - ☐ Design boundary
 - ☒ Create pins
 - ☐ Each selected block/domain/fence
 - ☐ Specify rectangular area: X1: , Y1: , X2: , Y2:
 - ☐ Specify rectilinear area:
- First/Last Stripe:**
 - Start from: ☒ Left ☐ Right ☐ Top ☐ Bottom
 - ☒ Relative from core or selected area: Start: 1.8, Stop:
 - ☐ Absolute: Start: , Stop:

Buttons at the bottom: OK, Apply, Defaults, Cancel, Help.

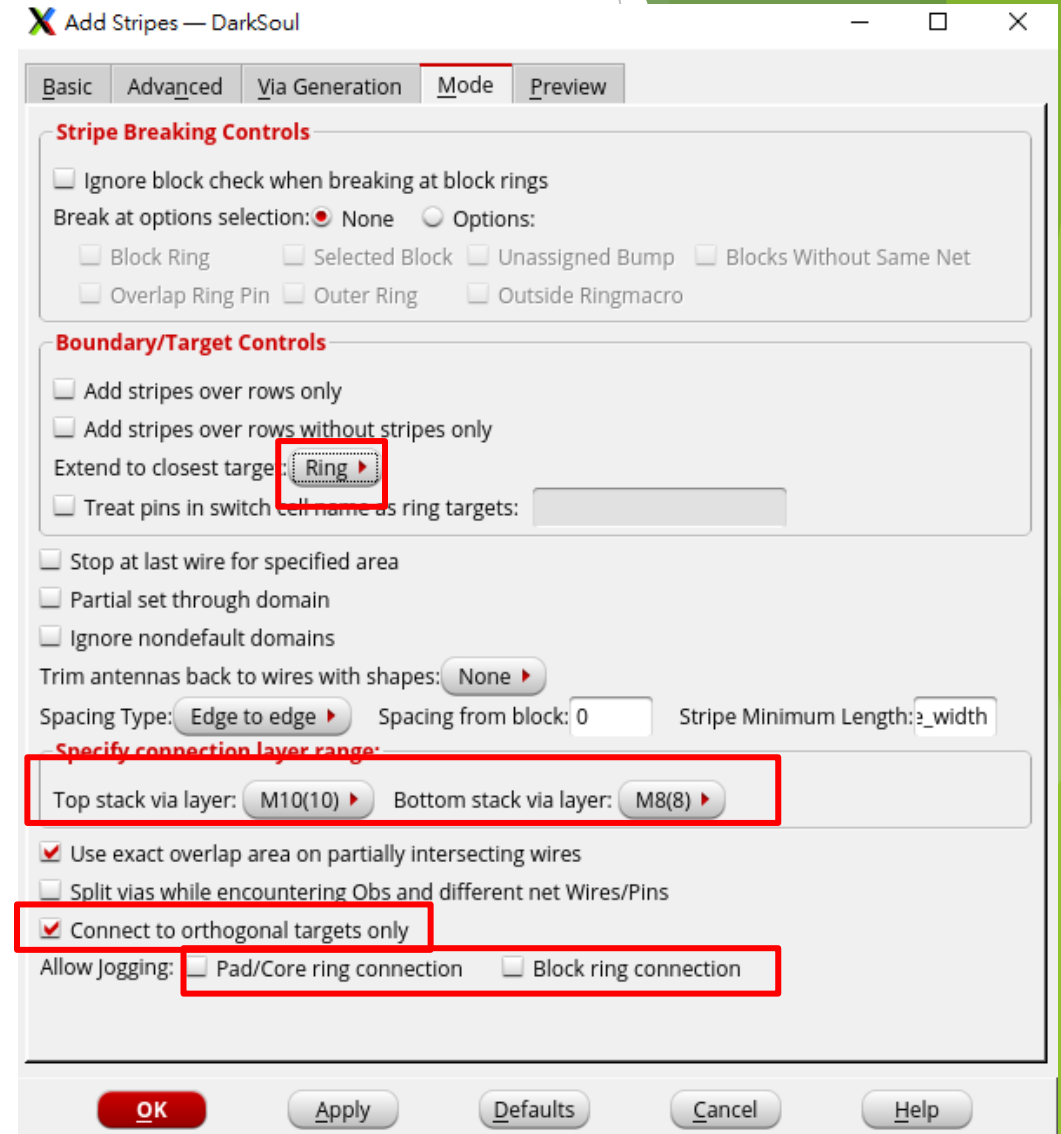
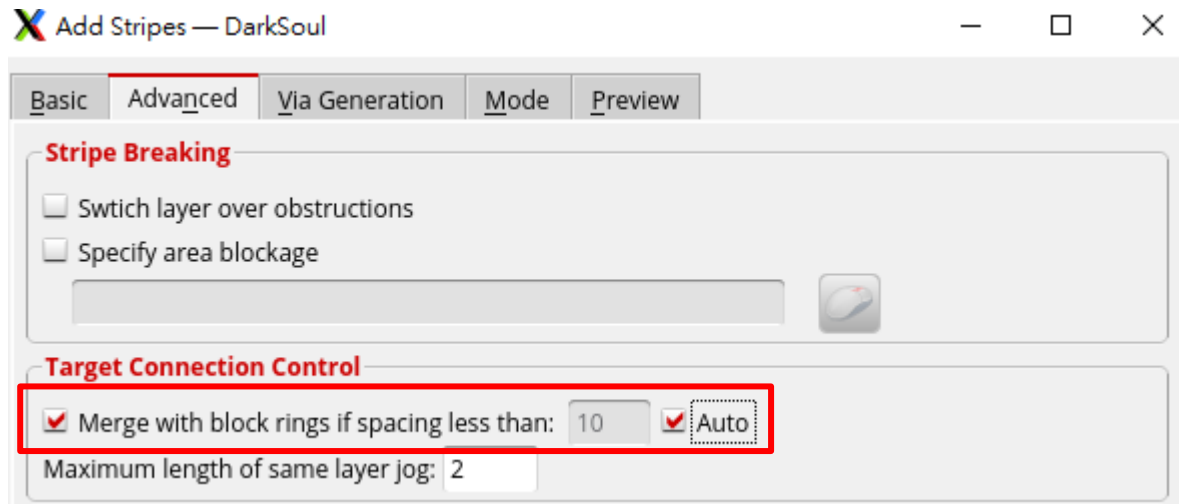
PowerPlan(7/9)

► 10. Change to **Advanced** Page

- Choose **Merge** with block ring if spacing less than : 10
- Choose **Auto**

► 11. Change to **Mode**

- Extend to closest target: **Ring**
- Top Stack via layer: **METAL10** Bottom Stack via layer: **METAL8**
- Choose **Connect to orthogonal targets only**
- **un-choose** Pad/Core ring connection & Block ring connection



PowerPlan(8/9)

Basic

Mode

Advanced

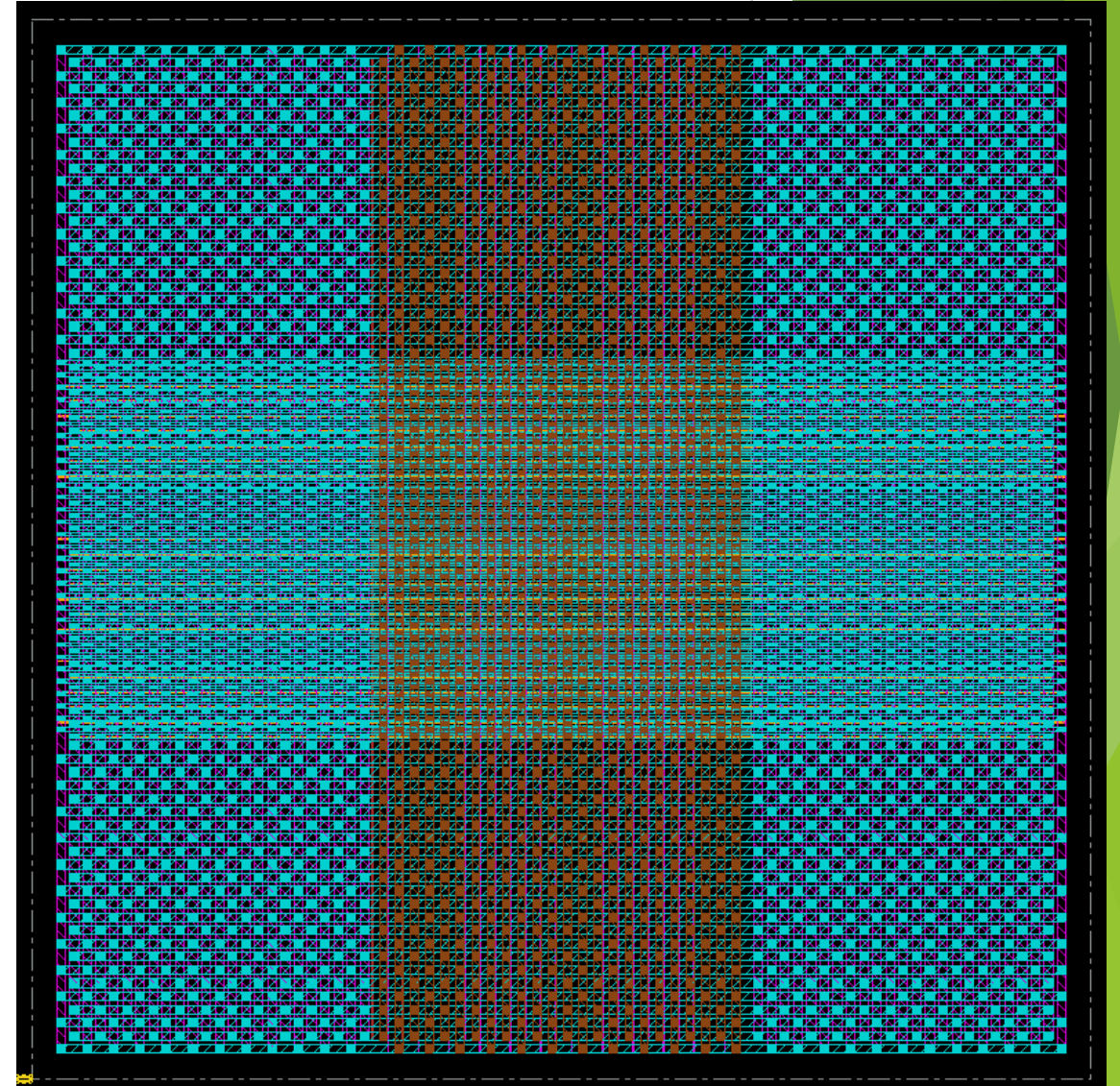
Net	Metal layer	dir	width	space	set to set	start	Top stack via	Bottom stack via	Snap to Routing grid
VDD VSS	M9	V	1.8	1.8	7.2	1.8	M10	M8	
VDD	M8	H	0.864	0	2.88	0	M9	M7	Half_Grid
VSS	M8	H	0.864	0	2.88	1.44	M9	M7	Half_Grid
VDD	M7	V	0.24	0	7.2	7.2	M8	M6	Grid
VSS	M7	V	0.24	0	7.2	3.6	M8	M6	Grid
VDD	M6	H	0.24	0	7.2	0	M7	M5	Grid
VSS	M6	H	0.24	0	7.2	3.6	M7	M5	Grid
VDD	M5	V	0.24	0	7.2	0	M6	M4	Grid
VSS	M5	V	0.24	0	7.2	3.6	M6	M4	Grid

重複6~7的步驟做9次，並更改上面的內容

PowerPlan(9/9)

12. Check → CheckDRC... → OK

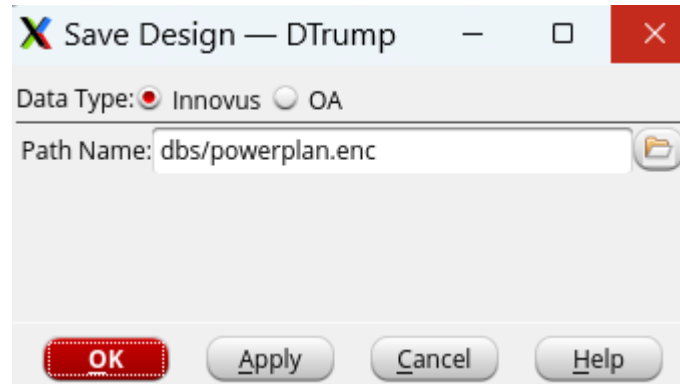
```
VERIFY DRC ..... Sub-Area: {194.432 222.208 222.208 248.736} 80 of 81  
VERIFY DRC ..... Sub-Area : 80 complete 0 Viols.  
VERIFY DRC ..... Sub-Area: {222.208 222.208 248.940 248.736} 81 of 81  
VERIFY DRC ..... Sub-Area : 81 complete 0 Viols.  
Verification Complete : 0 Viols.
```



PowerPlan

► Save Design

File → Save Design
dbs/powerplan.enc



Power Route(1/8)

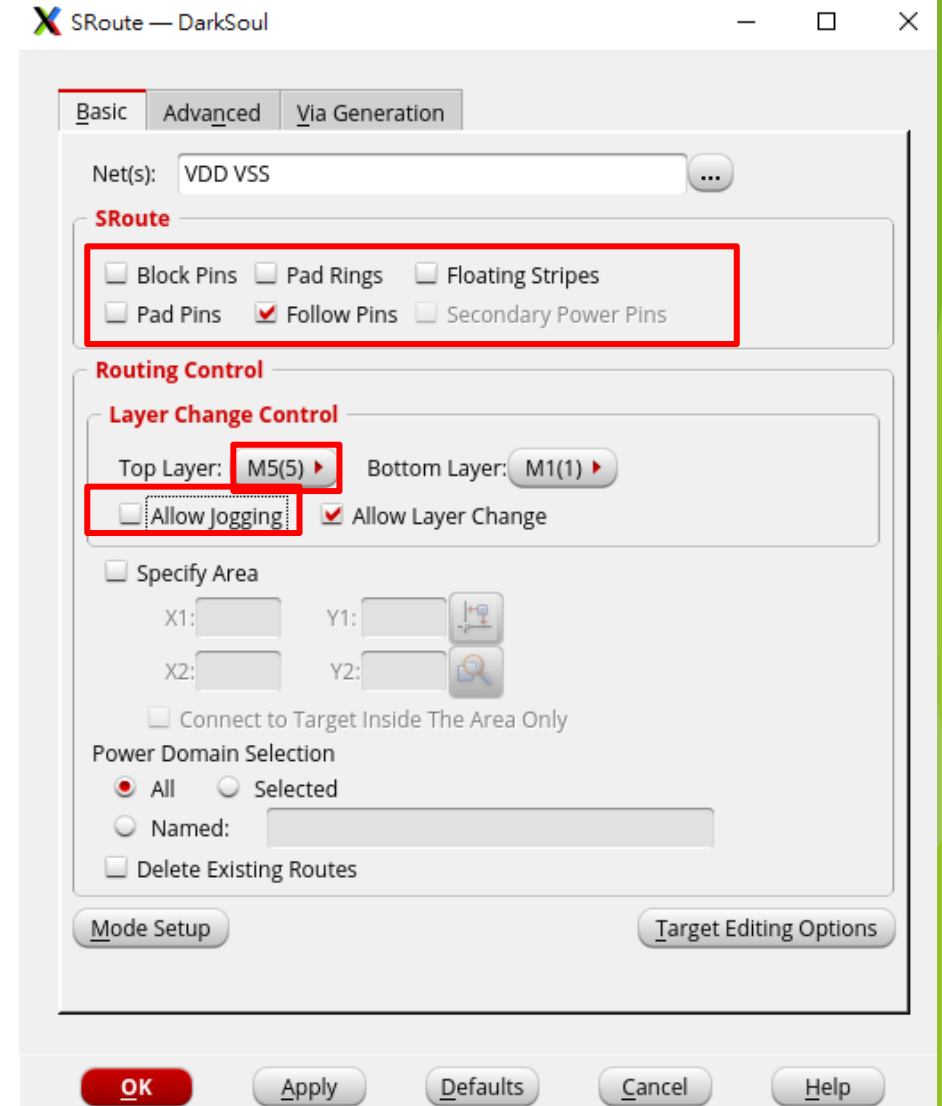
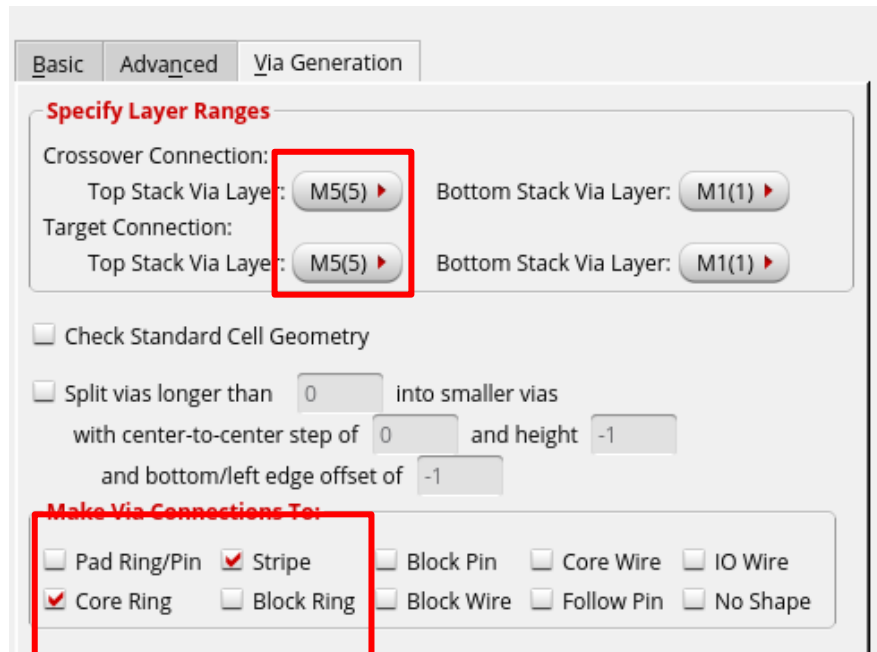
► What's power route? ---- Connect all cell to power ring

► 1. Route → Special Route → Basic

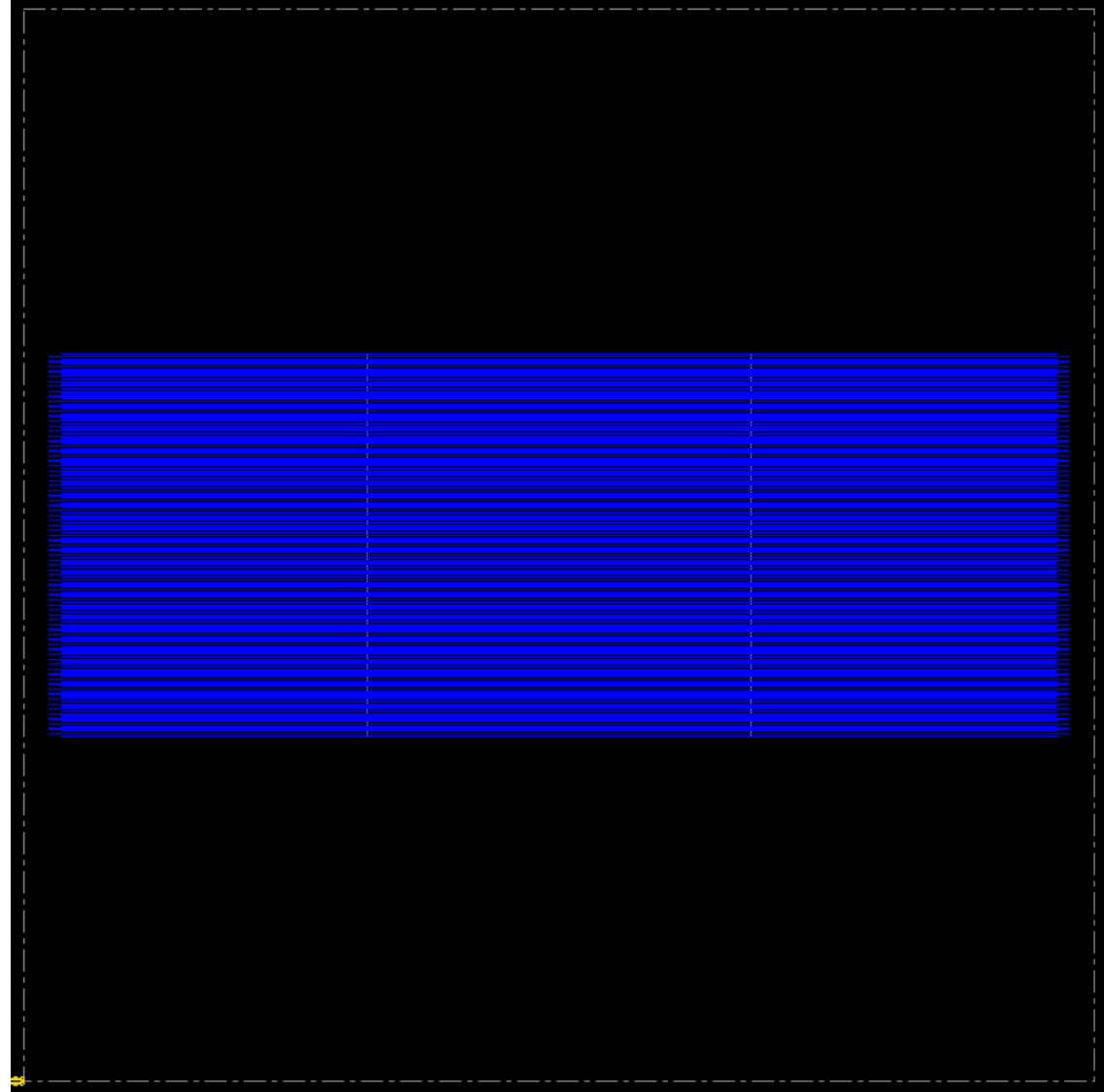
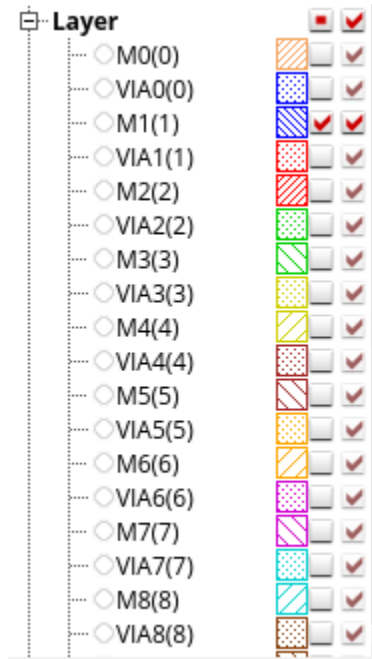
- Net(s): VDD VSS
- In SRoute, only select **Follow pins**
- **un-choose** Allow **jogging**

► 2. Change to Via Generation

- In Make Via Connection To, select Core **Ring & Stripe**
- Crossover Connection: Top Stack Via Layer: **METAL5**



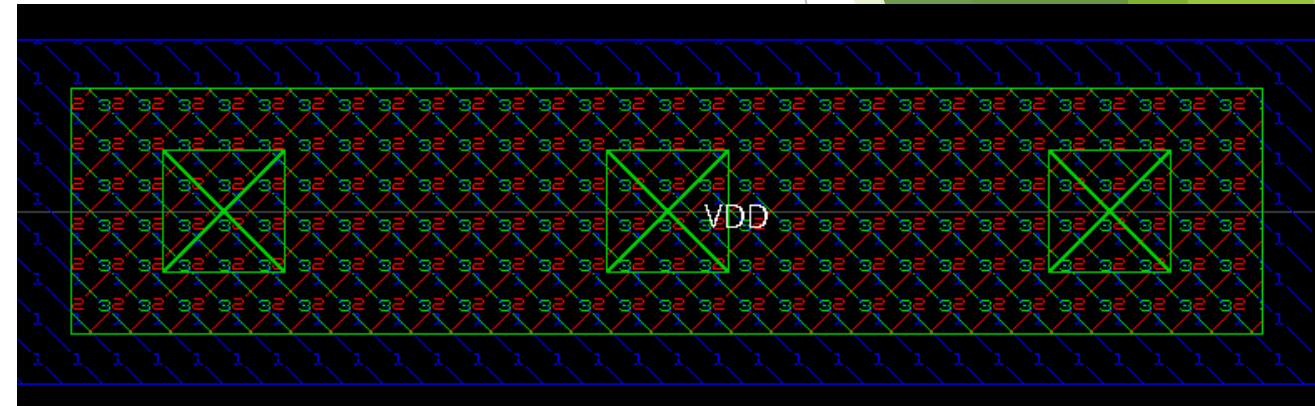
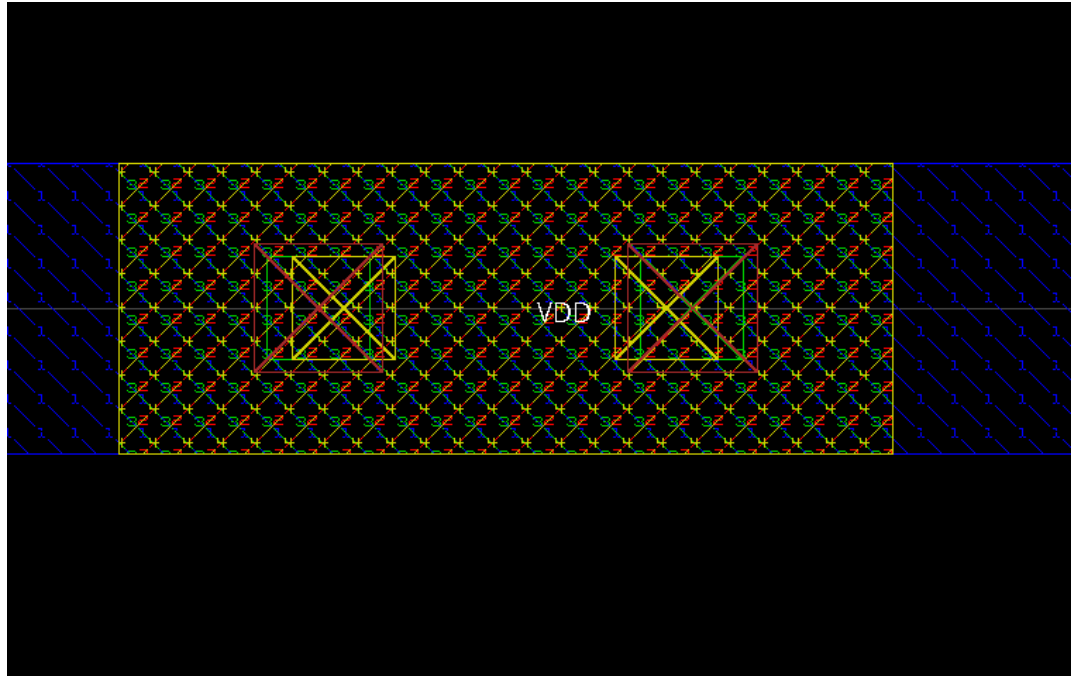
Power Route(2/8)



Power Route(3/8)

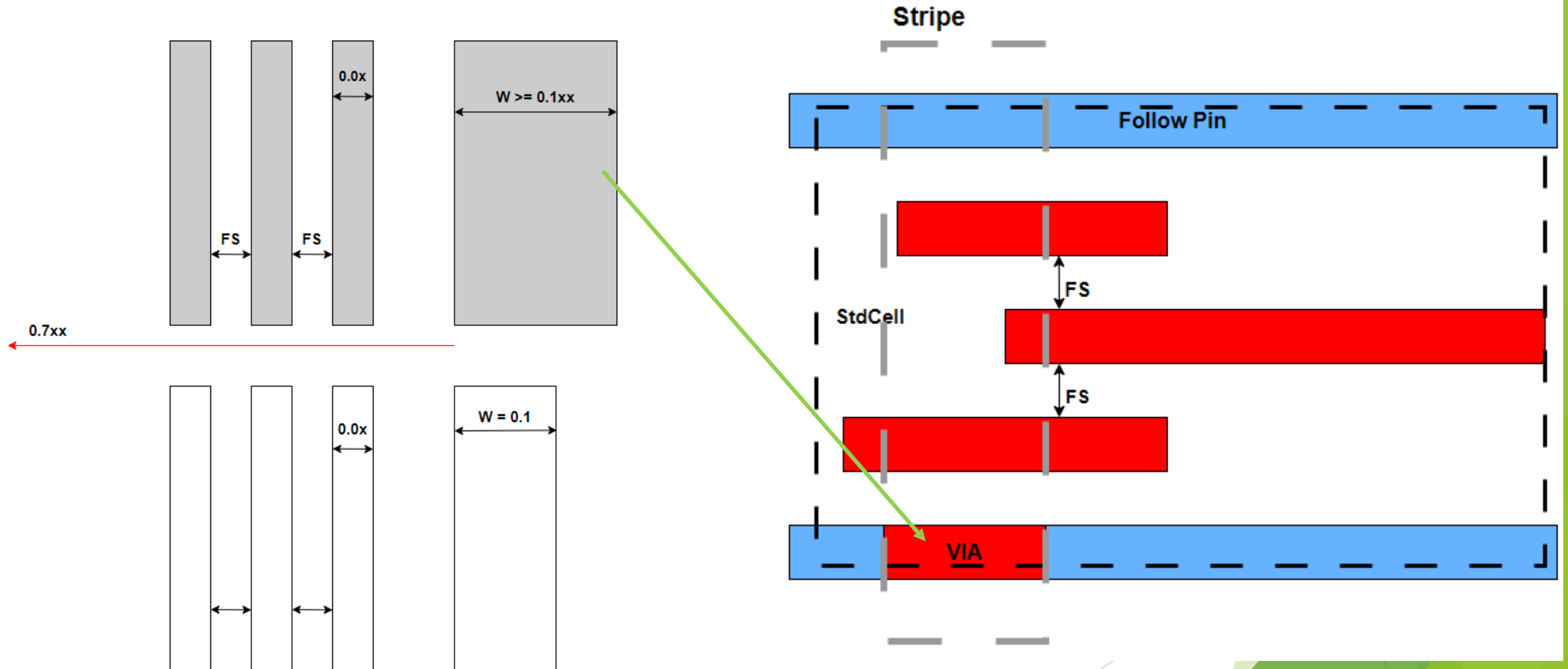
3. **innovus** > source lab_script/shrink_via.tcl

調整Follow pin連接到的via size



Power Route(4/8)

► Mxa Forbidden Spacing



Power Route(5/8)

► 4. Power → Power Planning → Add Stripe → Basic

- Nets: **VSS**
- Layers: **METAL2** and select Horizontal;
- Set Width to **0.064** and Spacing to **0**
- In Set Pattern, select Set-to-set distance and input **1.152**
- Select Relative from core or selected area
- Start: **0.544**

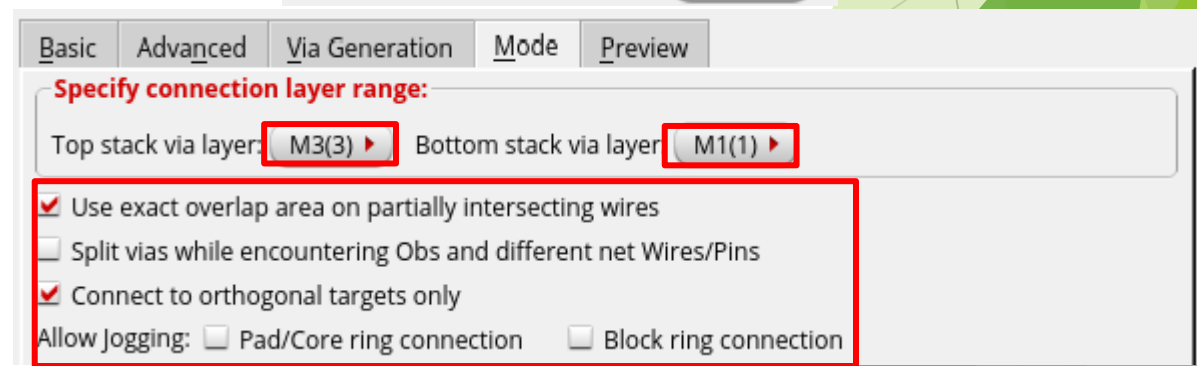
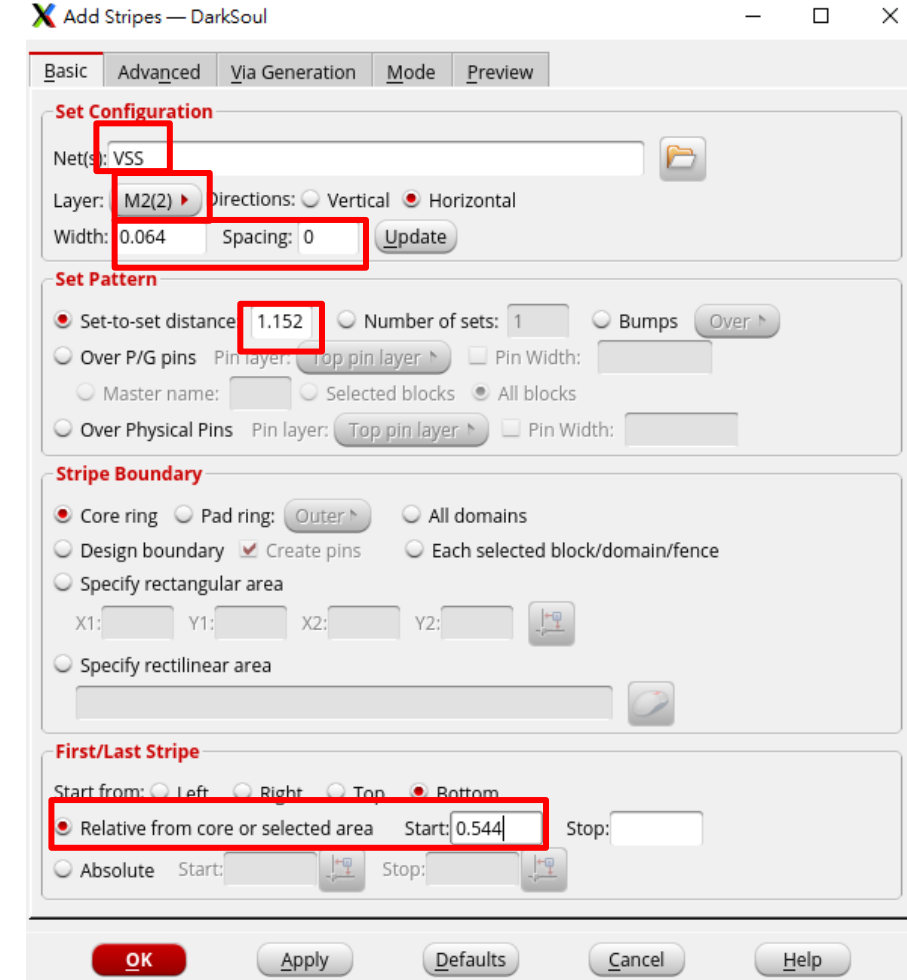
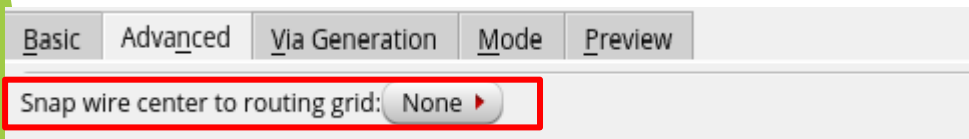
► 5. Change to Advanced Page

- Snap wire center to routing grid : select “None”

► 6. Change to Mode

- Extend to closest target: **Ring**
- Top Stack via layer: METAL3 Bottom Stack via layer: METAL1
- un-choose Pad/Core ring connection & Block ring connection

► 7. Click Apply



Power Route(6/8)

► 8. Change VSS to VDD

- Nets: VDD
- Start: -0.032

► 9. Click Apply

Add Stripes — DarkSoul

Basic Advanced Via Generation Mode Preview

Set Configuration

Net(s): VDD

Layer: M2(2) Directions: ☐ Vertical ☒ Horizontal

Width: 0.064 Spacing: 0 Update

Set Pattern

☒ Set-to-set distance: 1.152 ☐ Number of sets: 1 ☐ Bumps Over

☐ Over P/G pins Pin layer: Top pin layer ☐ Pin Width:

☐ Master name: ☐ Selected blocks ☒ All blocks

☐ Over Physical Pins Pin layer: Top pin layer ☐ Pin Width:

Stripe Boundary

☒ Core ring ☐ Pad ring: Outer ☐ All domains

☐ Design boundary ☒ Create pins ☐ Each selected block/domain/fence

☐ Specify rectangular area

X1: Y1: X2: Y2:

☐ Specify rectilinear area

First/Last Stripe

Start from: ☐ Left ☐ Right ☐ Top ☒ Bottom

☒ Relative from core or selected area Start: -0.032 Stop:

☐ Absolute Start: Stop:

OK Apply Defaults Cancel Help

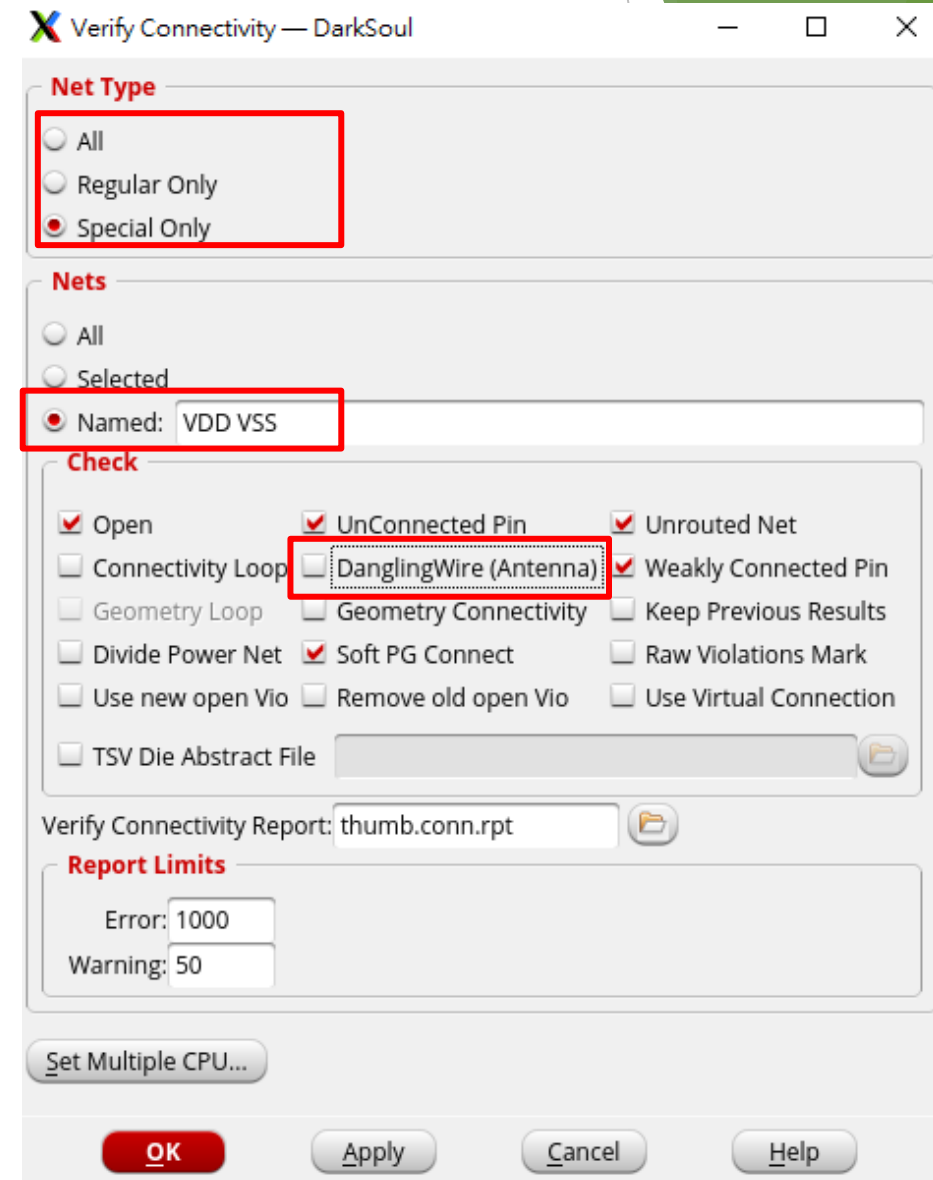
Power Route(7/8)

► 10. Check → Check Connectivity...

- Net Type: Special Only
- Nets: VDD VSS
- In Check, un-choose DanglingWire (Antenna)

There should not have any violation and X on the screen.

```
***** End: VERIFY CONNECTIVITY *****  
Verification Complete : 0 Viols. 0 Wrngs.  
(CPU Time: 0:00:00.1 MEM: 0.000M)
```

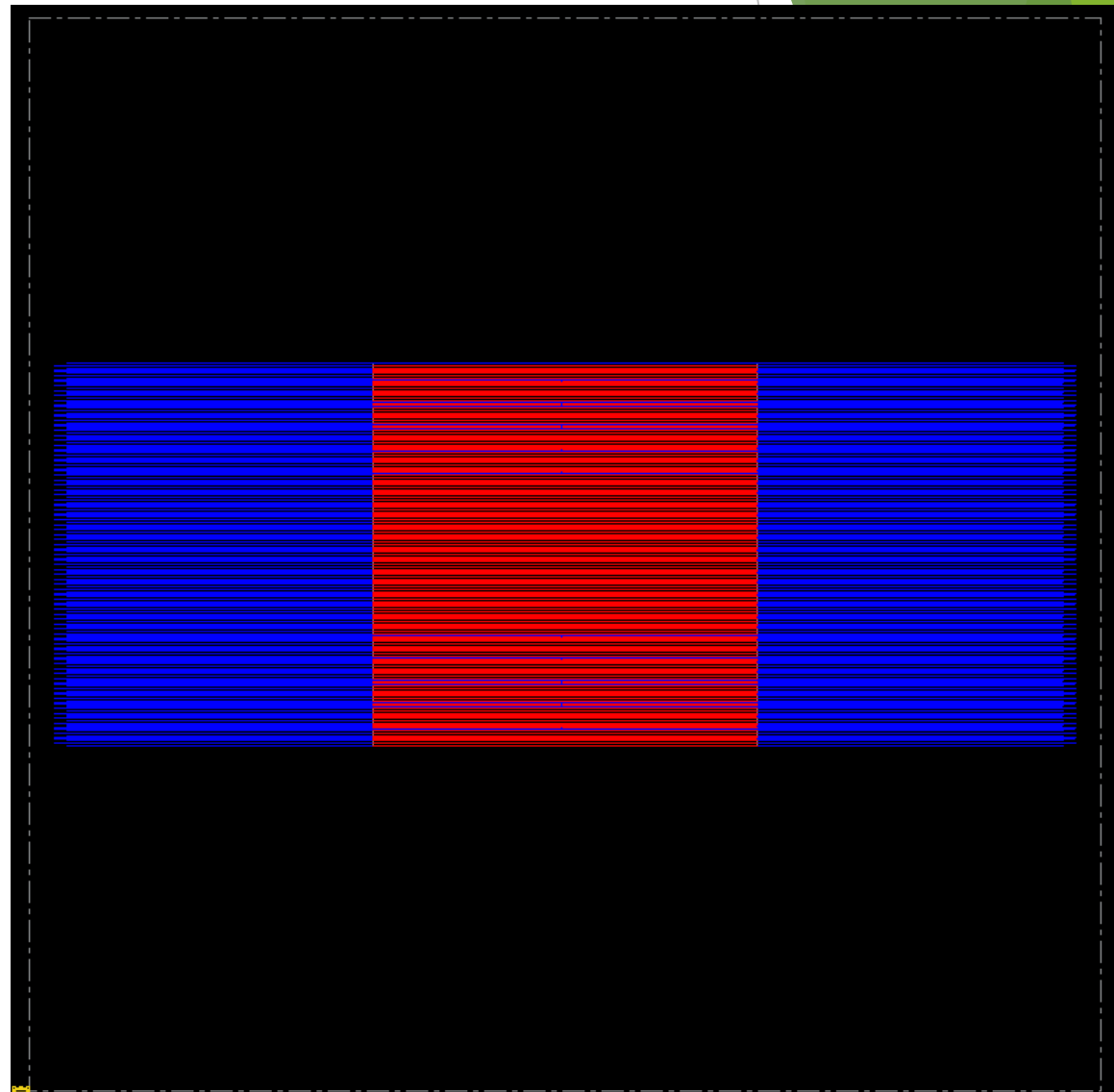


Power Route(8/8)

► 12. Check → CheckDRC... → OK

```
VERIFY DRC ..... Sub-Area : 80 complete 0 Viols.  
VERIFY DRC ..... Sub-Area: {222.208 222.208 248.940 248.736} 81 of 81  
VERIFY DRC ..... Sub-Area : 81 complete 0 Viols.  
Verification Complete : 0 Viols.
```

Layer			
○ M0(0)			<input checked="" type="checkbox"/>
○ VIA0(0)			<input checked="" type="checkbox"/>
○ M1(1)			<input checked="" type="checkbox"/>
○ VIA1(1)			<input checked="" type="checkbox"/>
○ M2(2)			<input checked="" type="checkbox"/>
○ VIA2(2)			<input checked="" type="checkbox"/>
○ M3(3)			<input checked="" type="checkbox"/>
○ VIA3(3)			<input checked="" type="checkbox"/>
○ M4(4)			<input checked="" type="checkbox"/>
● VIA4(4)			<input checked="" type="checkbox"/>
○ M5(5)			<input checked="" type="checkbox"/>
○ VIA5(5)			<input checked="" type="checkbox"/>
○ M6(6)			<input checked="" type="checkbox"/>
○ VIA6(6)			<input checked="" type="checkbox"/>
○ M7(7)			<input checked="" type="checkbox"/>
○ VIA7(7)			<input checked="" type="checkbox"/>
○ M8(8)			<input checked="" type="checkbox"/>
○ VIA8(8)			<input checked="" type="checkbox"/>
○ M9(9)			<input checked="" type="checkbox"/>
○ VIA9(9)			<input checked="" type="checkbox"/>
○ M10(10)			<input checked="" type="checkbox"/>
○ VIA10(10)			<input checked="" type="checkbox"/>
○ M11(11)			<input checked="" type="checkbox"/>
○ RV(11)			<input checked="" type="checkbox"/>



Power Route

► Save Design

File → Save Design

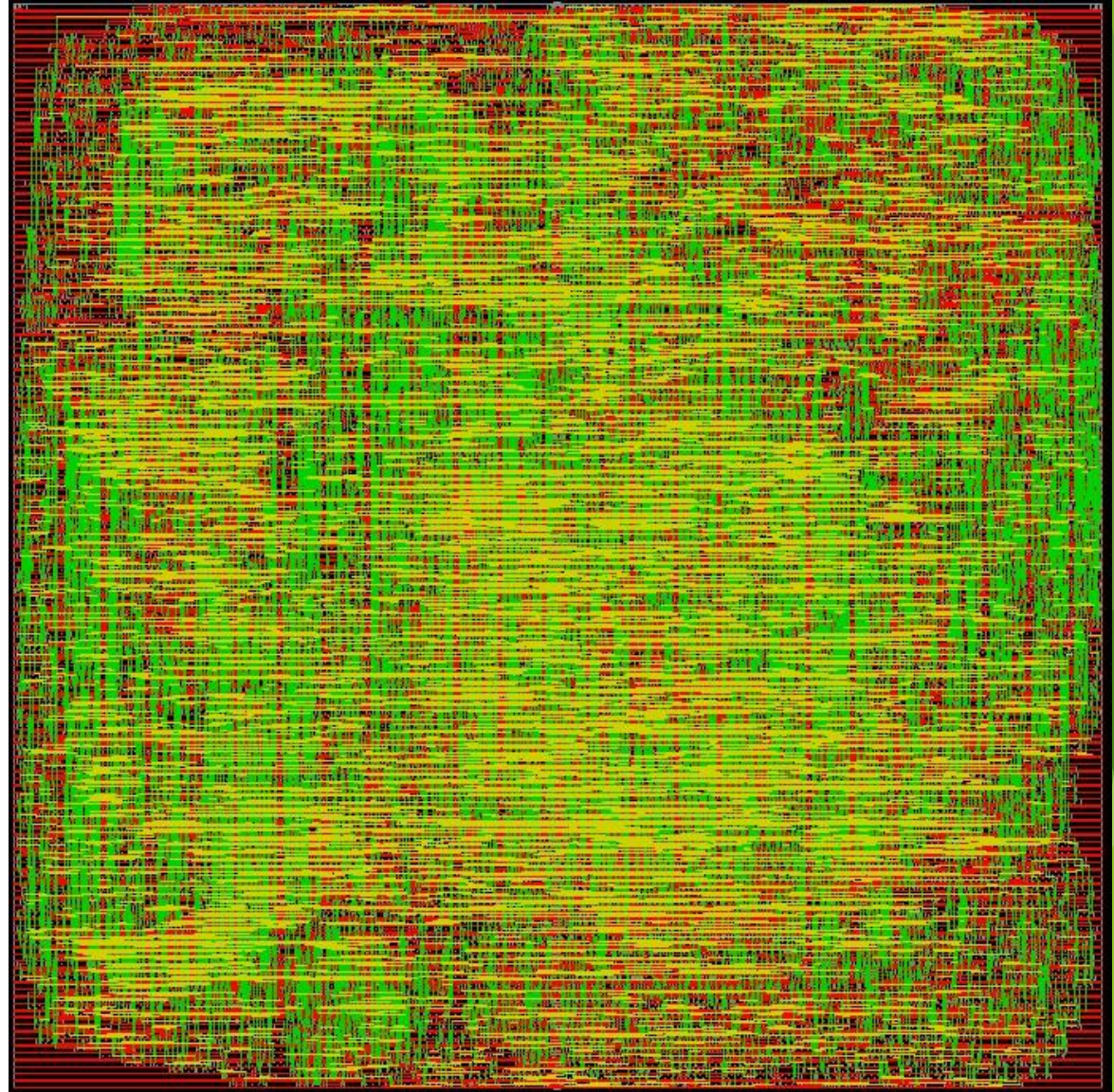
dbb/powerroute.enc



Placement(1/3)

- ▶ 1. **innovus** > source lab_script/add_well_taps.tcl
- ▶ 2. Place → Place Standard Cell → Click OK
- ▶ 3. Place → Check Placement → Click Ok

```
Begin checking placement ... (start mem=4451.4M, init mem=4451.4M)
*info: Placed = 13587          (Fixed = 78)
*info: Unplaced = 0
```



Placement(2/3)

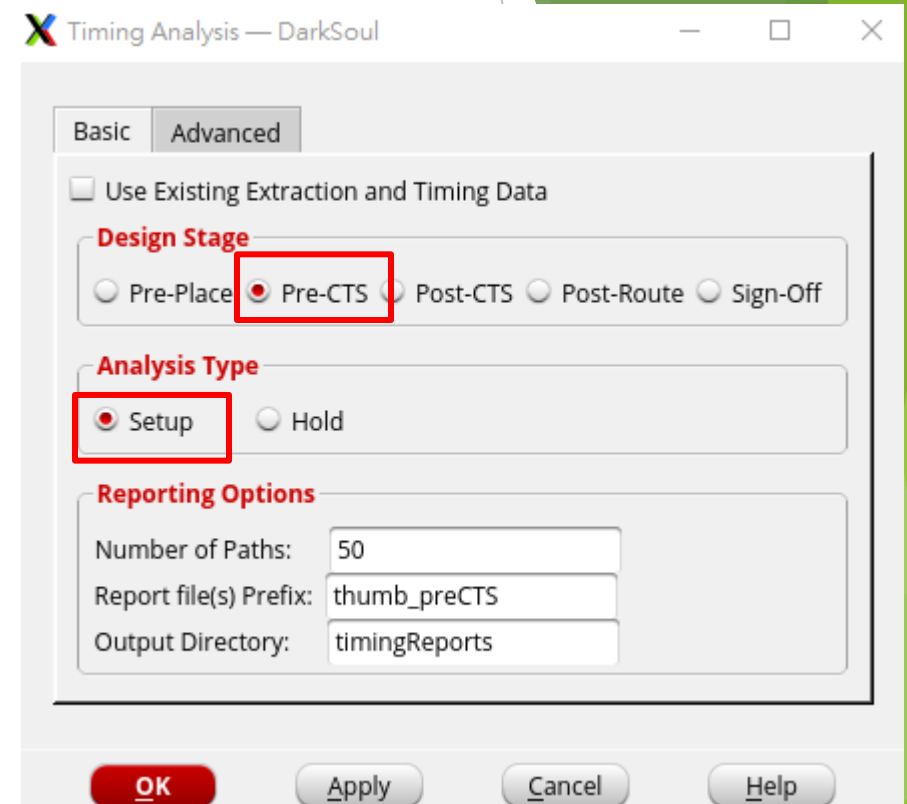
► 4. Timing → Report Timing

- Design Stage : Choose Pre-CTS

-Analysis Type : Choose Setup

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	-1.009	-1.009	0.154	0.456	N/A	0.000
TNS (ns):	164.026	164.026	0.000	0.000	N/A	0.000
Violating Paths:	339	339	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0

如果WNS有負的，照下一頁講義修



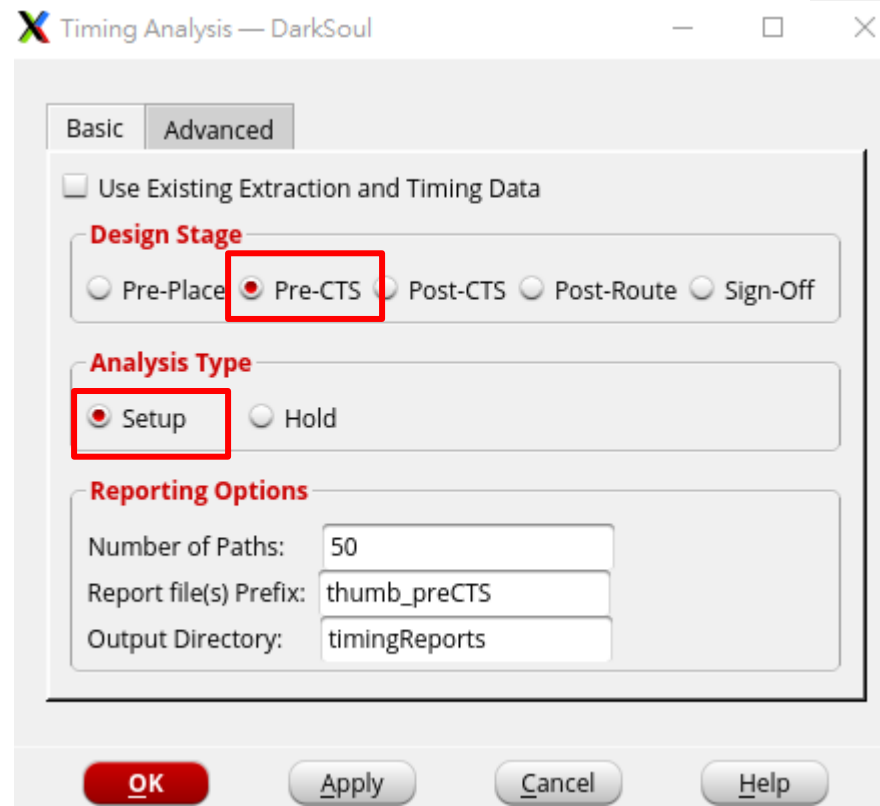
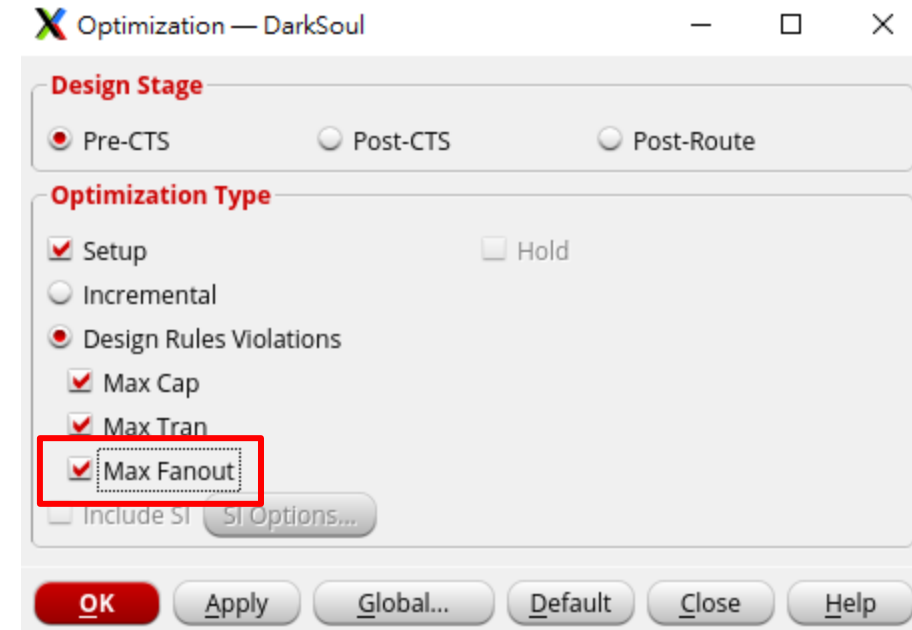
Placement(3/3)

► 5. ECO → Optimize Design

- Design Stage : Choose Pre-CTS
- Optimization Type : Choose Max Fanout

► 6. Timing → Report Timing

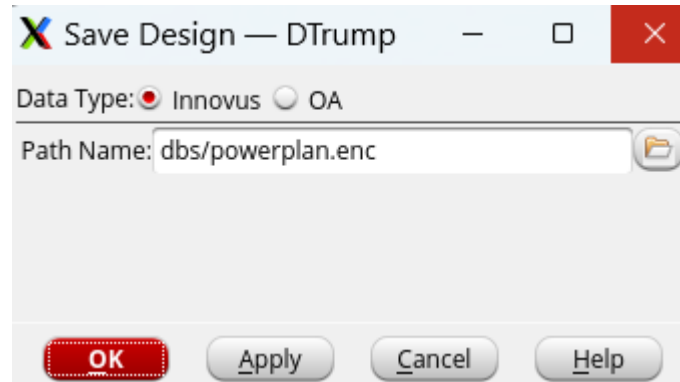
- Design Stage : Choose Pre-CTS
- Analysis Type : Choose Setup



Placement

► Save Design

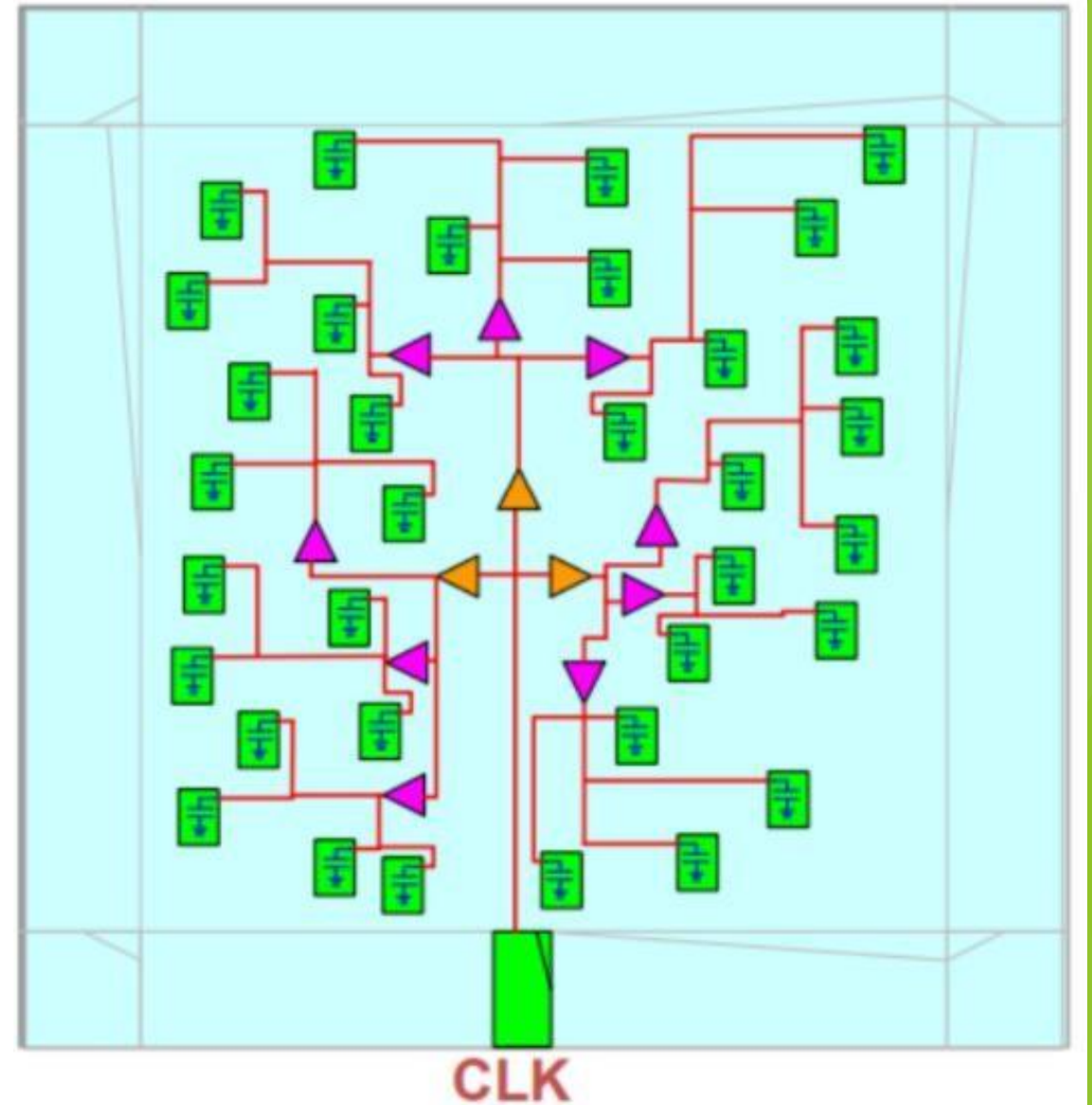
File → Save Design
dbs/powerplan.enc



CTS(1/6)

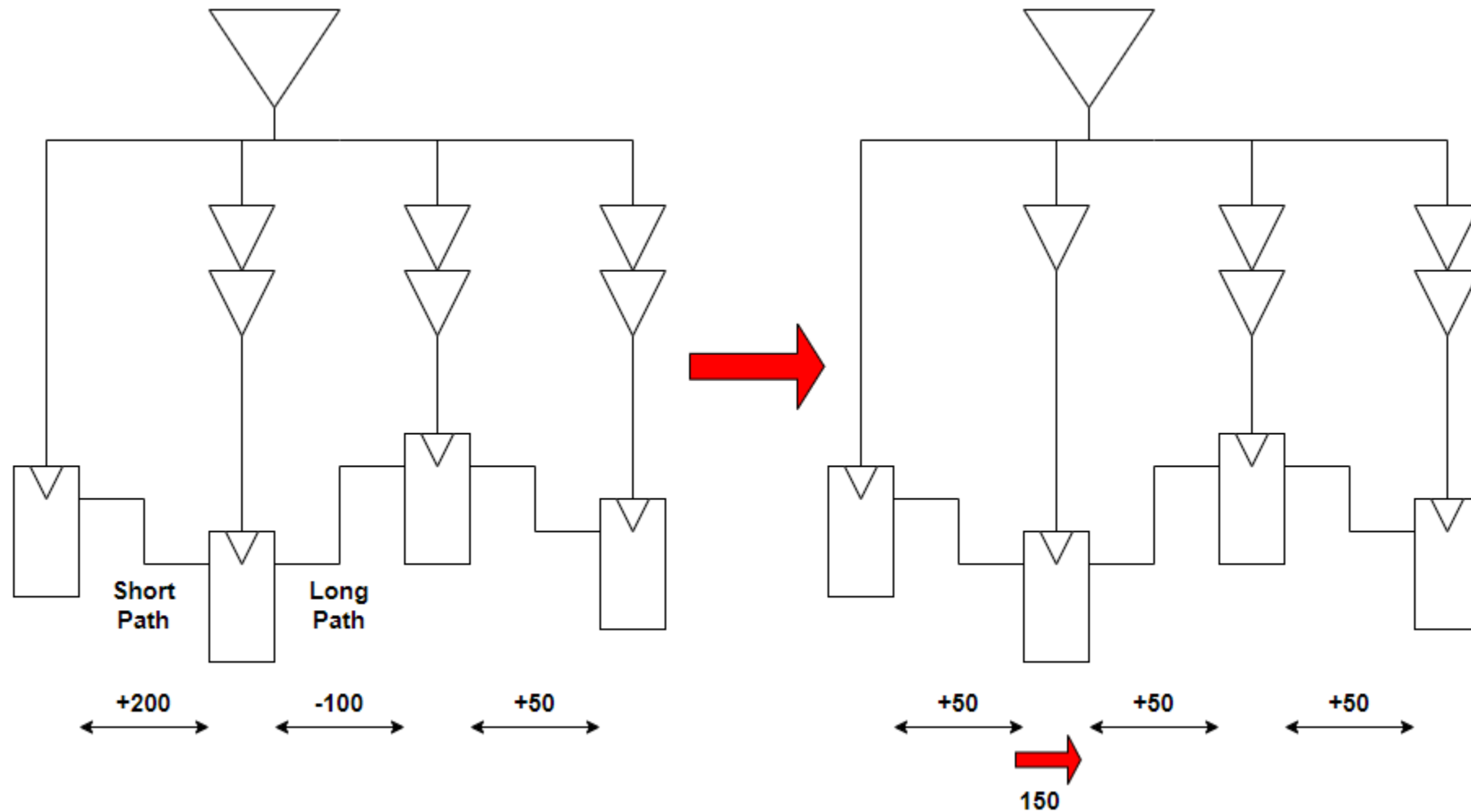
► Clock Tree Synthesis(CTS), To solve Clock problem:

- Heavy clock net loading
- Long clock insertion delay
- Clock skew
- Skew across clocks
- Clock to signal coupling effect
- Clock is power hungry



CTS(2/6)

► Clock Concurrent Optimization



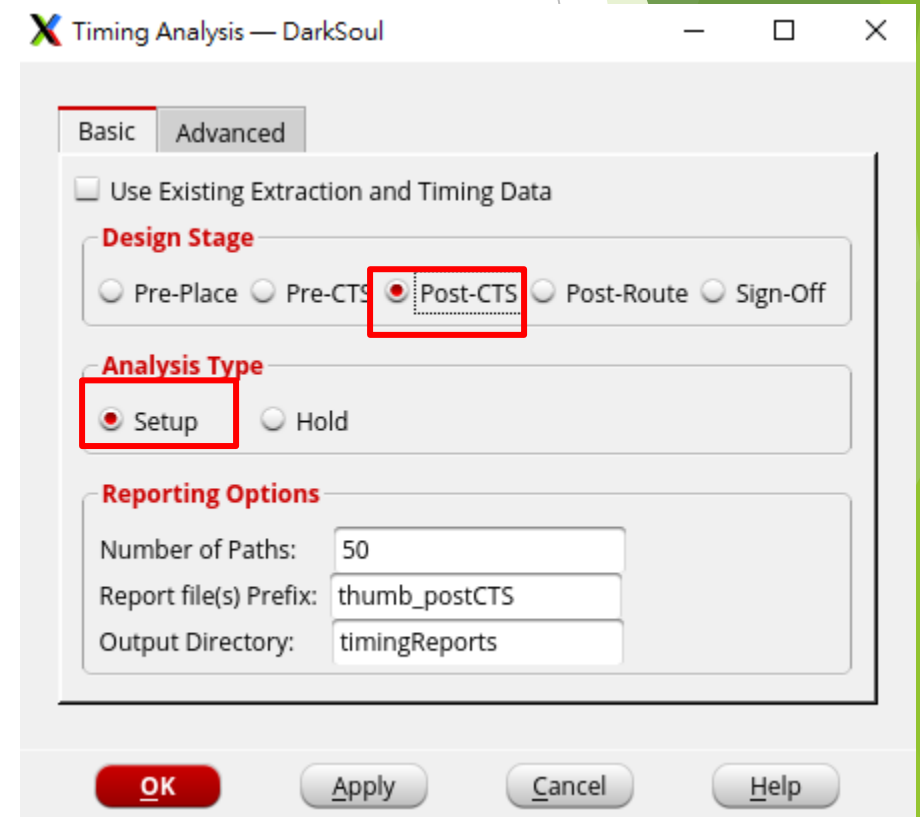
CTS(3/6)

- ▶ 1. **innovus** > set_interactive_constraint_modes [all_constraint_modes]
- ▶ 2. **innovus** > reset_clock_latency [all_clocks]
- ▶ 3. **innovus** > ccopt_design
- ▶ 4. Timing → Report Timing

- Design Stage : Choose Post-CTS

-Analysis Type : Choose Setup

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.001	0.001	0.297	0.413	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1349	734	1006	66	N/A	0



CTS(4/6)

► 5. Timing → Report Timing

- Design Stage : Choose Post-CTS

-Analysis Type : Choose hold

Timing Analysis — DarkSoul

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold

Reporting Options

Number of Paths: 50

Report file(s) Prefix: thumb_postCTS

Output Directory: timingReports

OK Apply Cancel Help

Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	-0.061	0.027	-0.061	0.041	N/A	0.000
TNS (ns):	-28.644	0.000	-28.644	0.000	N/A	0.000
Violating Paths:	724	0	724	0	N/A	0
All Paths:	1349	734	1006	66	N/A	0

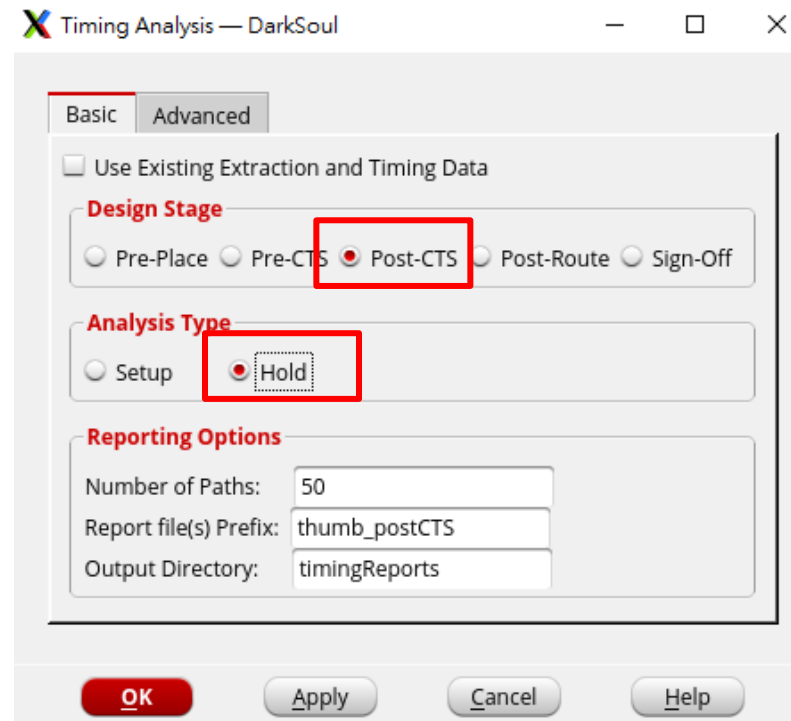
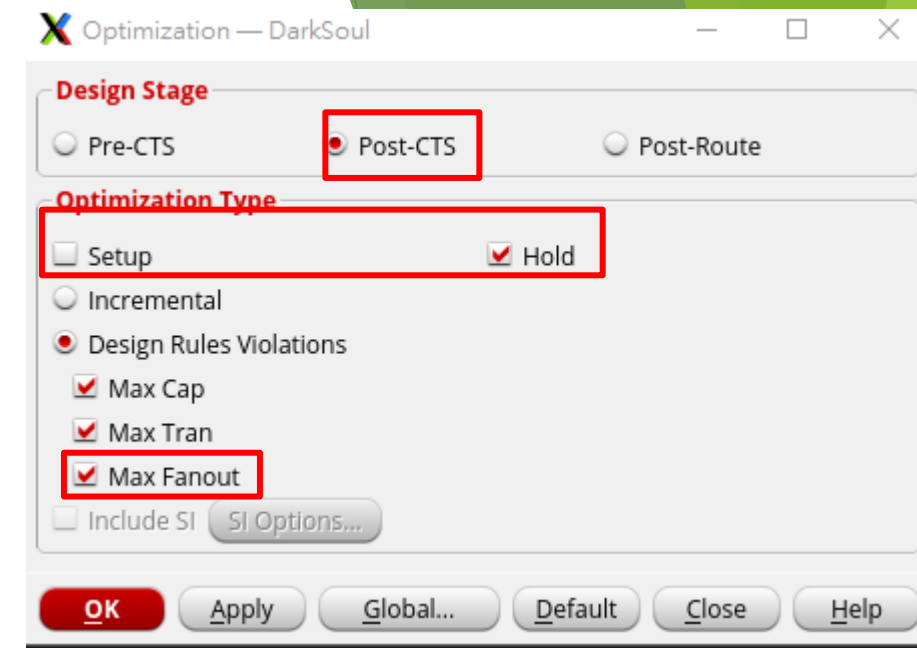
CTS(5/6)

► 6. ECO → Optimize Design

- Design Stage : Choose Post-CTS
- Optimization Type : Choose Hold
- Optimization Type : Choose Max Fanout

► 7. Timing → Report Timing

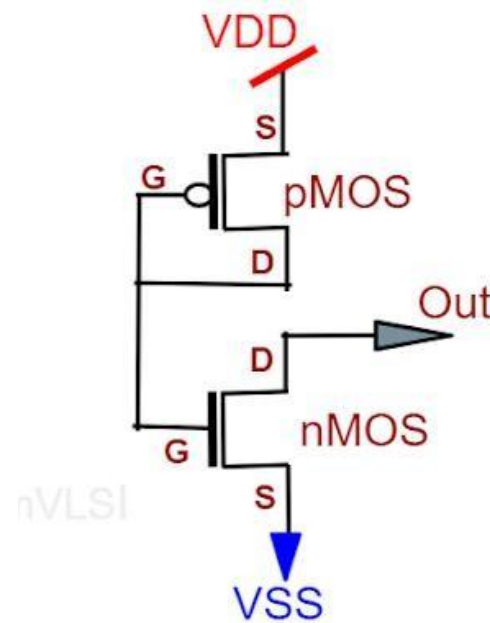
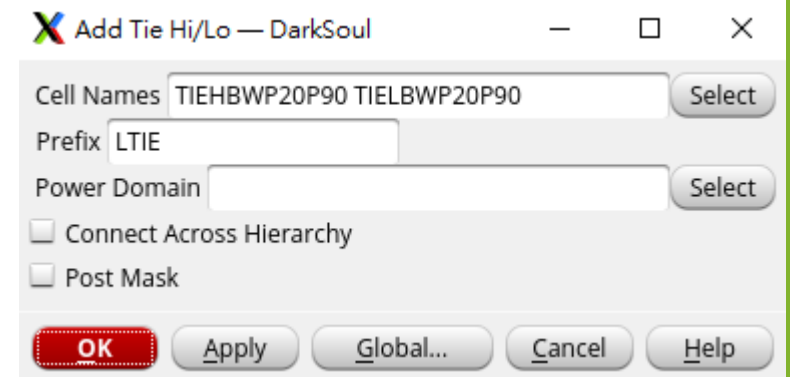
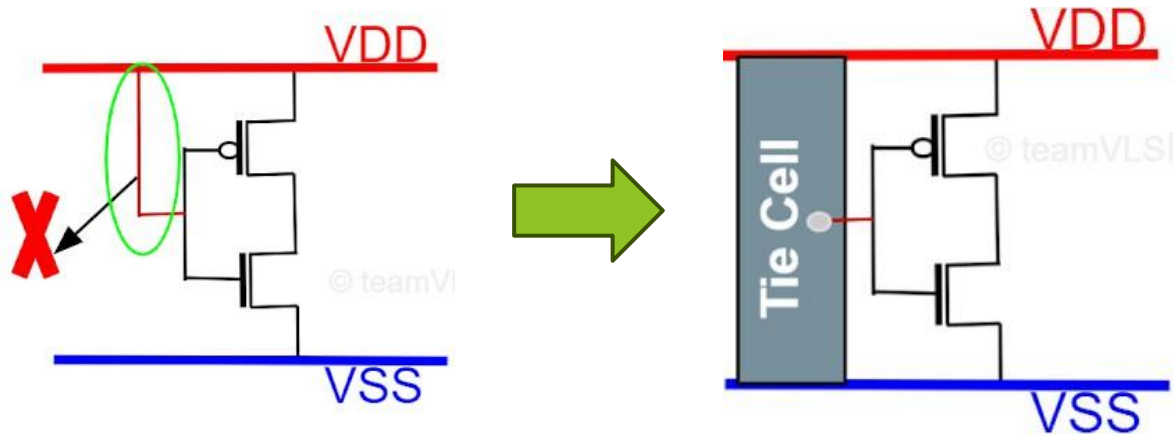
- Design Stage : Choose Post-CTS
- Analysis Type : Choose Hold



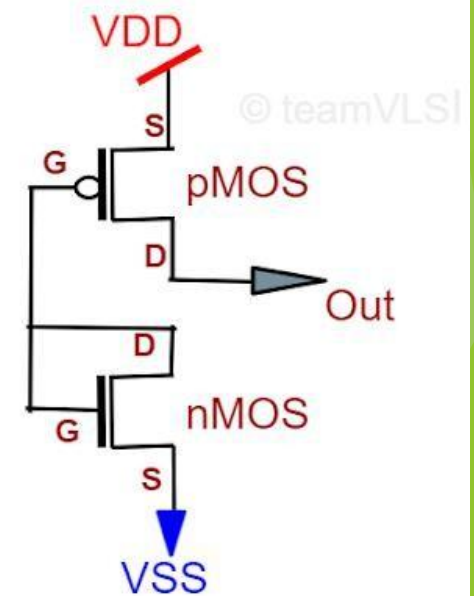
CTS(6/6)

► 8. Add Tie HI / LO cell

- Place → Tie HI / LO → Add
- Click Ok



Tie-low Cell



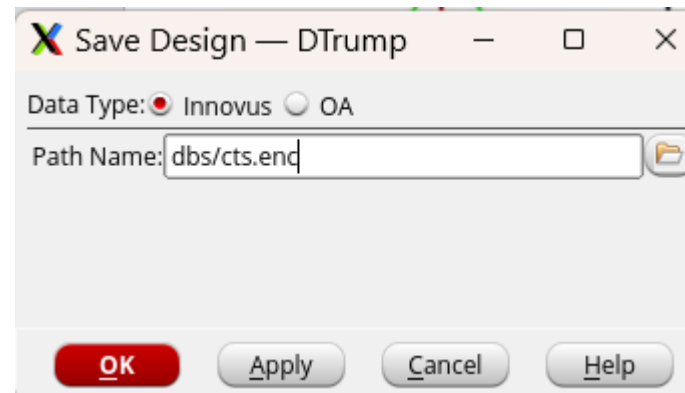
Tie-high Cell

CTS

► Save Design

File → Save Design

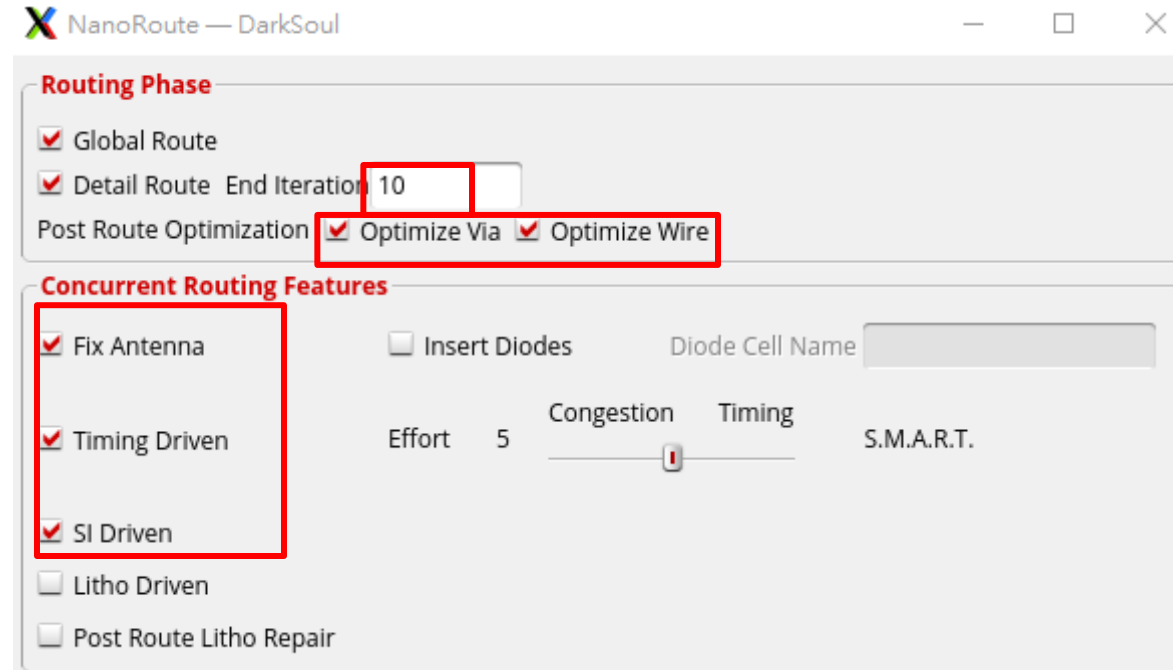
dbb/cts.ene



Route(1/5)

► 1. Start routing:

- Route → NanoRoute → Route
- Detail Route End Iteration :10
- In Routing Phase, select Optimize Via & Optimize Wire
- In Concurrent Routing Features, select Fix Antenna, Timing Driven, SI Driven
- Click OK



Route(2/5)

► 2. **innovus** > set_db delaycal_enable_si true

► 3. Timing → Report Timing

-Design Stage : Choose Post-Route

-Analysis Type : Choose Setup

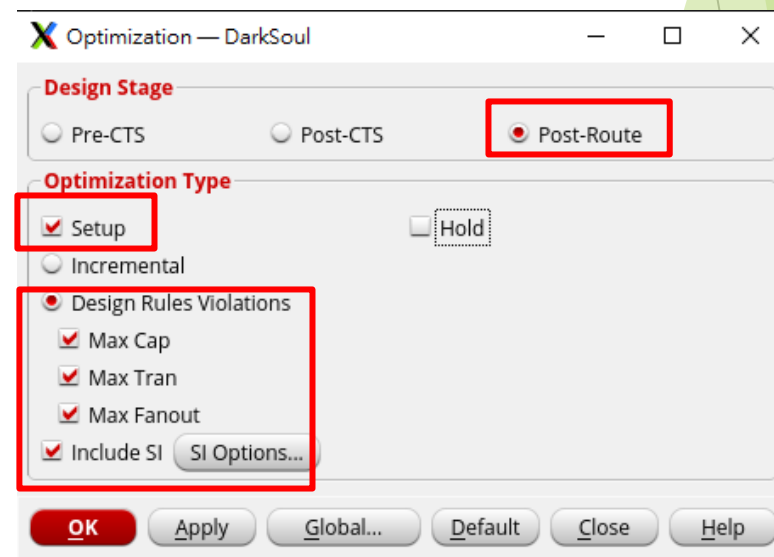
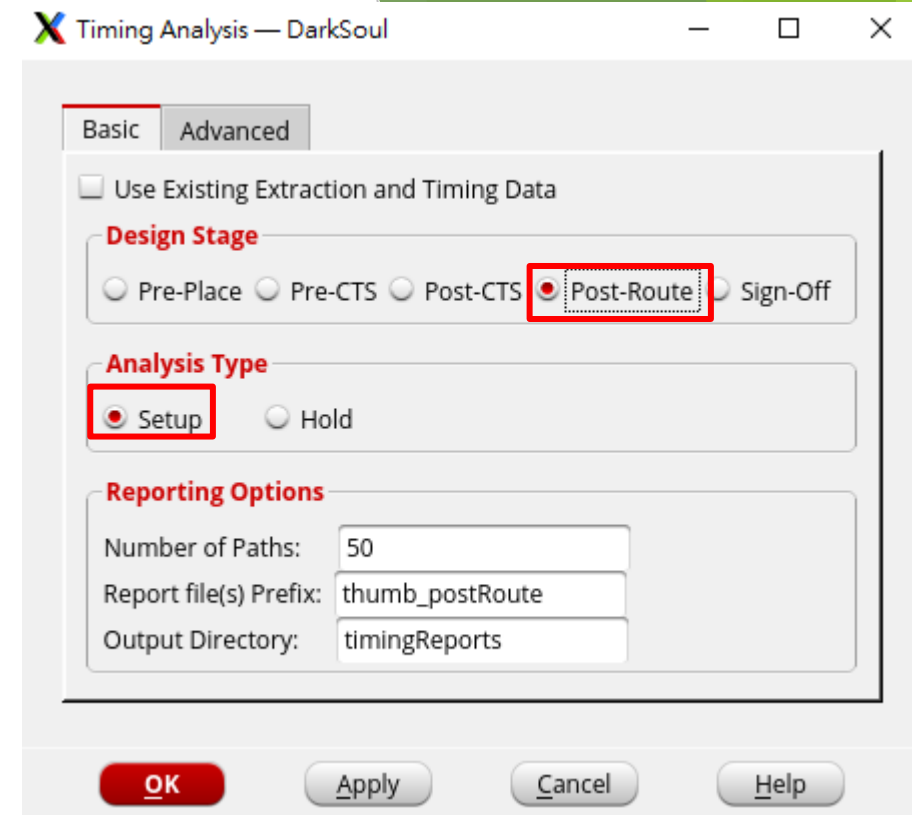
► 4. ECO → Optimize Design

- Design Stage : Choose Post-Route

-Optimization Type : Choose Setup

- Click OK

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.398	0.746	0.398	2.303	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0



Route(3/5)

► 5. Timing → Report Timing

-Design Stage : Choose Post-Route

-Analysis Type : Choose Hold

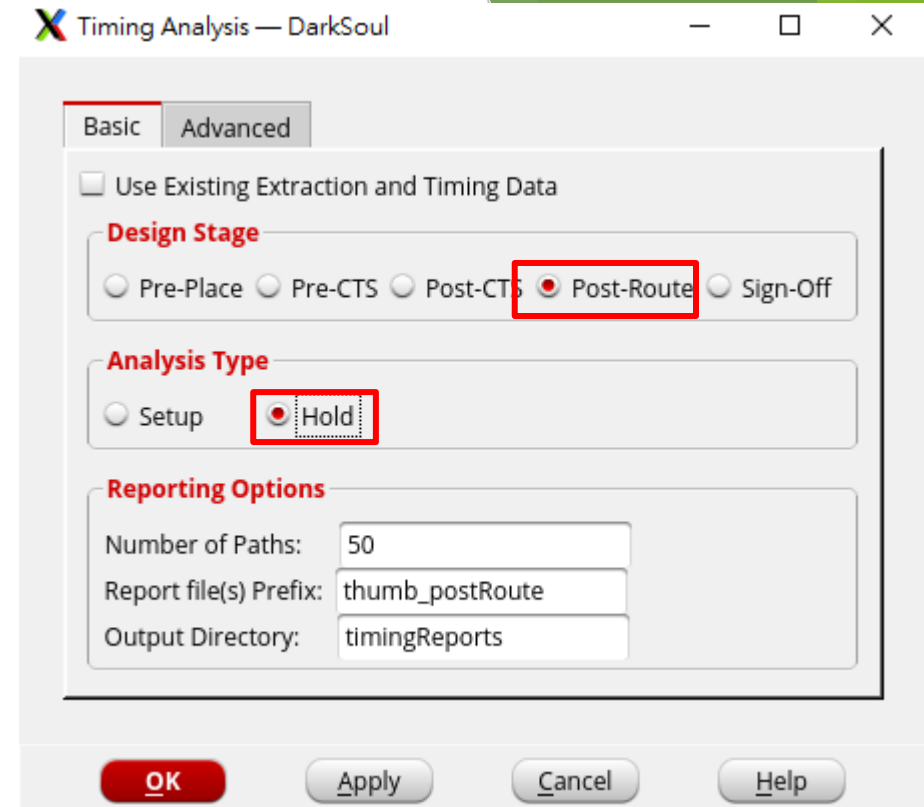
► 6. ECO → Optimize Design

- Design Stage : Choose Post-Route

-Optimization Type : Choose Hold

- Click OK

Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.004	0.004	0.034	0.086	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0



Timing Analysis — DarkSoul

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☐ Post-CTS ☒ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold

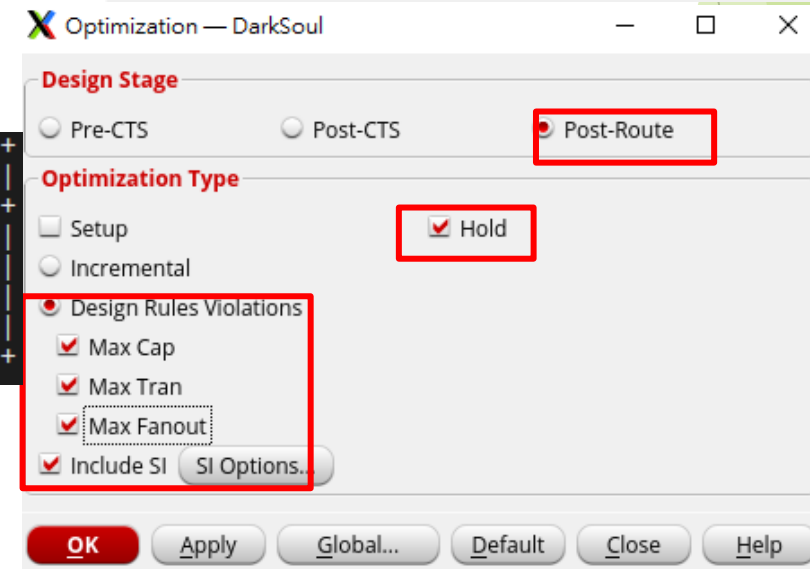
Reporting Options

Number of Paths: 50

Report file(s) Prefix: thumb_postRoute

Output Directory: timingReports

OK Apply Cancel Help



Optimization — DarkSoul

Design Stage

☐ Pre-CTS ☐ Post-CTS ☒ Post-Route

Optimization Type

☐ Setup ☒ Hold

☒ Design Rules Violations

☒ Max Cap

☒ Max Tran

☒ Max Fanout

☒ Include SI SI Options...

OK Apply Global... Default Close Help

Route(4/5)

► 7. Timing → Report Timing

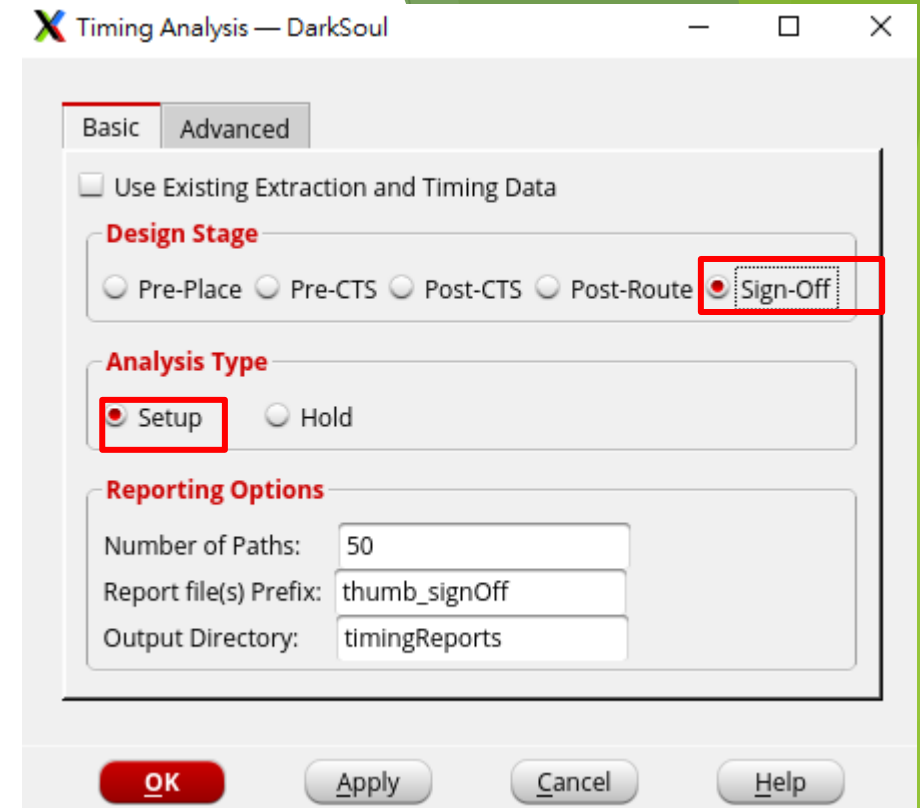
-Design Stage : Choose Sign-Off

-Analysis Type : Choose Setup

► 8. **innovus** > set_multi_cpu_usage -remote_host 8

innovus > opt_signoff –setup

(如果Timing沒過再修)



Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.730	0.730	1.319	2.302	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0

Route(5/5)

► 9. Timing → Report Timing

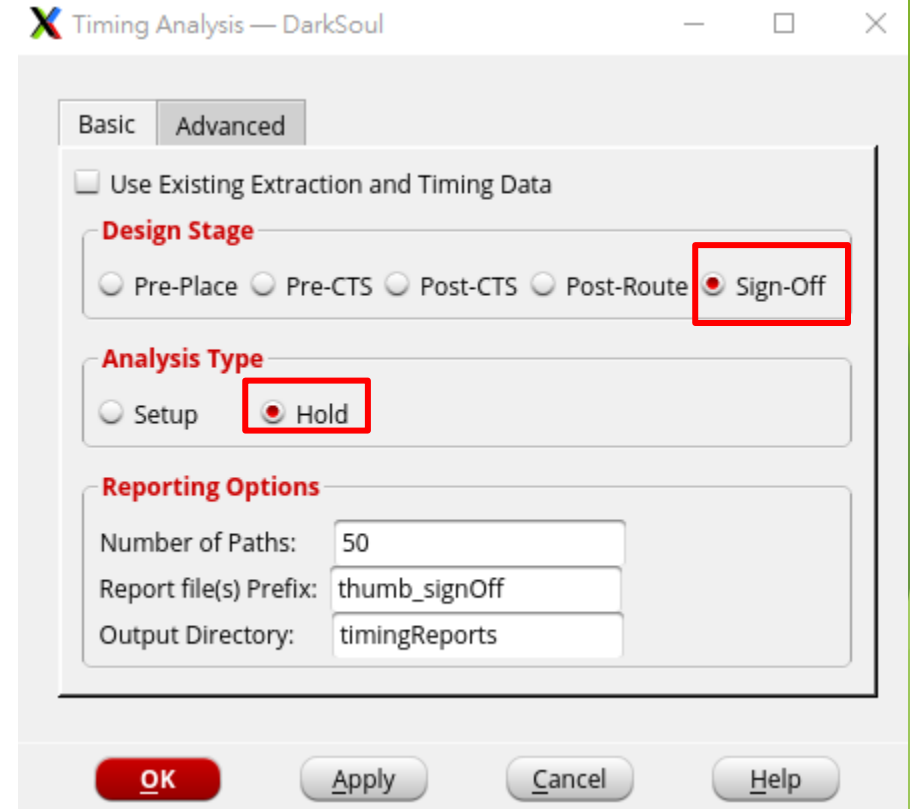
-Design Stage : Choose Sign-Off

-Analysis Type : Choose Hold

► 10. **innovus** > set_multi_cpu_usage -remote_host 8

innovus > opt_signoff -hold

(如果Timing沒過再修)



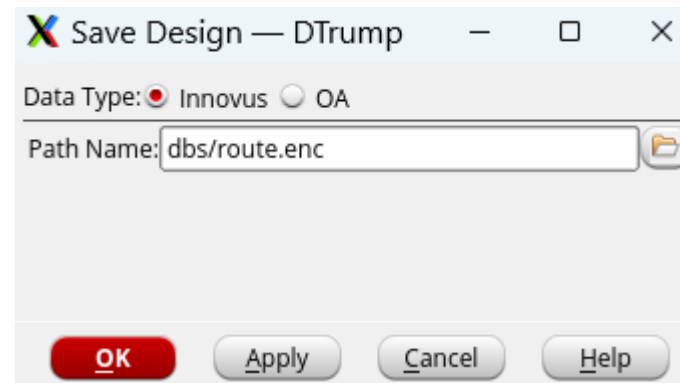
Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.008	0.008	0.018	0.090	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0

Route

► Save Design

File → Save Design

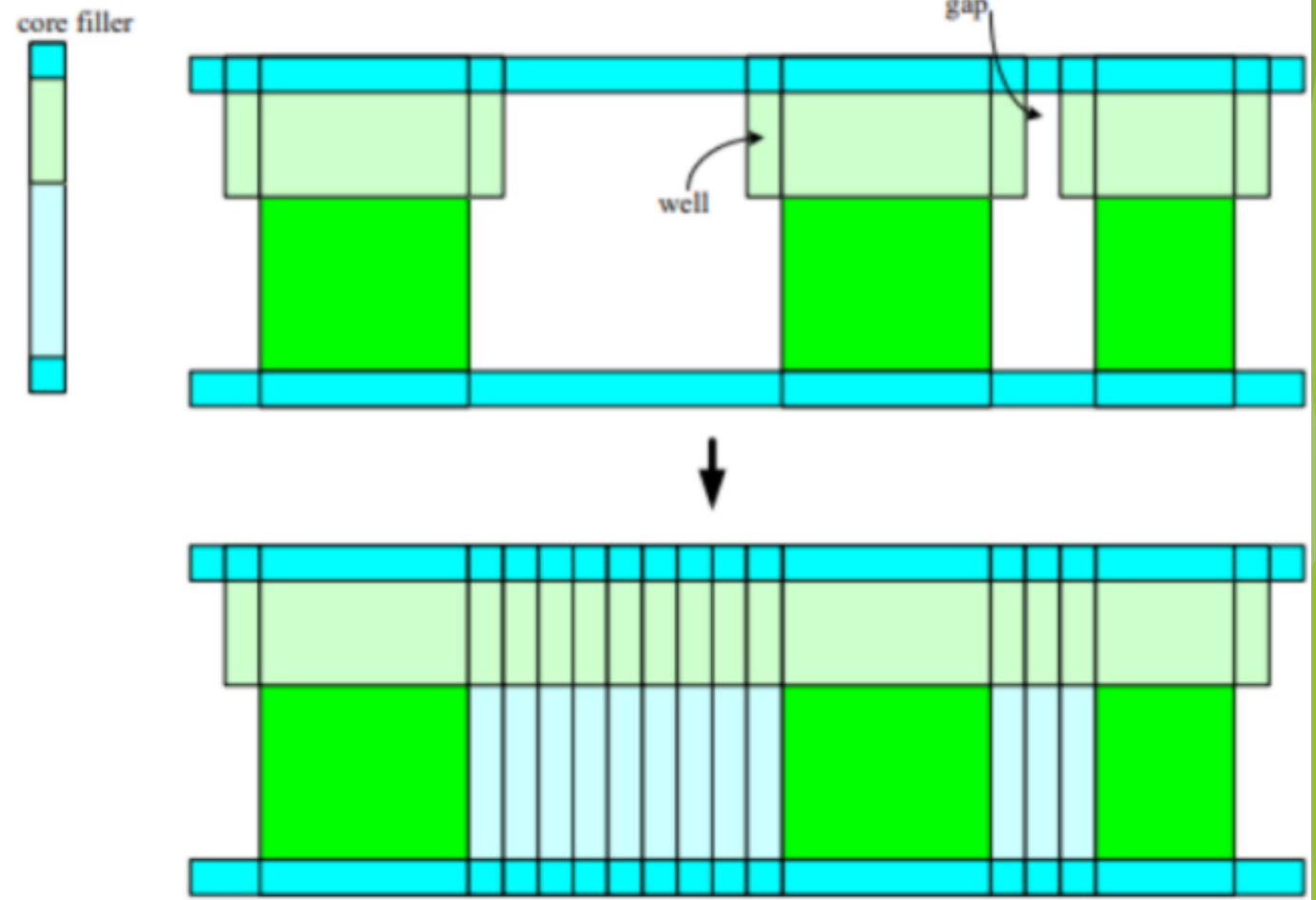
dbb/route.enc



Post processing(1/5)

► 1. Add Core Filler

- To fill the gap between cells.
- Start from wider filler to narrow filler



Post processing(2/5)

► 2. Add Core Filler:

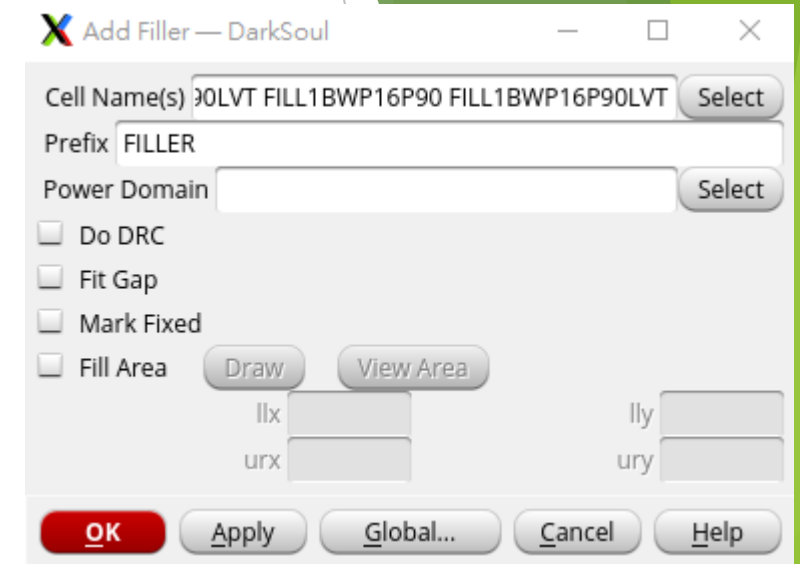
- **innovus** > get_db add_fillers_cells
- Place → Physical Cells → Add Filler → Click OK

► 3. Add VIA1 between M1 and M2

- **innovus** > source lab_script/post_via_drop.tcl

► 4. Check DRC

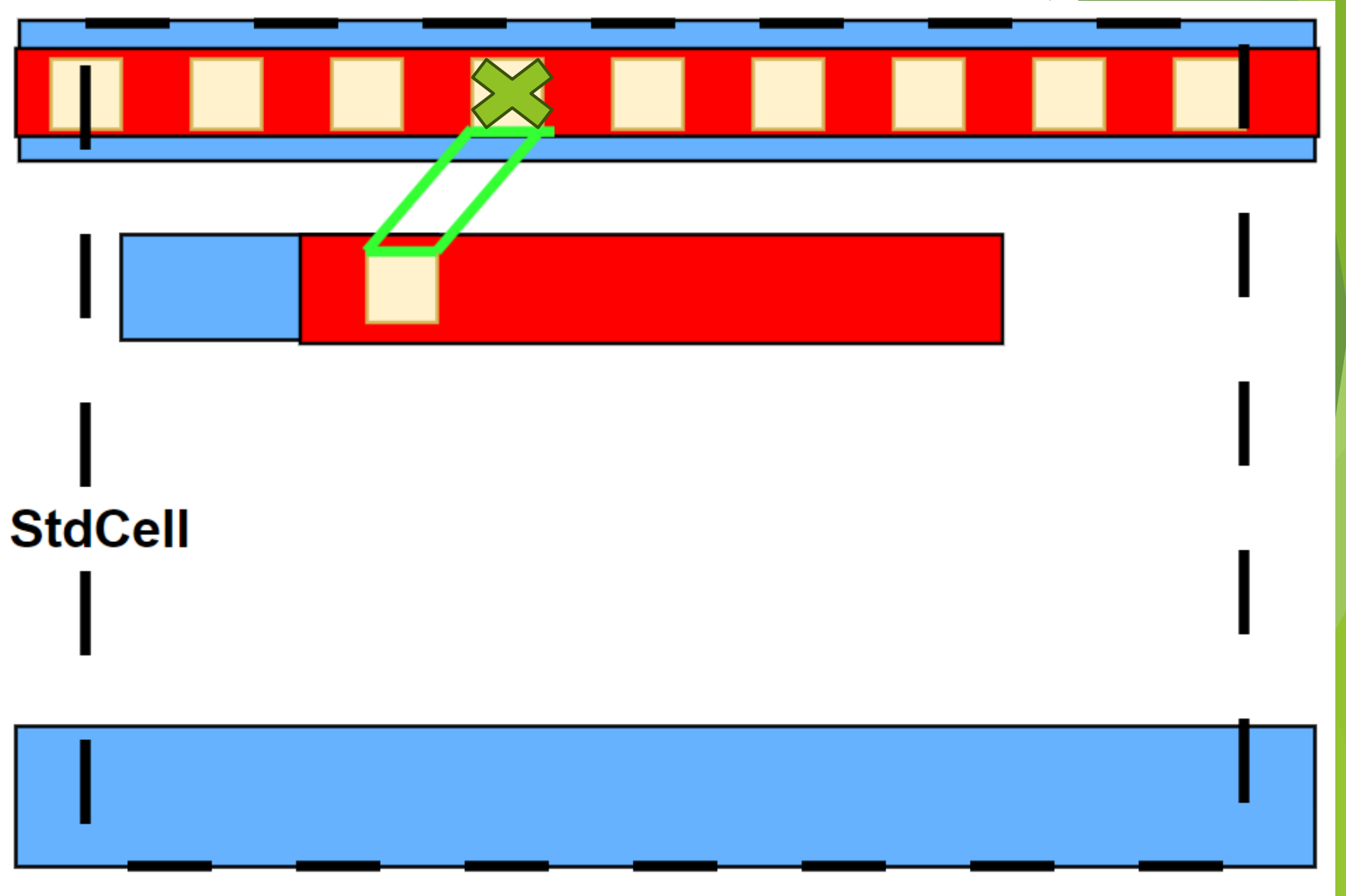
- **innovus** > set_db check_drc_limit 10000
- **innovus** > check_drc
- **innovus** > source lab_script/fix_manual_via12.tcl



```
VERIFICATION DRC ..... Thread : 2 finished.  
VERIFICATION DRC ..... Sub-Area: {0.000 187.488 27.280 214.272} 64 of 81 Thread : 6  
VERIFICATION DRC ..... Thread : 6 finished.  
VERIFICATION DRC ..... Sub-Area: {54.560 187.488 81.840 214.272} 66 of 81 Thread : 7  
VERIFICATION DRC ..... Thread : 7 finished.  
VERIFICATION DRC ..... Sub-Area: {218.240 187.488 241.380 214.272} 72 of 81 Thread : 0  
VERIFICATION DRC ..... Thread : 0 finished.  
VERIFICATION DRC ..... Sub-Area: {163.680 187.488 190.960 214.272} 70 of 81 Thread : 4  
VERIFICATION DRC ..... Thread : 4 finished.  
  
Verification Complete : 3 Viols
```

Post processing(3/5)

fix_manual_via12.tcl



Post processing(4/5)

► 5. Check → CheckDRC... → OK

► 6. Check → Check Connectivity

-Net Type → Choose **Regular Only**

-Net → **All**

-Check → un-choose DanglingWire(Antenna)

► 7. Finish Design

- **innovus** > source lab_script/write_netlist.tcl

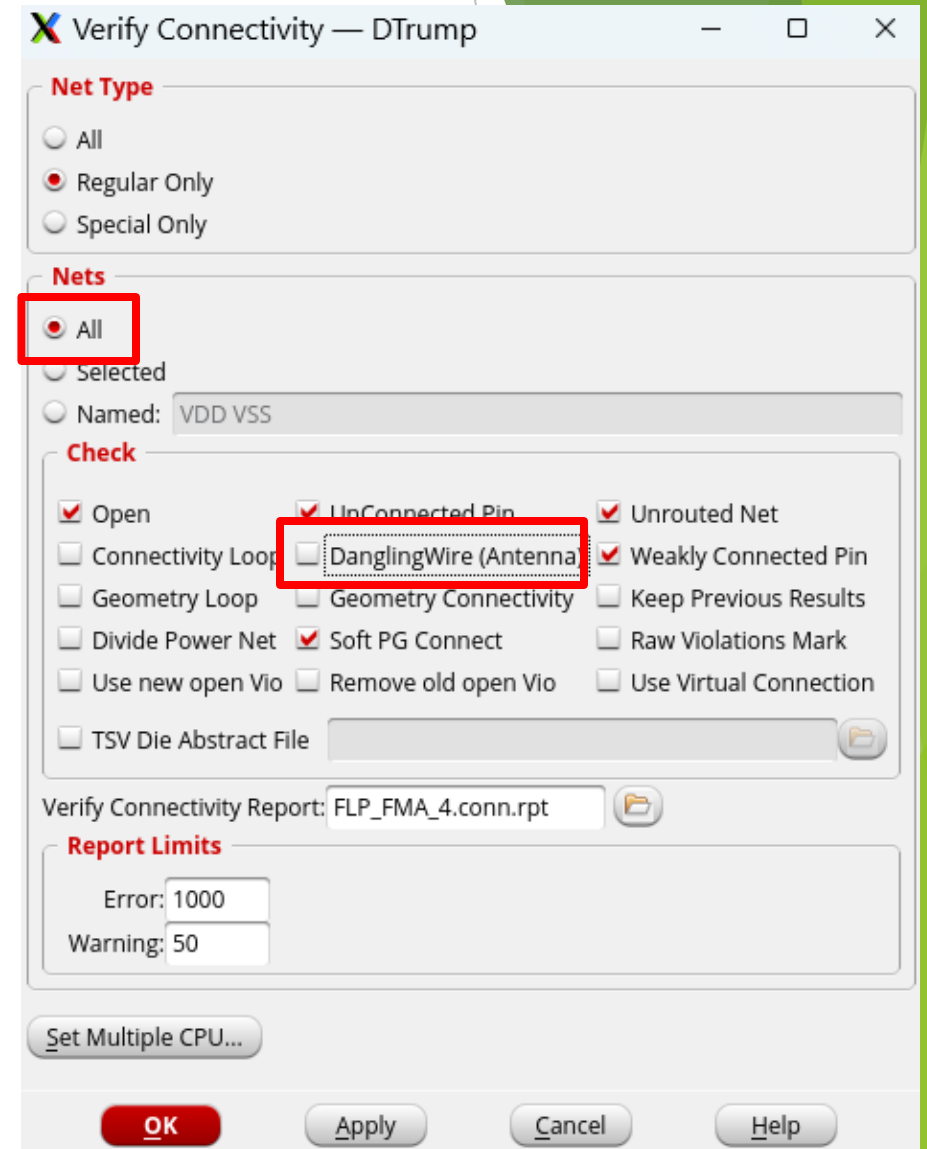
- **innovus** > source lab_APR_script/write_sdf.tcl

- **innovus** > source lab_script/write_stream.tcl

```
VERIFY DRC ..... Thread : 4 finished.  
VERIFY DRC ..... Thread : 6 finished.  
VERIFY DRC ..... Sub-Area: {190.960 187.488 218.240 214.272} 71 of 81 Thread : 3  
VERIFY DRC ..... Thread : 3 finished.
```

Verification Complete : **0 Viols**

```
*** End Verify DRC (CPU: 0:01:18 ELAPSED TIME: 14.00 MEM: 8.0M) ***
```



Post processing(5/5)

write_netlist.tcl

```
Delete_empty_hinsts

write_netlist outputs/FMA_pipe_pr.v
set TAP_CELL_LIST [get_db [get_db base_cells TAP_*] .name]
set BOUNDARY_CELL_LIST [get_db [get_db base_cells BOUNDARY_*] .name]
set DECAP_CELL_LIST [get_db [get_db base_cells DCAP_*] .name]
set PVDD_CELL_LIST [get_db [get_db base_cells PVDD_*] .name]
set FILLER_CELL_LIST [get_db [get_db base_cells FILL_*] .name]
set PFILLER_CELL_LIST [get_db [get_db base_cells PFILL_*] .name]
set PCORNER_CELL_LIST [get_db [get_db base_cells PCORNER_*] .name]
write_netlist -include_pg_ports -include_phys_cells "$TAP_CELL_LIST $BOUNDARY_CELL_LIST $DECAP_CELL_LIST $PVDD_CELL_LIST $FILLER_CELL_LIST $PFILLER_CELL_LIST $PCORNER_CELL_LIST" outputs/FMA_pipe_pg.v
```

write_sdf.tcl

```
write_sdf outputs/FMA_pipe_ff0p88v125c.sdf -max_view AV_func_ff0p88v125c
write_sdf outputs/FMA_pipe_ss0p72vm40c.sdf -max_view AV_func_ss0p72vm40c
```

write_stream.tcl

```
write_stream outputs/FMA_pipe.gds -map_file stream_out_map -lib_name DesignLib \
    -merge { \
        /home/cad/CBDK/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/GDS/N16ADFP_StdCell.gds \
    } \
    -uniquify_cell_names -unit 1000 -mode all -report_file write_stream.log

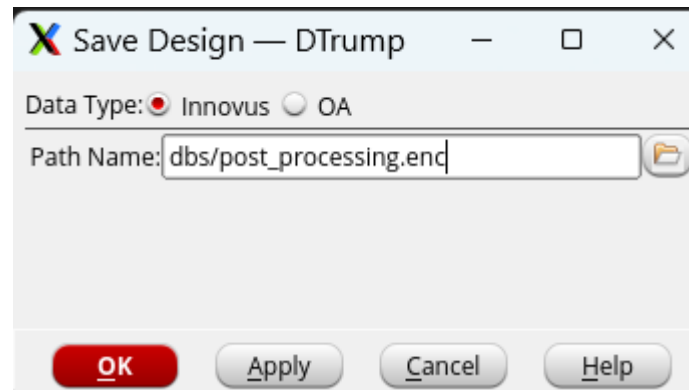
#create_pin_text -cells thumb label_loc.txt
```

Post processing

► Save Design

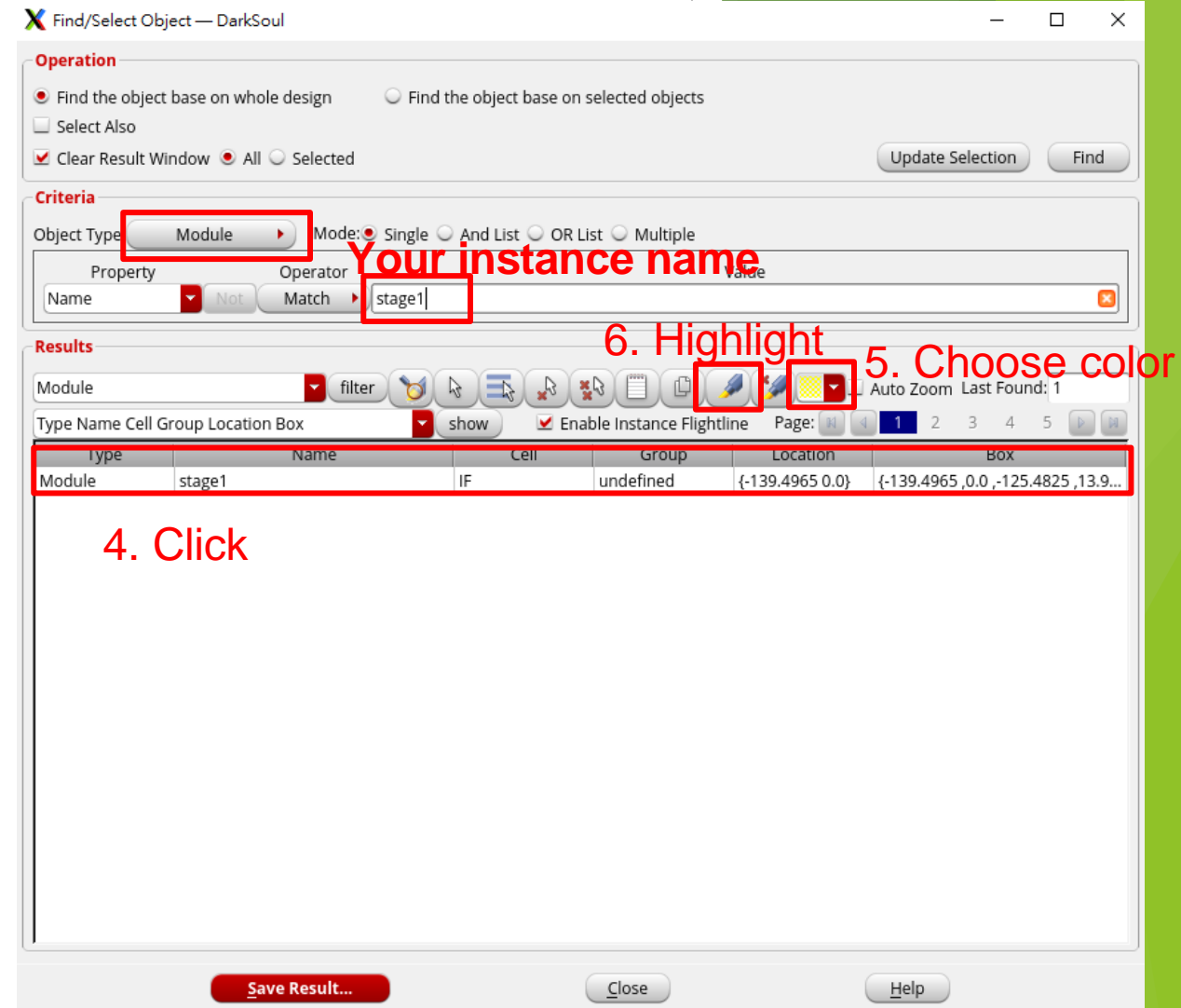
File → Save Design

dbb/post_processing.ene

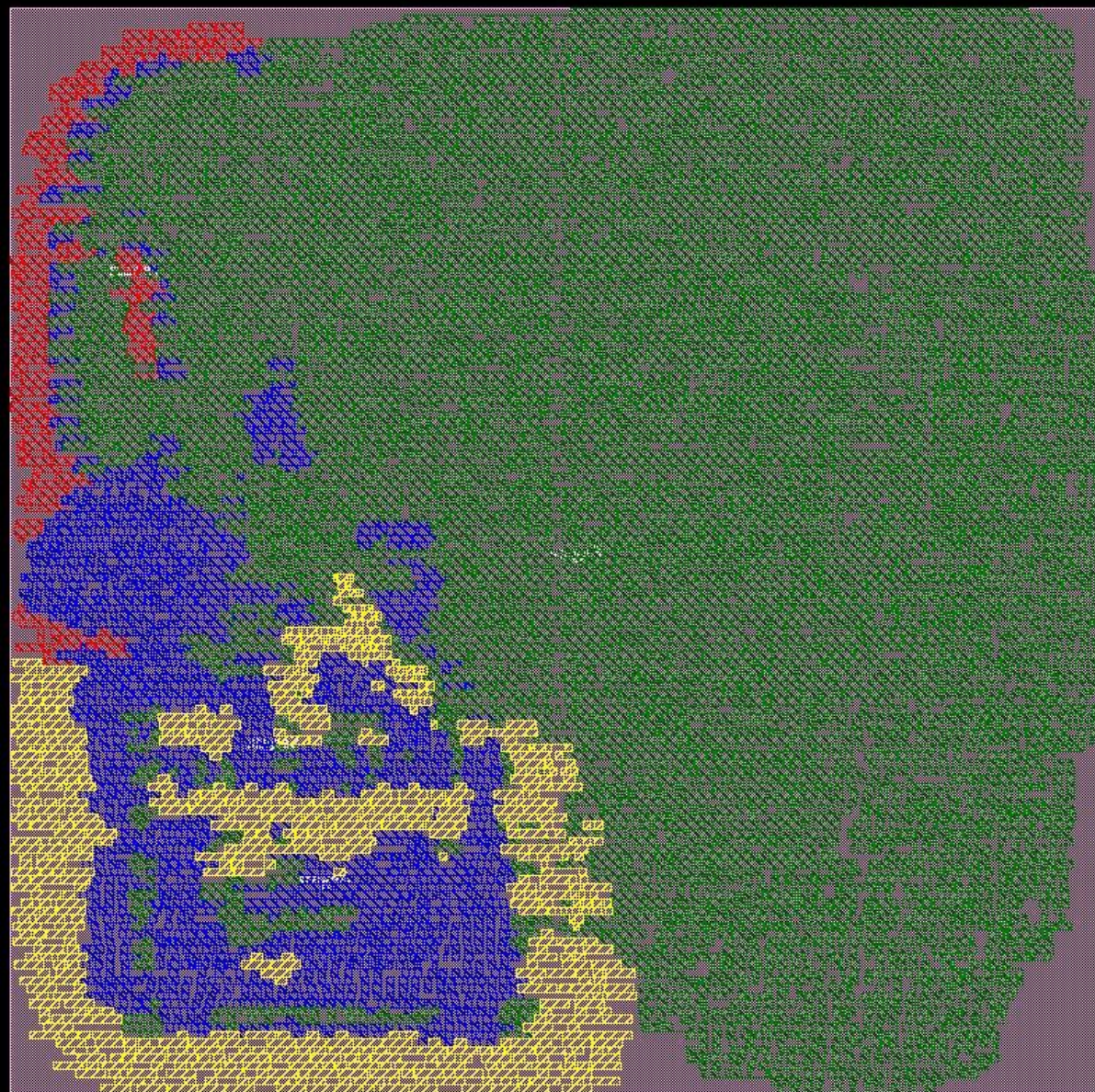
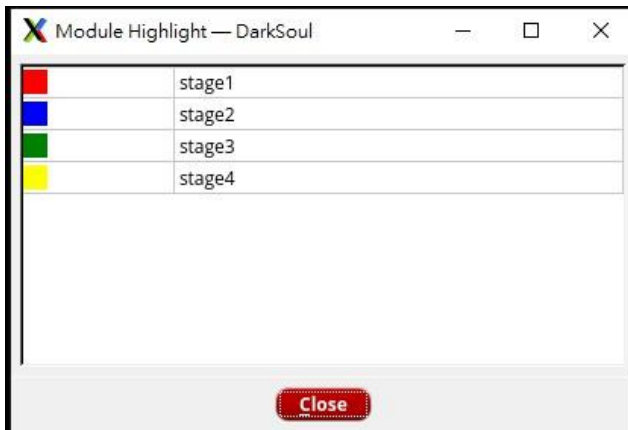


Highlight module(1/3)

- ▶ 1. ctrl +f
- ▶ 2. Select Module
- ▶ 3. Type stage1 → Enter



Highlight module(2/3)



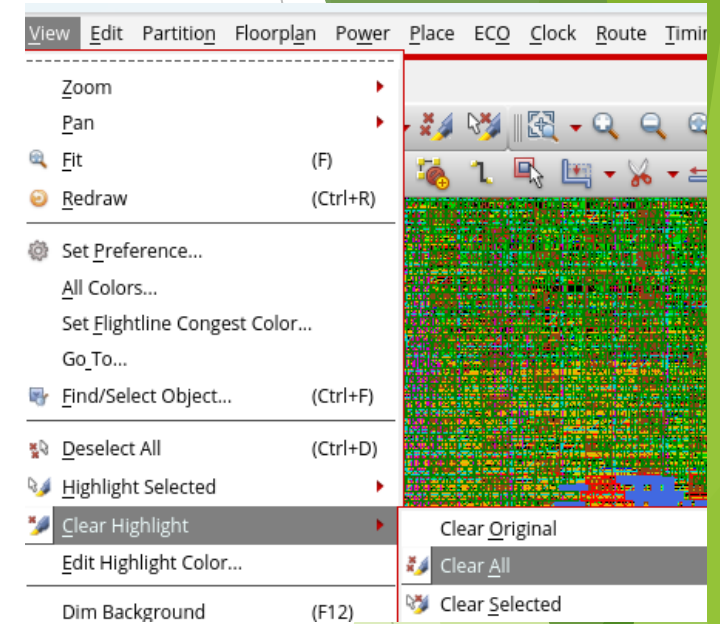
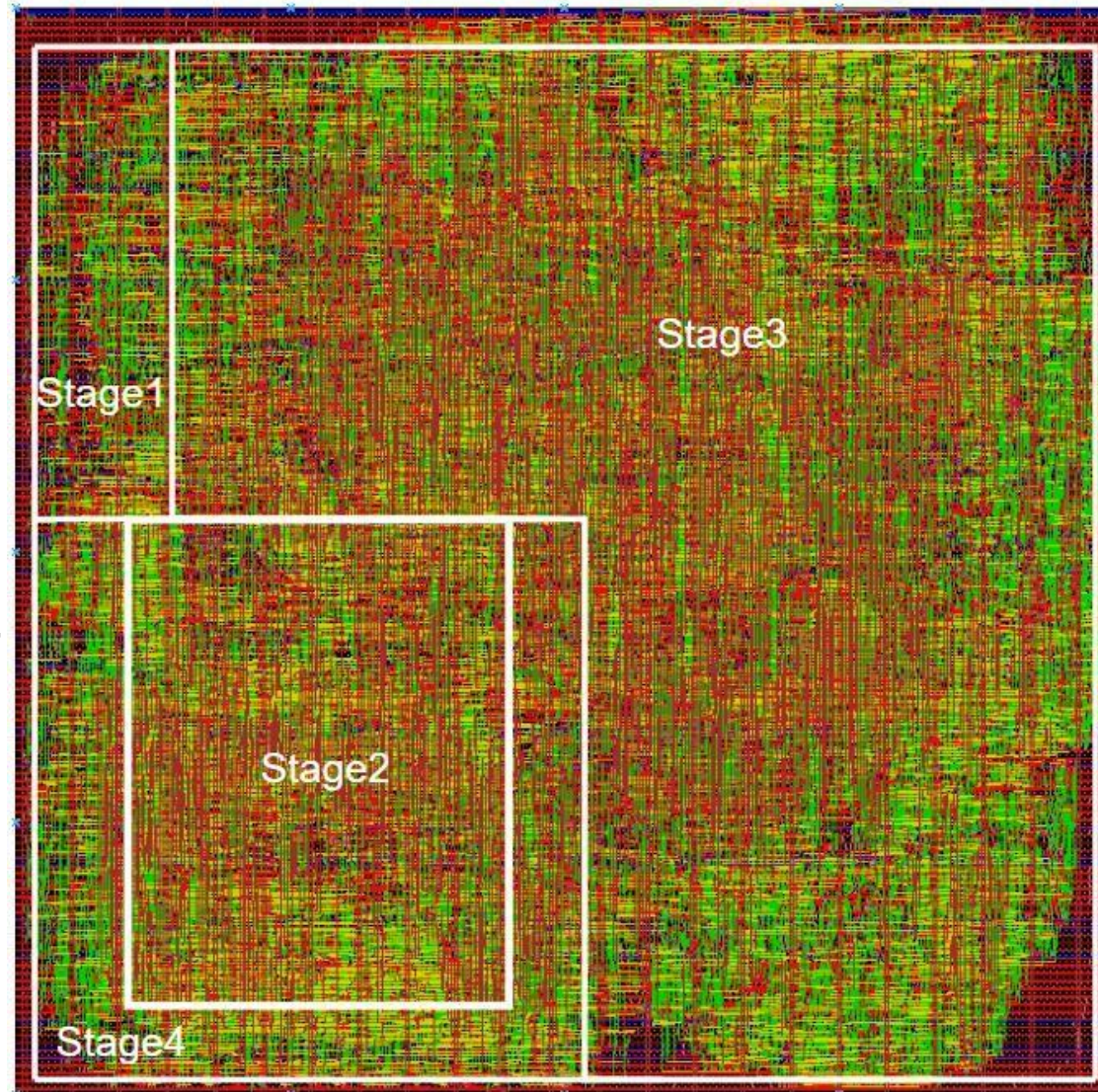
Highlight module(3/3)

► 1.用ipad繪圖

► 2.用小畫家繪圖

► 3.用任意方法繪圖

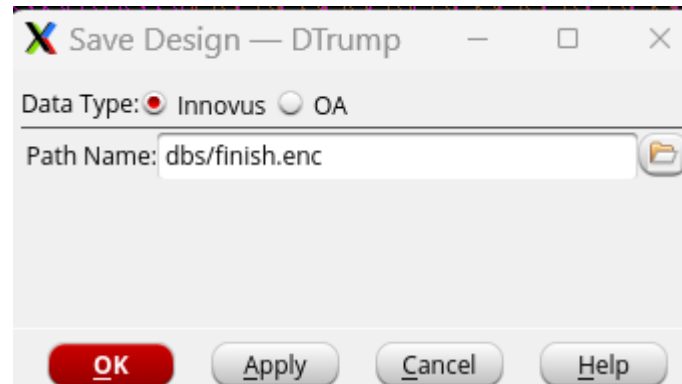
► 大致繪出各級面積即可



Finish

► Save Design

File → Save Design
dbs/finish.enc



The background features abstract, overlapping green geometric shapes, primarily triangles and polygons, in various shades of green, creating a modern, layered effect on the right side of the slide.

Thank you