

# Xilinx Vivado Tutorial

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2025/11/17  
EC5015-VLSILab

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# Outline

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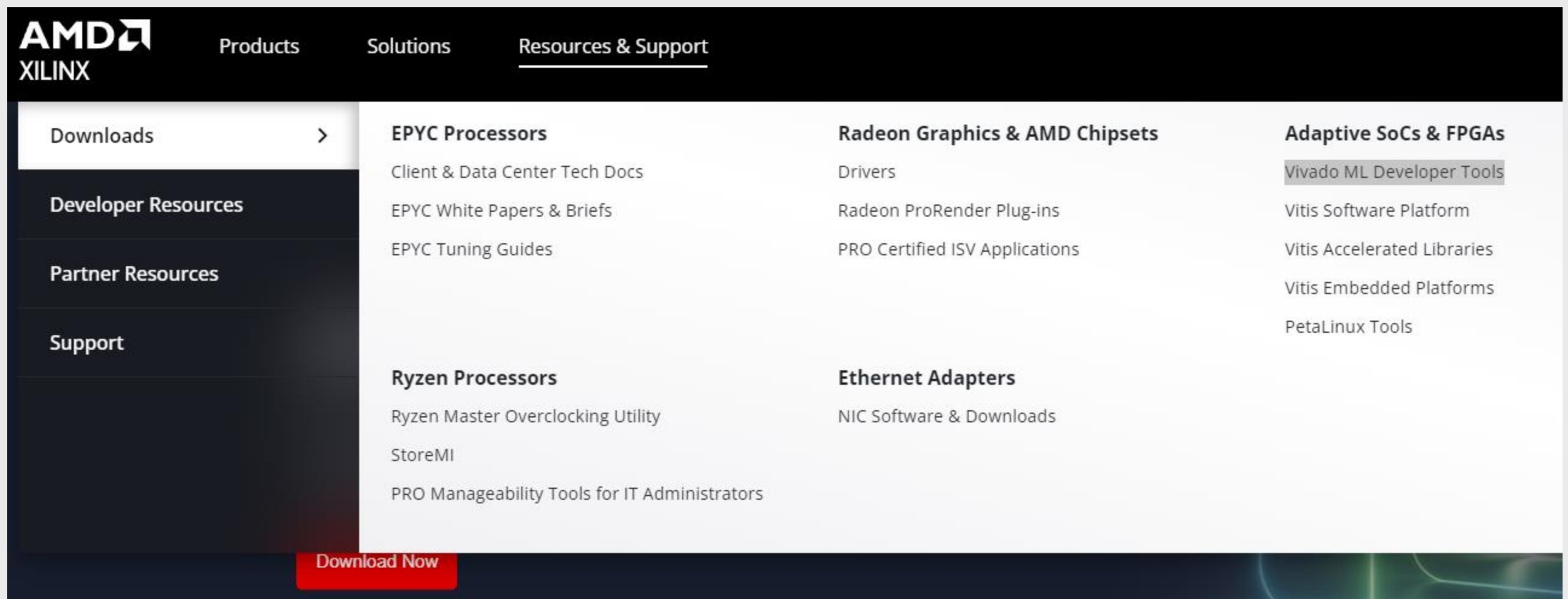
- 1. Download & Install**
- 2. Setup License**
- 3. Create Project**
- 4. Setting Constraint**
- 5. Xsim**
- 6. Synthesis & Implementation**
- 7. Summary**

# Download & Install (1/11)

1. 連結至Xilinx官網 Website:

<https://www.xilinx.com/products/design-tools/vivado.html>

2. Resources &Support->Downloads-> Vivado ML Developer Tools



# Download & Install (2/11)

3. 選擇Vivado Archive
4. 選擇2018.3並下載Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation裡的All OS installer Single-File Download

Version

- [2023.1](#)
- [2022.2](#)
- [2022.1](#)
- [Vivado Archive](#)**
- [ISE Archive](#)
- [CAE Vendor Libraries Archive](#)

## Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation

**Important**

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Note: Download verification is only supported with Google Chrome and Microsoft Edge web browsers.

Download Includes

Vivado Design Suite HLx Editions (All Editions)

Download Type

Full Product Installation

Last Updated

Dec 10, 2018

Answers

[2018.x - Vivado Known Issues](#)

Documentation

[Release Notes](#)

Support Forums

[Installation and Licensing](#)

📄 Vivado HLx 2018.3: All OS installer Single-File Download (TAR/GZIP - 18.97 GB)

MD5 SUM Value : 8a3a75f26d0e20de21fc673ad9d40d0f

Download Verification ⓘ

Digests

Signature

Public Key

點這個

# Download & Install (2/11)

5. 註冊一個帳號，此帳號然後之後安裝會用到
6. 辦好後就能下載



登入

電子郵件地址

密碼

登入

或

創建密碼

[忘記/重設密碼？](#)

[幫助](#) [使用條款](#) [隱私權](#)

Business E-mail\*

Company Name\*

Please enter the name of your business or institution.

Address 1\*

Address 2

Location\*

State

City\*

Posta

Phone

Job Function\*

For more information about how we process your personal information, please see our [privacy policy](#).

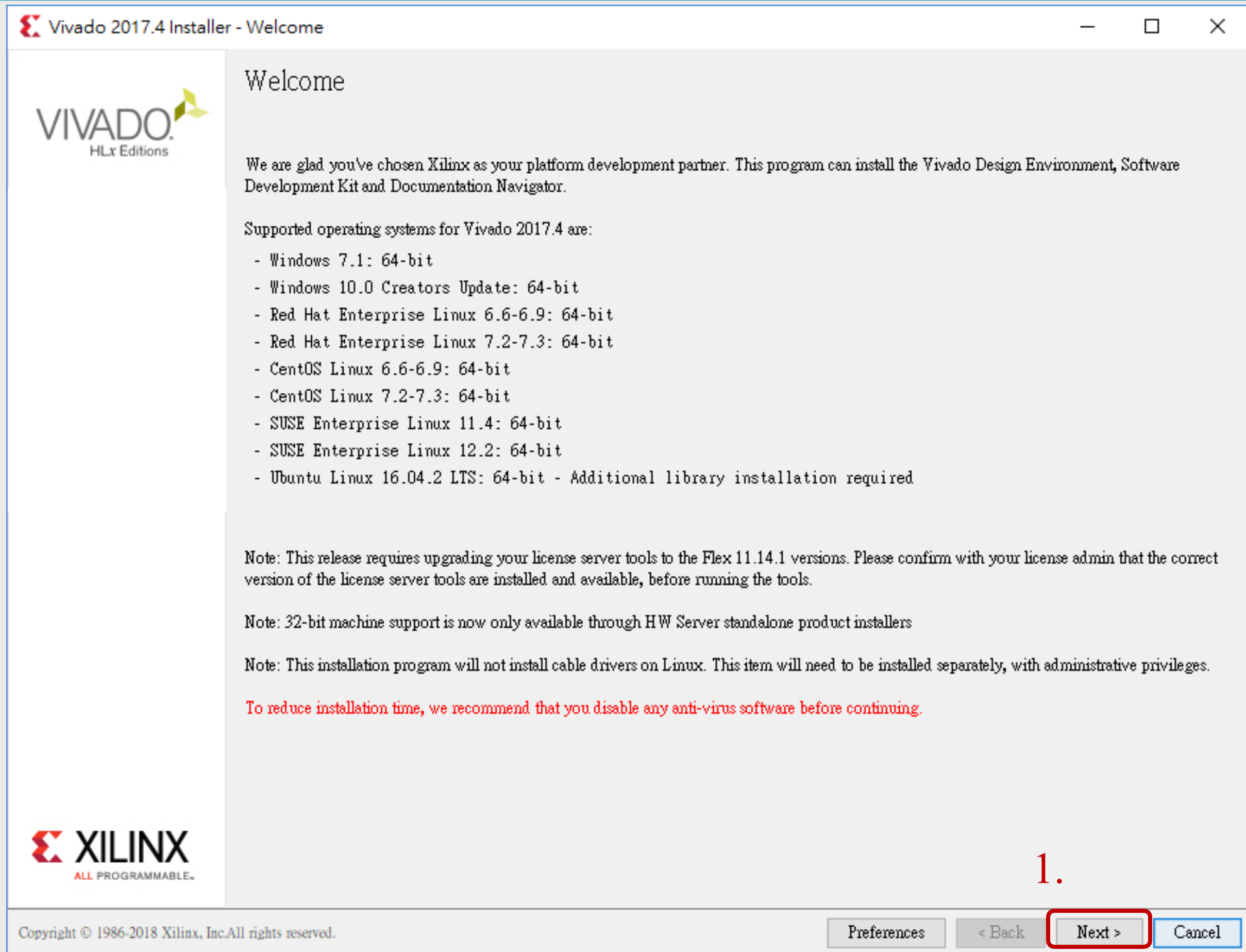
Download

# Download & Install (3/11)

---

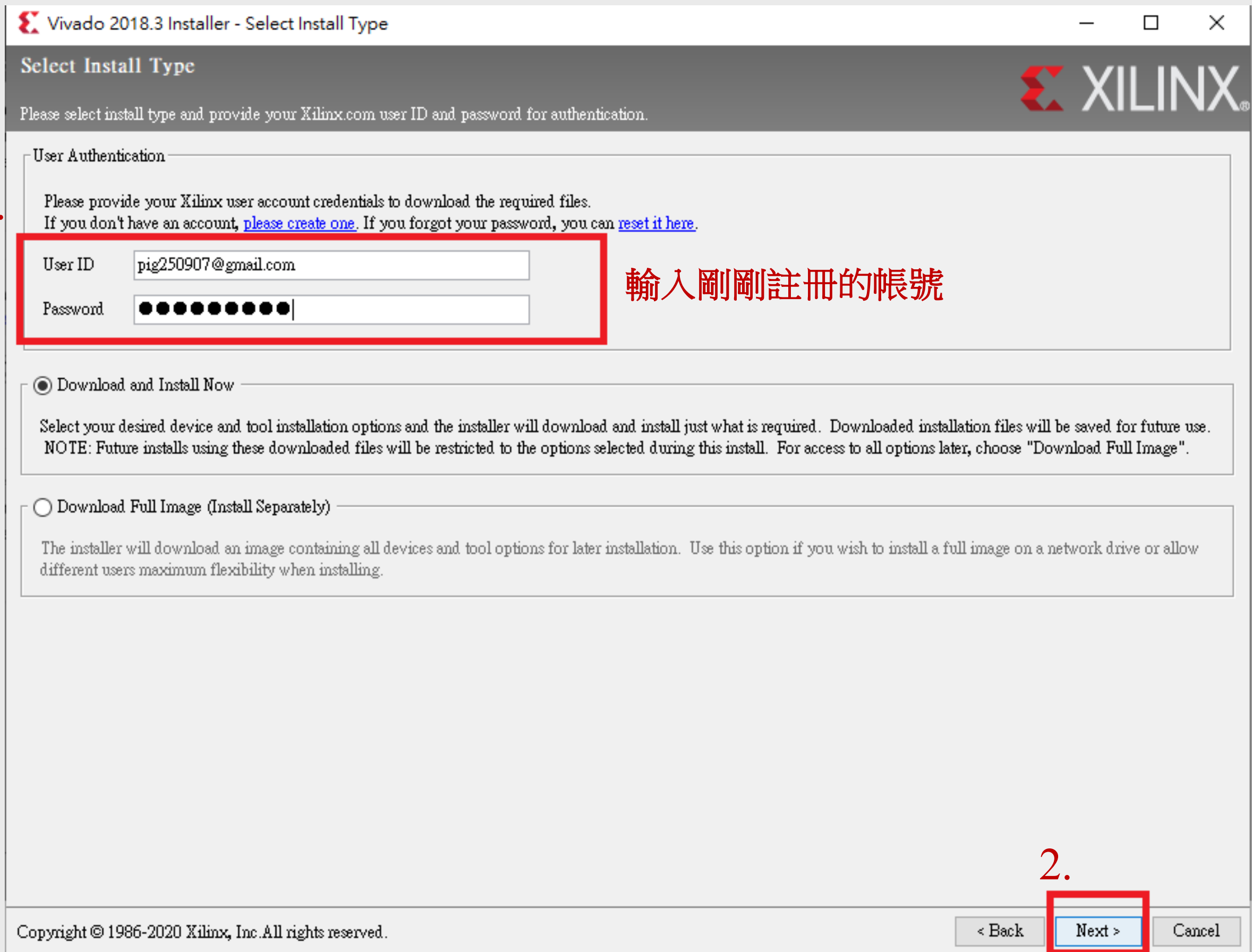
1. Exunzip vivado.
2. execute installer
  - Windows :
    - A. Go to folder of vivado
    - B. Double-Click xsetup.exe
  - Linux :
    - A. Open terminal
    - B. `cd <path to folder of vivado>`
    - C. `sudo ./xsetup`

# Download & Install (4/11)



# Download & Install (5/11)

1.



The image shows the 'Vivado 2018.3 Installer - Select Install Type' window. The title bar includes the Xilinx logo and the text 'Vivado 2018.3 Installer - Select Install Type'. The window has a dark header bar with the Xilinx logo and the text 'XILINX®'. Below the header, there is a section titled 'Select Install Type' with the instruction: 'Please select install type and provide your Xilinx.com user ID and password for authentication.' The main content area is divided into two sections. The first section is 'User Authentication' with the text: 'Please provide your Xilinx user account credentials to download the required files. If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).' Below this text are two input fields: 'User ID' with the value 'pig250907@gmail.com' and 'Password' with a masked password represented by black dots. The second section contains two radio button options: 'Download and Install Now' (selected) and 'Download Full Image (Install Separately)'. The 'Download and Install Now' option has a note: 'Select your desired device and tool installation options and the installer will download and install just what is required. Downloaded installation files will be saved for future use. NOTE: Future installs using these downloaded files will be restricted to the options selected during this install. For access to all options later, choose "Download Full Image".' The 'Download Full Image (Install Separately)' option has a note: 'The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.' At the bottom of the window, there is a footer with the text 'Copyright © 1986-2020 Xilinx, Inc. All rights reserved.' and three buttons: '< Back', 'Next >', and 'Cancel'. The 'Next >' button is highlighted with a red box.

Vivado 2018.3 Installer - Select Install Type

Select Install Type

Please select install type and provide your Xilinx.com user ID and password for authentication.

User Authentication

Please provide your Xilinx user account credentials to download the required files.  
If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).

User ID: pig250907@gmail.com

Password: ●●●●●●●●●●

☒ Download and Install Now

Select your desired device and tool installation options and the installer will download and install just what is required. Downloaded installation files will be saved for future use.  
NOTE: Future installs using these downloaded files will be restricted to the options selected during this install. For access to all options later, choose "Download Full Image".

☐ Download Full Image (Install Separately)

The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.

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< Back Next > Cancel


輸入剛剛註冊的帳號

2.



# Download & Install (5/11)

 — □ ×

**Accept License Agreements** 

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

**Xilinx Inc. End User License Agreement**

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

1. ☒ **I Agree**

**WebTalk Terms And Conditions**

By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

☒ **I Agree**

**Third Party Software End User License Agreement**

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ **I Agree**

2.

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# Download & Install (6/11)

**Vivado 2017.4 Installer - Select Edition to Install**

**Select Edition to Install**

Select an edition to continue installation. You will be able to customize the content in the next page.

☐ Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

☐ Vivado HL Design Edition

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

**1. ☒ Vivado HL System Edition**

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

☐ Documentation Navigator (Standalone)

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

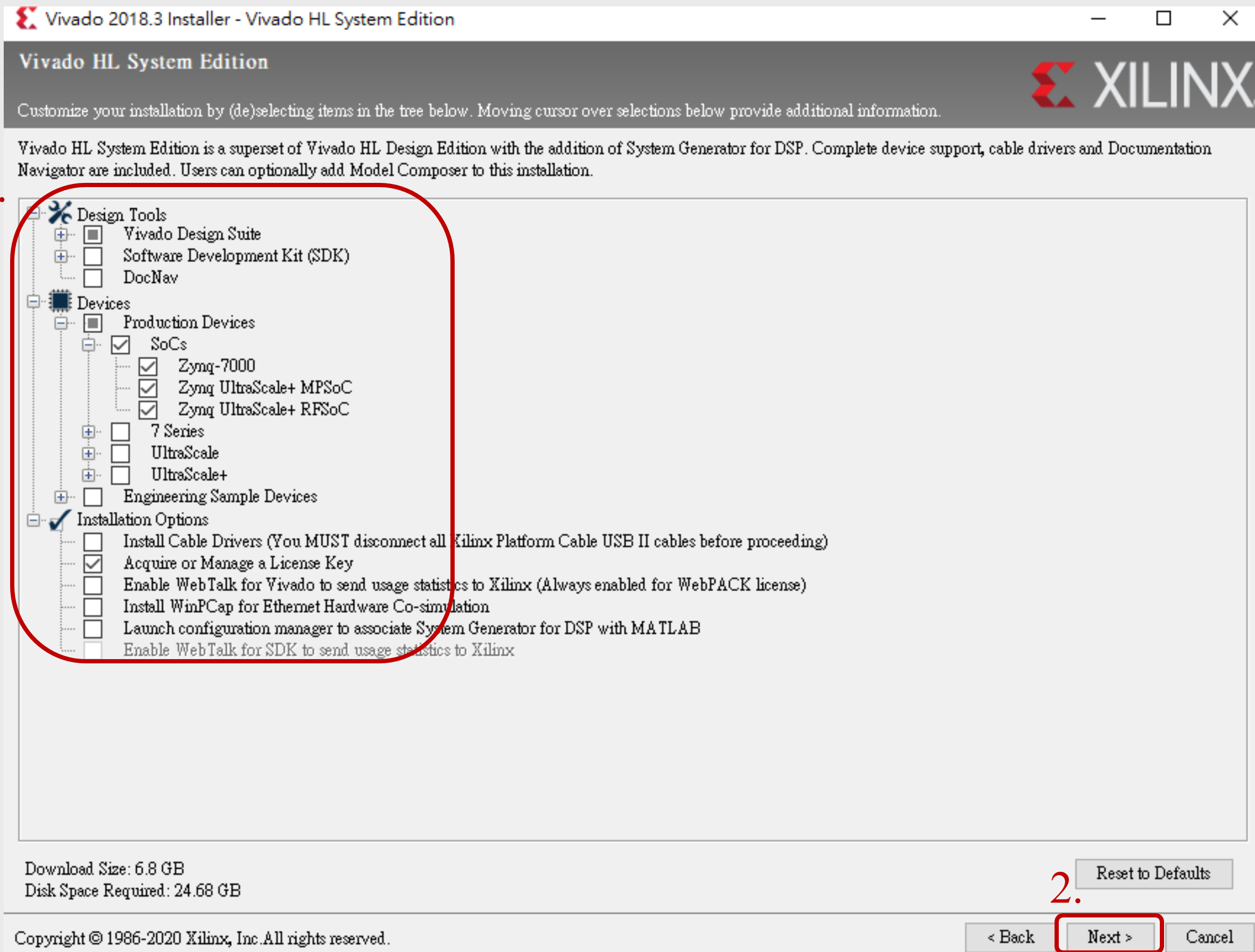
**2.**

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< Back **Next >** Cancel

# Download & Install (7/11)

1.



# Download & Install (8/11)

**Vivado 2017.4 Installer - Select Destination Directory**

**Select Destination Directory**

Choose installation options such as location and shortcuts.

**Installation Options**

Select the installation directory

C:\Xilinx

**Installation location(s)**

C:\Xilinx\Vivado\2017.4  
C:\Xilinx\DocNav

**Disk Space Required**

Download Size: NA  
Disk Space Required: 11.98 GB  
Disk Space Available: 64.64 GB

**Select shortcut and file association options**

☒ Create program group entries  
Xilinx Design Tool

☒ Create desktop shortcuts

☒ Create file associations

Apply shortcut & file association selections to

☐ Current user

☒ All users

**1.**

**2.**

**3.**

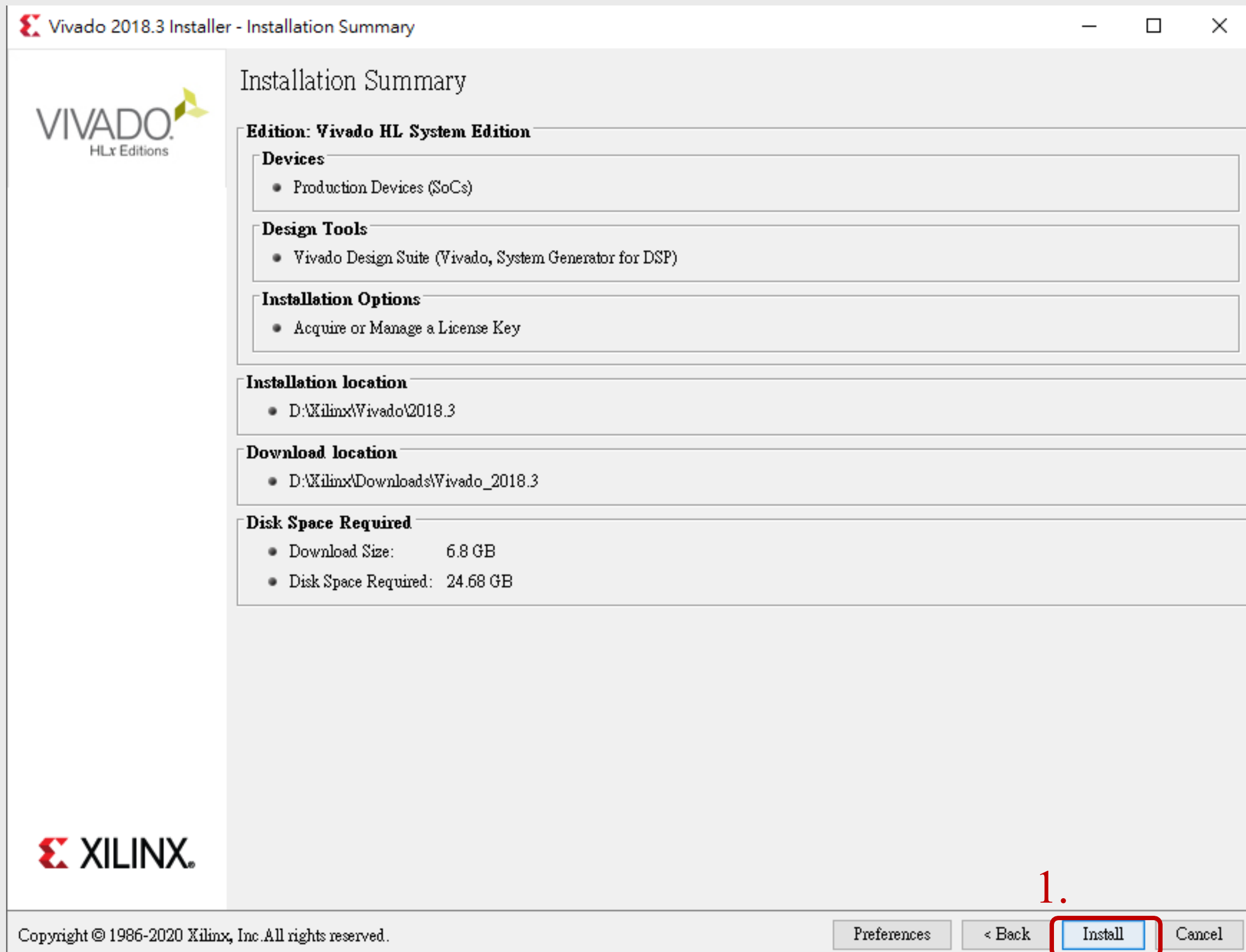
If you aren't windows, please don't select.

< Back Next > Cancel

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# Download & Install (9/11)

- 如安裝完成後遇到License，可先至18頁設定。



# Download & Install (11/11)

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After installing vivado, you can open vivado by following :

1. Window :

◆ Double-Click the icon



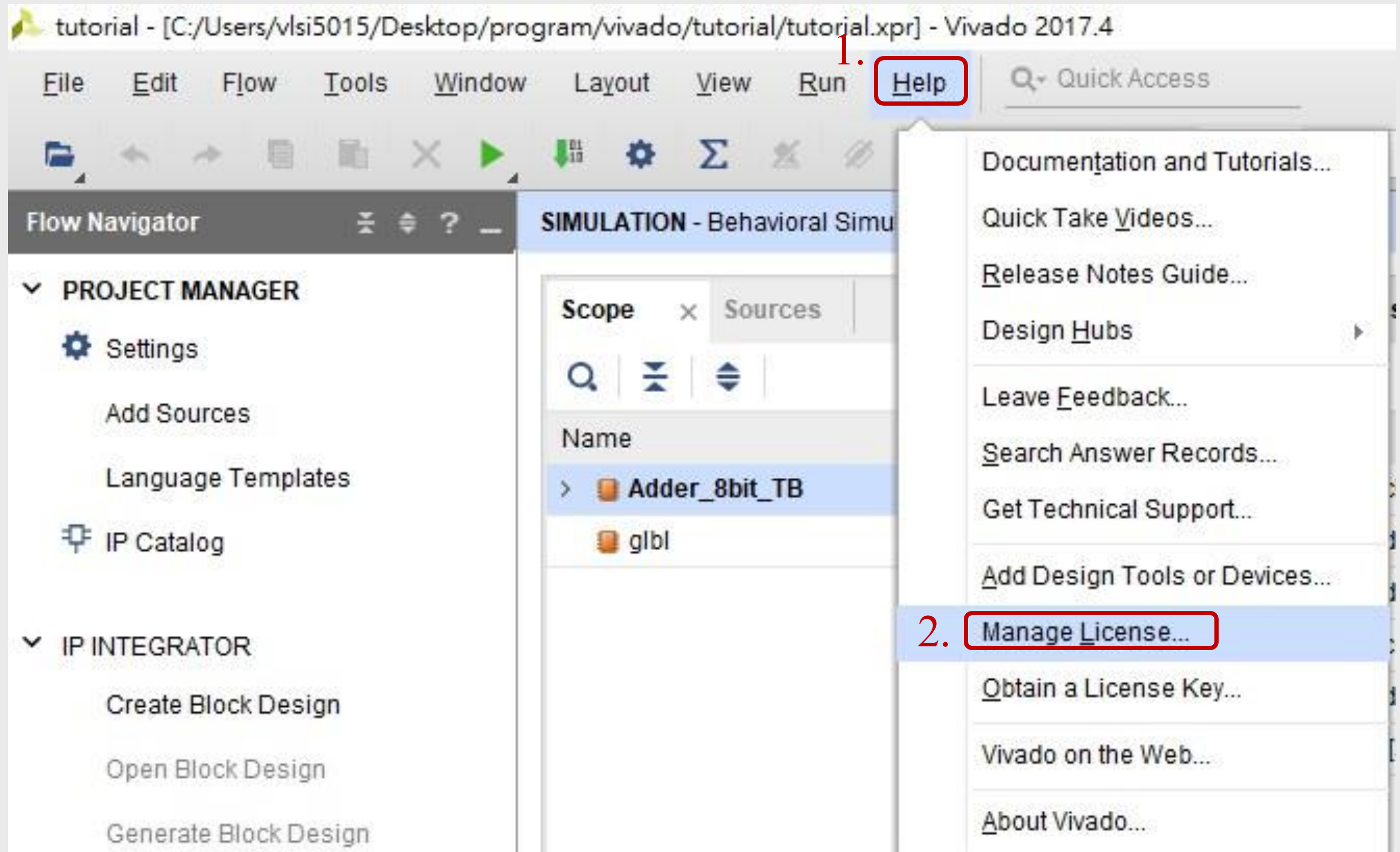
# Outline

---

1. Download & Install
- 2. Setup License**
3. Create Project
4. Setting Constraint
5. Xsim
6. Synthesis & Implementation
7. Summary



# Setup License (1/3)





# Setup License (2/3)

The screenshot shows the Vivado License Manager 2018.3 application window. The title bar reads 'Vivado License Manager 2018.3'. The menu bar contains 'File' and 'Help'. The main header area features the 'VIVADO' logo and 'License Manager' text on the left, and the 'XILINX' logo on the right. A left-hand sidebar contains a tree view with the following items: 'Get License' (with a sub-menu containing 'Set Proxy', 'Obtain License', and 'Load License'), 'Manage License' (with a sub-menu containing 'Manage License Search Paths', 'View License Status', and 'View System Information'), and 'View Host Information'. The 'Manage License Search Paths' item is highlighted with a red box and a red number '1' next to it. The main content area is titled 'Manage License Search Paths' and contains the following text: 'To point to a floating server license, or to point to license files in locations other than %APPDATA%\Xilinx\License, set one of the environment variables below. XILINXD\_LICENSE\_FILE is the preferred environment variable for working with Xilinx licenses.' Below this, three examples are provided: 'Example: Pointing to a floating server license' with the command 'XILINXD\_LICENSE\_FILE=1234@server', 'Example: Including additional local directories' with the command 'XILINXD\_LICENSE\_FILE=C:\licenses\Xilinx.lic', and 'Example: Pointing to multiple locations' with the command 'XILINXD\_LICENSE\_FILE=1234@server;C:\licenses\Xilinx.lic'. A red number '2' is placed above the input field for 'XILINXD\_LICENSE\_FILE', which contains the text '10709@140.117.168.141' and is highlighted with a red box. Below this is an empty input field for 'LM\_LICENSE\_FILE'. At the bottom left of the main content area is a 'Set' button.

Vivado License Manager 2018.3

File Help

VIVADO License Manager

XILINX

1. Manage License Search Paths

2. XILINXD\_LICENSE\_FILE 10709@140.117.168.141

LM\_LICENSE\_FILE

Set

# Setup License (3/3)

Vivado License Manager 2017.4

File Help

VIVADO. License Manager

XILINX ALL PROGRAMMABLE.

1. Get License

- Set Proxy
- Obtain License
- Load License

2. Manage License

- Manage License Search Paths
- View License Status**
- View System Information
- View Host Information

3. If you set license successfully, you will see a lot of items in this field.

View License Status

Filter: ☒ Hide Free Built-in Licenses

License Name	Tools/IP	Expiration Date	Version Limit	License Type	Location	#
PartialReconfiguration	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
PartialReconfiguration	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
PlanAhead	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
SDK	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
SDK	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
SDSoC_Tools	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
Simulation	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
Simulation	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
Synthesis	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
SysGen	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
Vivado_System_Edition	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur
KC7Z010	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppData...	Ur

Activation Based Licenses:

NOTE: Support for activation based licenses has been deprecated. Your existing activation licenses have been replaced with certificate based licenses and added into your licensing account.


License Name	Tools/IP	Expiration Date	Version Limit	Server/Client	Location	# of S
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# Outline

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- 2. Setup License**
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# Create Project (1/8)

1.  Vivado 2017.4 File Flow Tools Window Help Q- Quick Access

2.  New Project... Open Project... Open Recent Project Open Example Project... Open Checkpoint... Open Recent Checkpoint New IP Location... Open IP Location... Open Recent IP Location Import Exit

**Recent Projects**

Wu_CNN_Rewrited	C:/Users/vlsi5015/Desk
Arith_HW1_FMA	C:/Users/vlsi5015/Desk
Wu_CNN	C:/Users/vlsi5015/Desk
Block_Dist_ramtest	C:/Users/vlsi5015/Desk
test	C:/Users/vlsi5015/Desk
AXI_DMA_test	C:/Users/vlsi5015/Desk
simple_dma	C:/Users/vlsi5015/Dow
winograd	C:/Users/vlsi5015/Desk
winograd_conv	C:/Users/vlsi5015/Desk

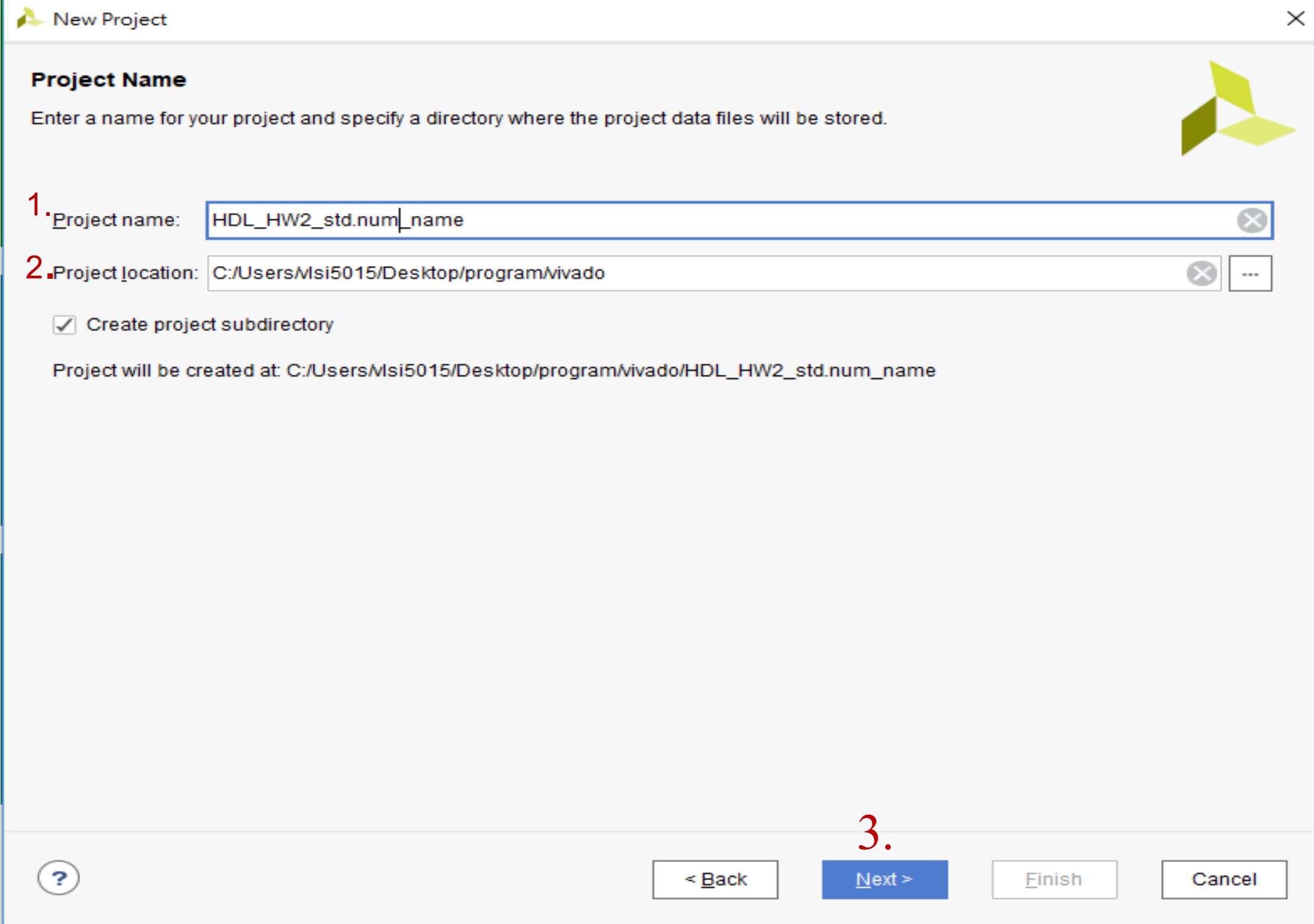
**Tasks**

- Manage IP >
- Open Hardware Manager >
- Xilinx Tcl Store >

**Learning Center**

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

# Create Project (2/8)



The image shows a 'New Project' dialog box from a software application. The dialog has a title bar with a small icon and the text 'New Project'. Inside, there's a section titled 'Project Name' with a description: 'Enter a name for your project and specify a directory where the project data files will be stored.' To the right of this text is a large Vivado logo. Below the description, there are two numbered steps: 1. 'Project name:' with a text input field containing 'HDL\_HW2\_std.num\_name'. 2. 'Project location:' with a text input field containing 'C:/Users/Msi5015/Desktop/program/vivado'. Below these fields, there is a checkbox labeled 'Create project subdirectory' which is checked. Underneath the checkbox, it says 'Project will be created at: C:/Users/Msi5015/Desktop/program/vivado/HDL\_HW2\_std.num\_name'. At the bottom of the dialog, there are four buttons: a help button (question mark in a circle), '< Back', 'Next >' (highlighted in blue), and 'Cancel'.

**New Project**

**Project Name**  
Enter a name for your project and specify a directory where the project data files will be stored.

1. Project name: HDL\_HW2\_std.num\_name

2. Project location: C:/Users/Msi5015/Desktop/program/vivado

☒ Create project subdirectory

Project will be created at: C:/Users/Msi5015/Desktop/program/vivado/HDL\_HW2\_std.num\_name

? < Back Next > Finish Cancel

# Create Project (3/8)

**New Project**

**Project Type**  
Specify the type of project to create.

1. ☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

2. ☒ **Do not specify sources at this time**

☐ **Post-synthesis Project**: You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ **Do not specify sources at this time**

☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**  
Create a new Vivado project from a predefined template.

3. **Next >**

**< Back** **Next >** **Finish** **Cancel**

We add source codes later  
or you can add now by unselecting this option.





# Create Project (4/8)

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards

1.


Filter/ Preview

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters


Search: 

Display Name

Vendor


Board Rev


Part

 Kintex-Ultrascale Alphadata board

alpha-data.com


1.0


 xcku060-ffva1156-2-e

 ZedBoard Zynq Evaluation and Development Kit

em.avnet.com


d

 xc7z020clg484-1

 Kintex UltraScale KCU1500 Acceleration Development Board

xilinx.com

1.0

 xcku115-flvb2104-2-e

No Board Connectors

?



< Back

3. Next >



Finish

Cancel

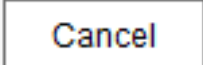
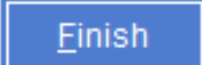
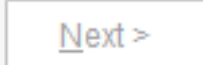
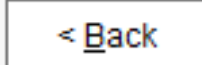

# Create Project (5/8)



## New Project Summary

-  A new RTL project named 'HDL\_HW2\_std.num\_name' will be created.
-  The default part and product family for the new project:
  - Default Board: ZedBoard Zynq Evaluation and Development Kit
  - Default Part: xc7z020clg484-1
  - Product: Zynq-7000
  - Family: Zynq-7000
  - Package: clg484
  - Speed Grade: -1

To create the project, click Finish



1.



# Create Project (6/8)

The screenshot displays the Xilinx Vivado Project Manager interface for a project named 'tutorial'. The left sidebar shows the project hierarchy with 'Add Sources' highlighted under the 'PROJECT MANAGER' section. The main workspace is divided into three panes: 'Sources', 'Properties', and 'Project Summary'.

**Sources Pane:** Shows the project structure with 'Design Sources', 'Constraints', and 'Simulation Sources' (containing 'sim\_1').

**Properties Pane:** Currently empty, displaying the message 'Select an object to see properties'.

**Project Summary Pane:** Contains project settings and board information.

**Project Summary Settings:**

- Project name: tutorial
- Project location: C:/Users/Msi5015/Desktop/program/vivado/tutorial
- Product family: Zynq-7000
- Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)
- Top module name: Not defined
- Target language: Verilog
- Simulator language: Mixed

**Board Part:**

- Display name: ZedBoard Zynq Evaluation and Development Kit
- Board part name: em.avnet.com.zed:part0:1.3
- Connectors:
- Repository path: C:/Xilinx/Vivado/2017.4/data/boards/board\_files
- URL: <http://www.zedboard.org>
- Board overview: ZedBoard Zynq Evaluation and Development Kit


**Synthesis and Implementation Status:**


Synthesis														Implementation				
Status:	Not started														Status:			
Messages:	No errors or warnings														Messages:			

**Design Runs Table:**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synth
impl_1	constrs_1	Not started															Vivado Imple

# Create Project (7/8)

  
**VIVADO**  
HLx Editions

  
**XILINX**  
ALL PROGRAMMABLE

**Add Sources**

This guides you through the process of adding and creating sources for your project

☐ Add or create constraints


☒ Add or create design sources

☐ Add or create simulation sources

Constraint

Source code

Testbench



< Back

Next >

Finish

Cancel

1.



2.

# Create Project (8/8)

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

	Index	Name	Library	Location
	1	MAD.v	xil_defaultlib	<Local to Project>
	2	MAD_Top.v	xil_defaultlib	<Local to Project>

1.

Add Files

Add Directories

Create File

☐ Scan and add RTL include files into project

☒ Copy sources into project

☒ Add sources from subdirectories

< Back

Next >

Finish

Cancel

27

# Outline

---

- 1. Download & Install**
- 2. Setup License**
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# Setting Constraint (1/5)

---

1. All you have to do is setting clock frequency, because the homework only asks you complete running implementation
2. There are two ways to set timing constraint
  - A. Create .xdc file and write constraint.
  - B. Use GUI

# Setting Constraint (2/5) (.xdc)

---

1. Create xdc file.

2. Write the below constraint to .xdc file.

```
create_clock -period 10.000 -name clk -waveform {0.000 5.000}  
[get_ports clk]
```

3. Explain :

- |                    |  |
|--------------------|--|
| 1. Create_clock    | : Create an independent clock source signal        |
| 2. {0.000 5.000}   | : posedge at 0.0ns, negedge at 5.0ns               |
| 3. [get_ports clk] | : Send clock signal to clk of Verilog's input port |

# Setting Constraint (3/5) (GUI)

1. You must run synthesis once after creating project.

2. **Edit Timing Constraints**

3. **Create Clock (0)**

4. **+**

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source Fil
Double click to create a Create Clock constraint							

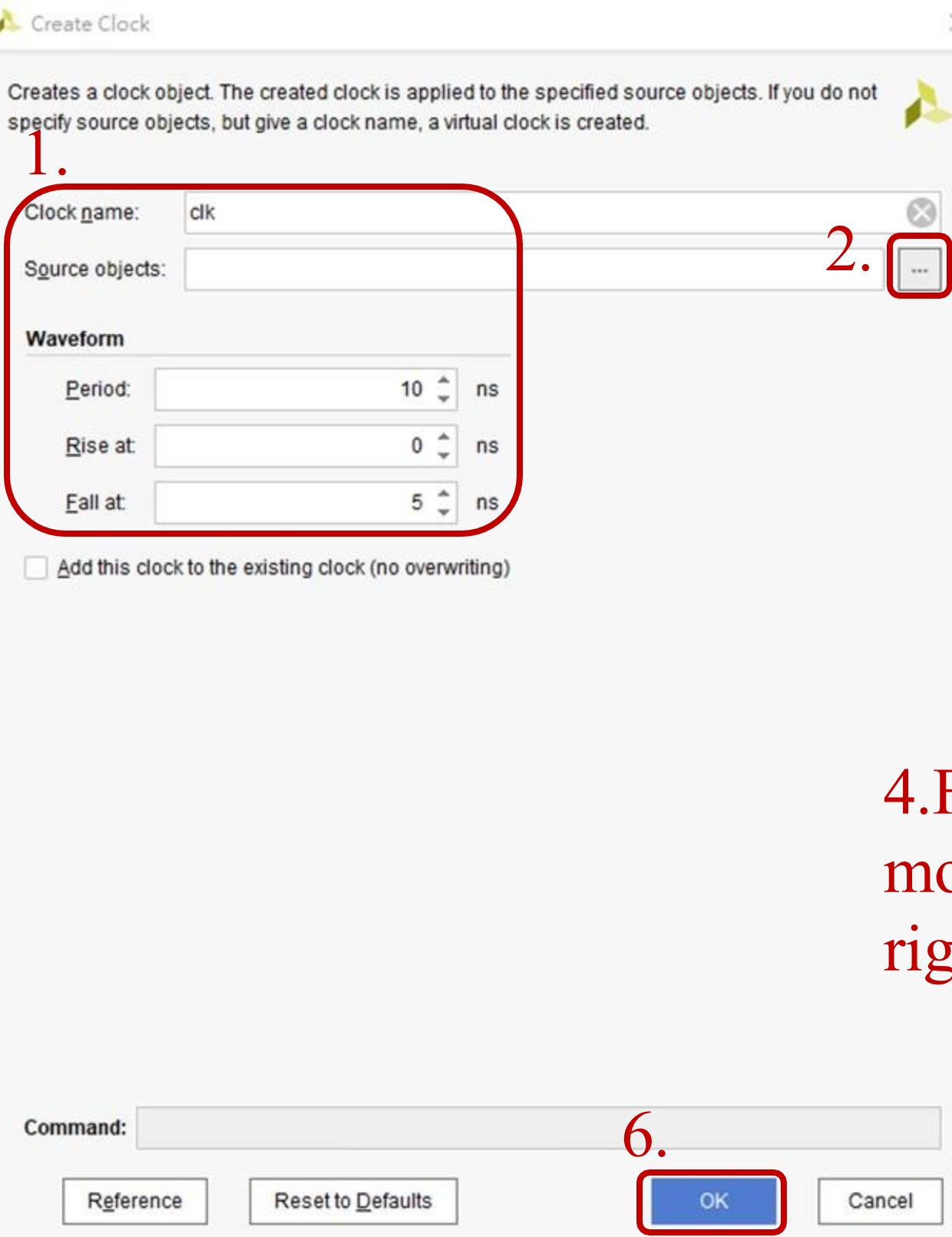
**All Constraints**

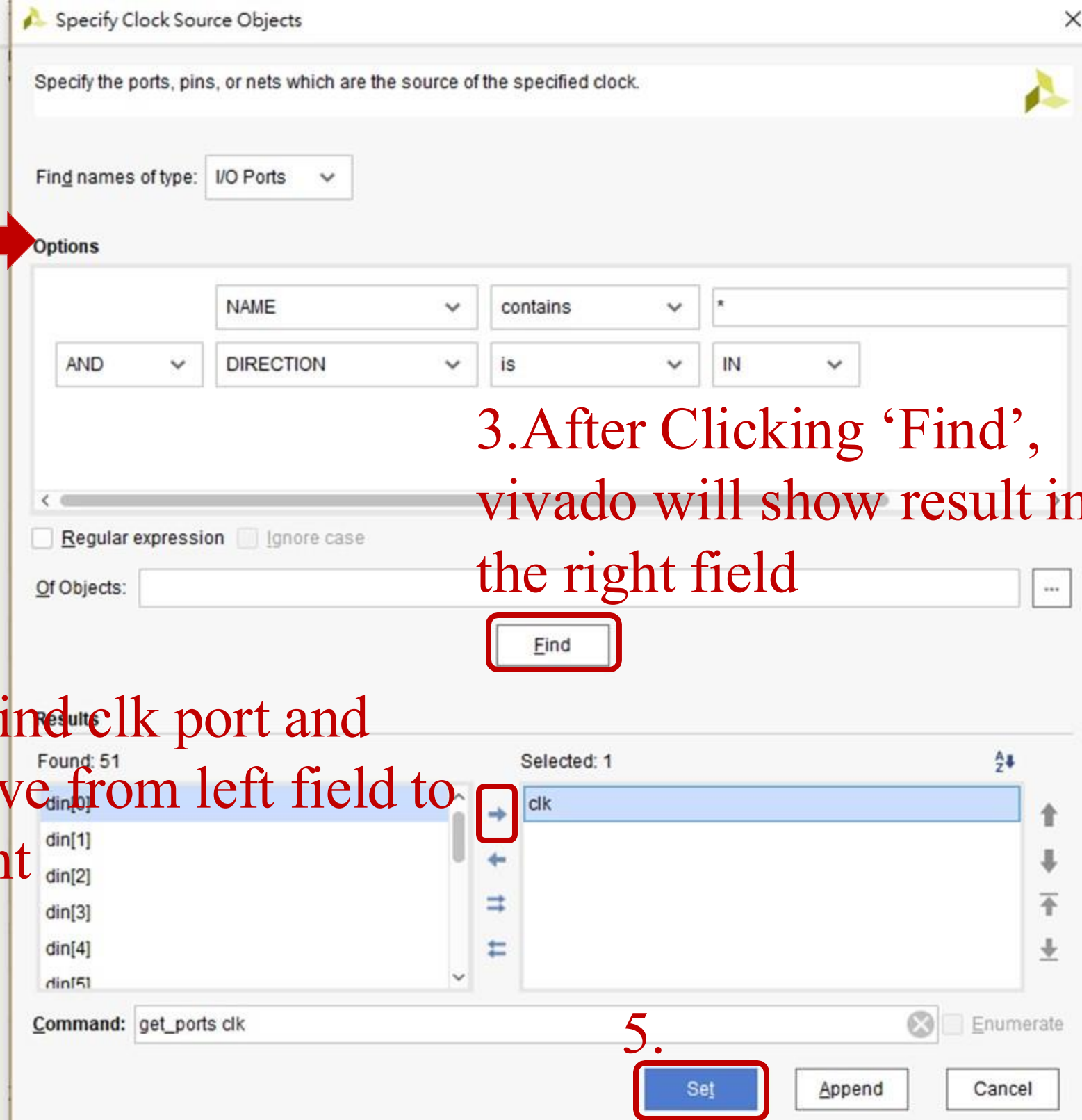
Position	Command	Scoped Cell
Constraints		

Apply Cancel



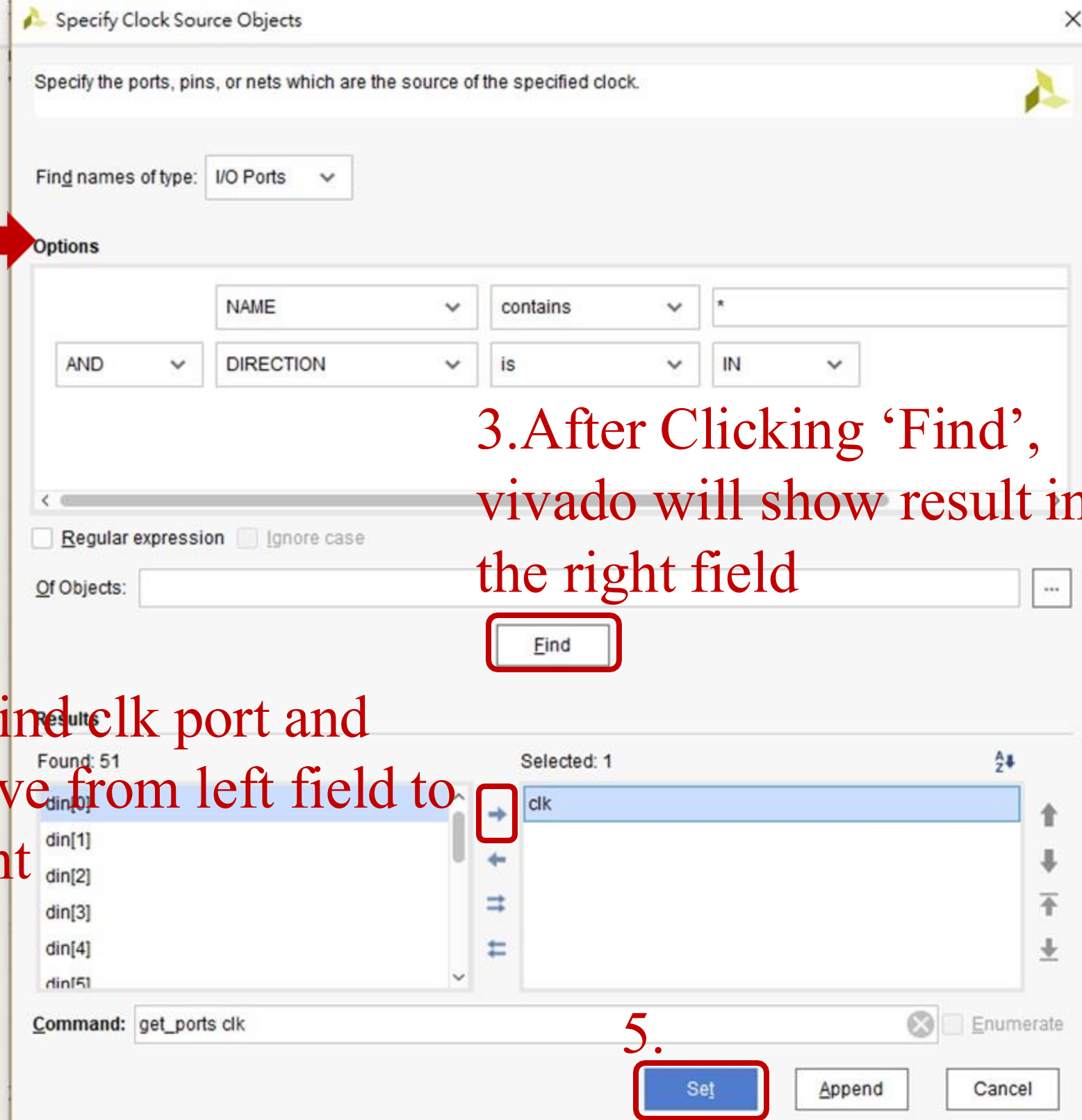
# Setting Constraint (4/5) (GUI)

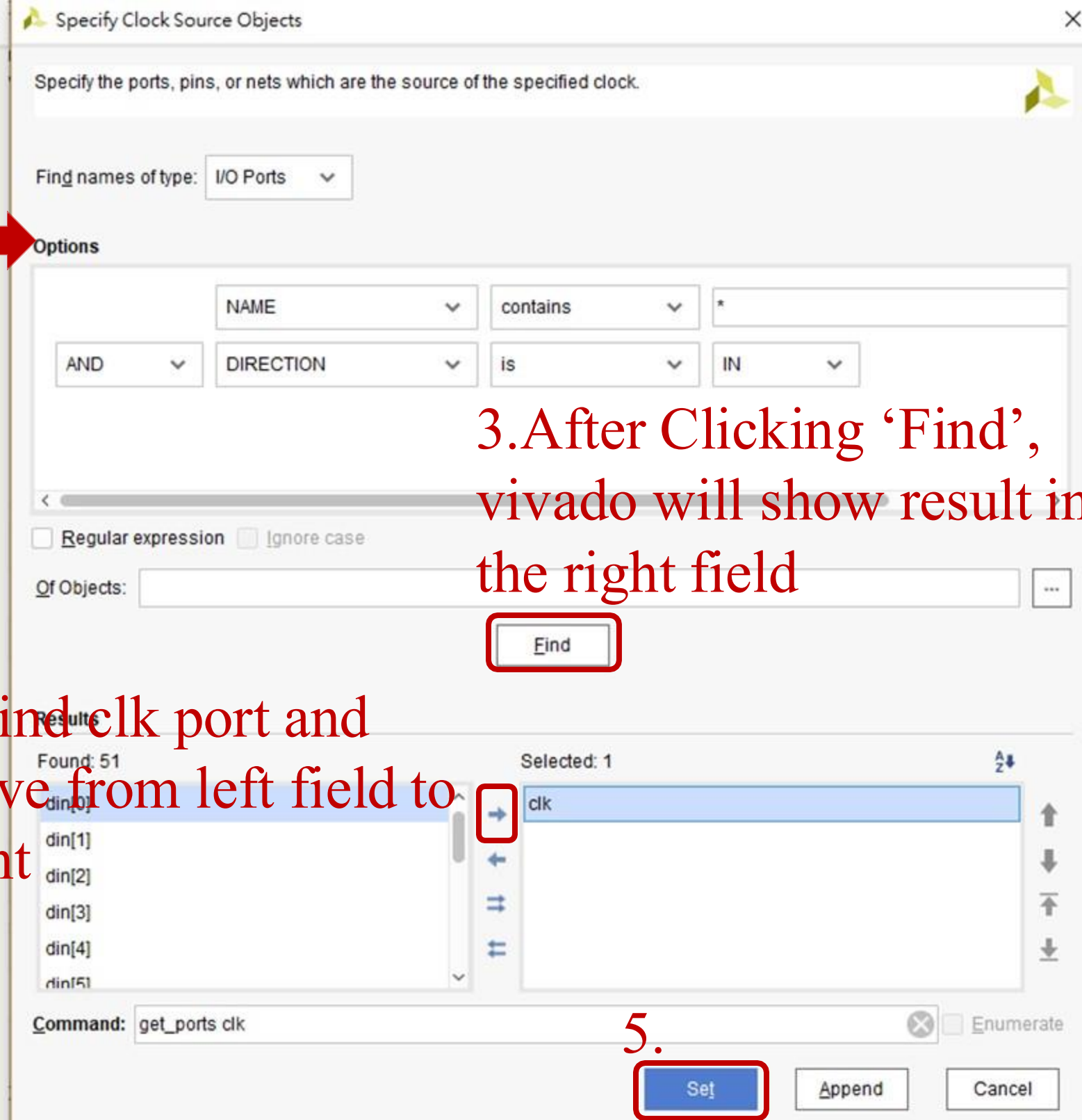
1. 

2. 

3. After Clicking 'Find', vivado will show result in the right field

4. Find clk port and move from left field to right

5. 

6. 



# Setting Constraint (5/5) (GUI)

The screenshot shows the 'Timing Constraints' window in the Xilinx ISE GUI. The 'Clocks (1)' section on the left lists various clock-related actions. The main table displays a single clock constraint for 'clk' with a period of 10.000 ns, rise time of 0.000 ns, and fall time of 5.000 ns. Below this, the 'All Constraints' section shows a list of constraints, with the first one highlighted and labeled '1.'. The 'Apply' button is highlighted and labeled '2.'.

**Timing Constraints Table:**

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File
2	clk	10.000	0.000	5.000	<input type="checkbox"/>	[get_ports clk]	<unsaved co...

*Double click to create a Create Clock constraint*

**All Constraints Table:**

Position	Command	Scoped Cell
Constraints	1.	
v <unsaved constraints>		
2	create_clock -period 10.000 -name clk -waveform {0.000 5.000} [get_ports clk]	

**Buttons:** Apply, Cancel

3. Finally, you have to check the timing constraint written correctly in the .xdc file.

# Outline

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- 1. Download & Install**
- 2. Setup License**
- 3. Create Project**
- 4. Setting Constraint**
- 5. Xsim**
- 6. Synthesis & Implementation**
- 7. Summary**

# Xsim (1/7)

Flow Navigator

Settings

PROJECT MANAGER

- Settings 1.
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

Project Settings

- General
- Simulation 2.
- Elaboration
- Synthesis
- Implementation
- Bitstream
- IP

Tool Settings

- Project
- IP Defaults
- Source File
- Display
- WebTalk
- Help
- Text Editor
- 3rd Party Simulators
- Colors
- Selection Rules
- Shortcuts
- Strategies
- Window Behavior

Simulation

Specify various settings associated to Simulation

Target simulator: Vivado Simulator

Simulator language: Mixed

Simulation set: sim\_1

Simulation top module name: men\_TB

3.

Compilation Elaboration Simulation Netlist Advanced

4.

Enter -all

xsim.simulate.tcl.post	
xsim.simulate.runtime*	-all
xsim.simulate.log_all_signals	<input type="checkbox"/>
xsim.simulate.custom_tcl	
xsim.simulate.wdb	
xsim.simulate.saif_scope	
xsim.simulate.saif	
xsim.simulate.saif_all_signals	<input type="checkbox"/>
xsim.simulate.xsim.more_options	

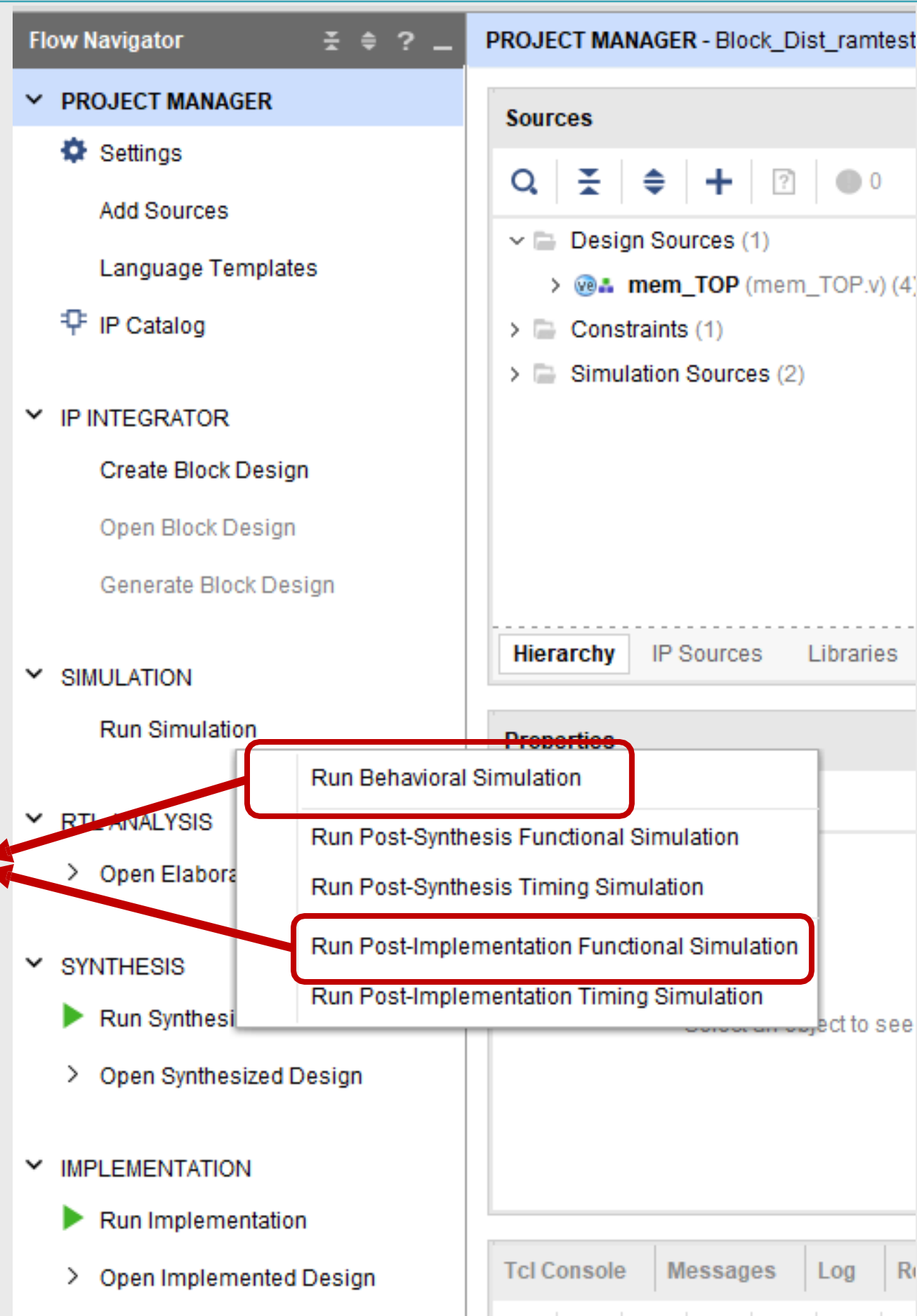
Select an option above to see a description of it

5.

OK Cancel Apply Restore...

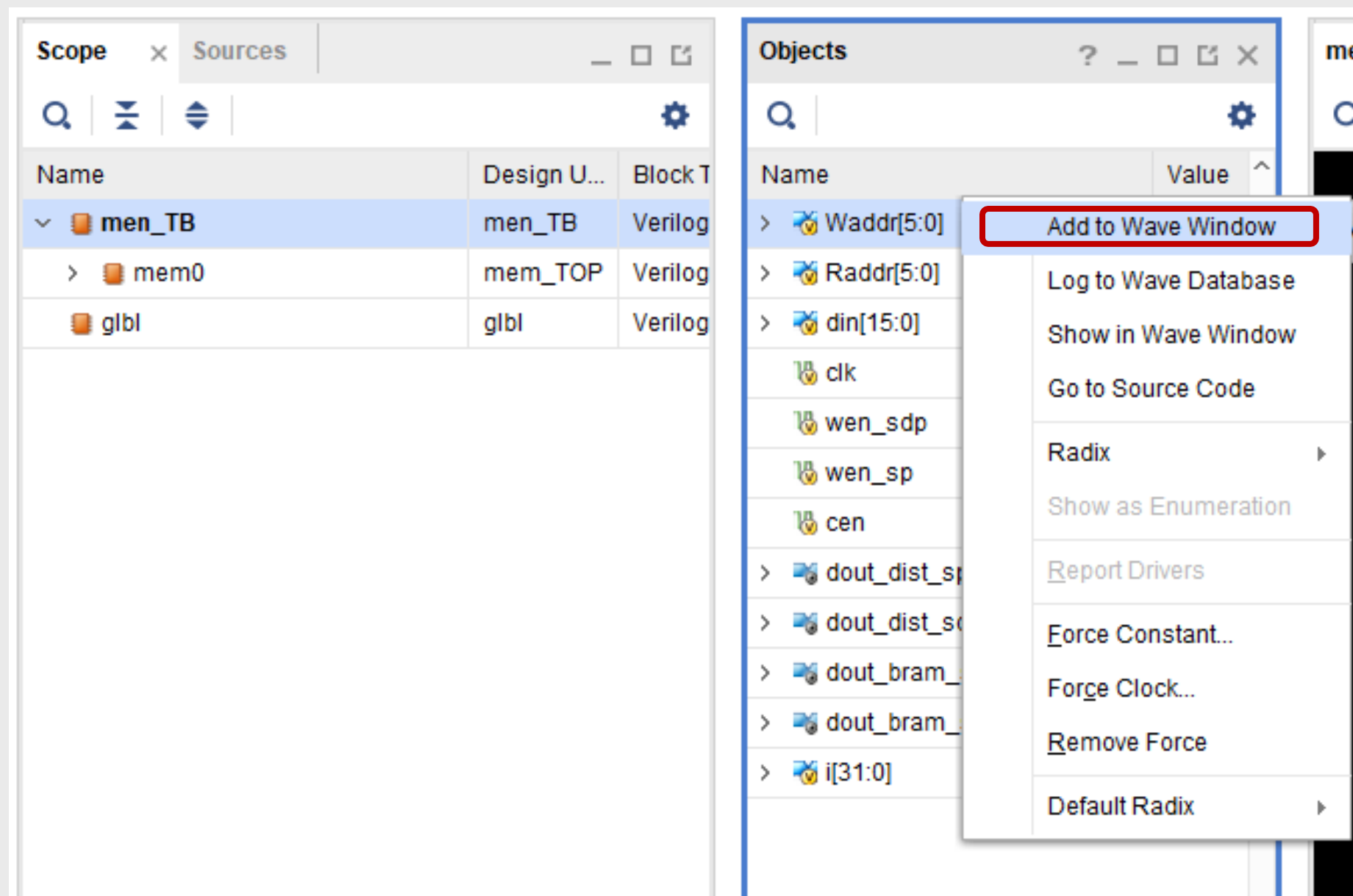
# Xsim (2/7)

We mainly use  
these two  
Simulation



# Xsim (3/7)

- You can add some signals which you want to observe.



# Xsim (4/7)

• There are three ways to help you observe waveform efficiently.

## 1. New Group :

Fold several signals into one row.

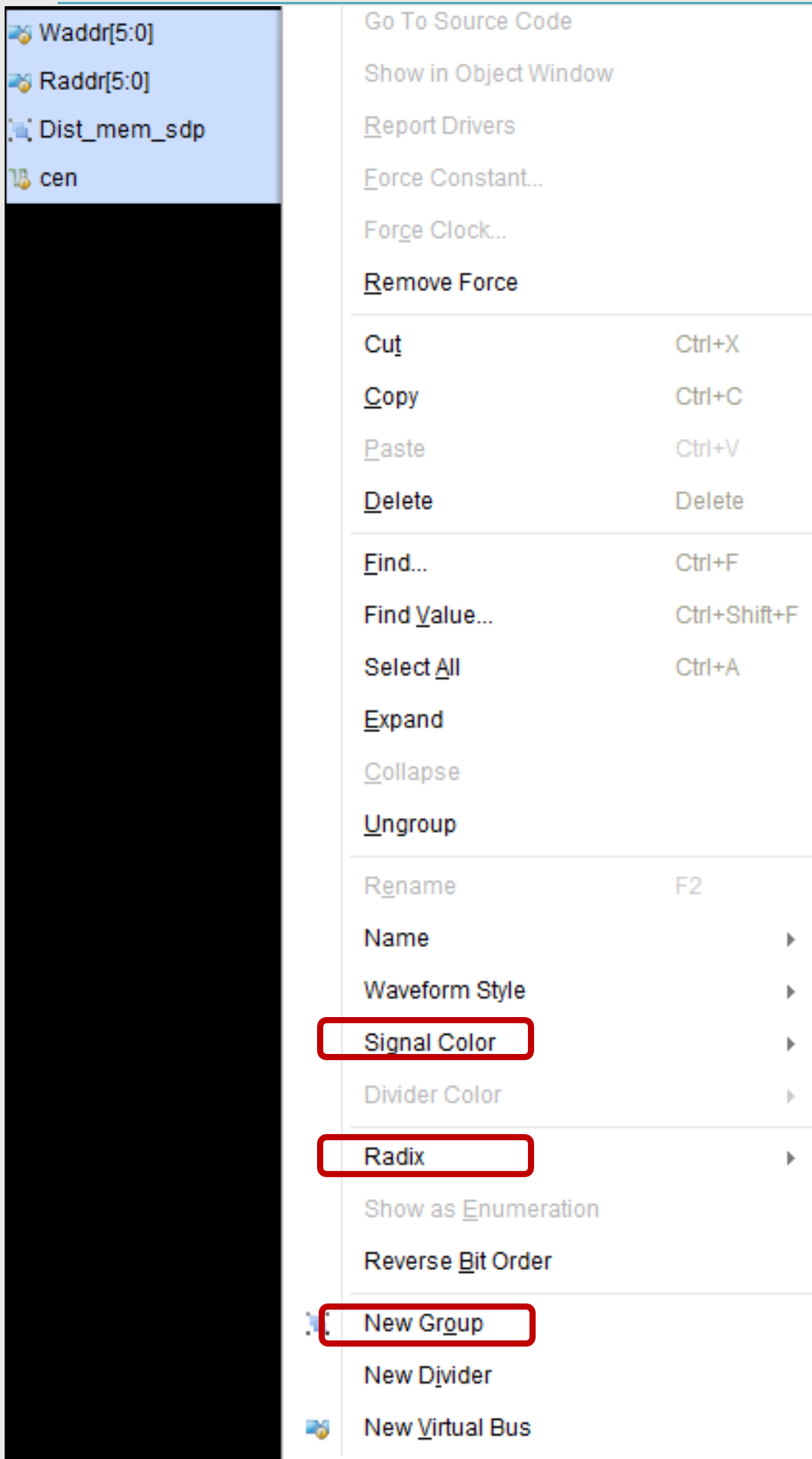
## 2. Signal Color

: Change

color

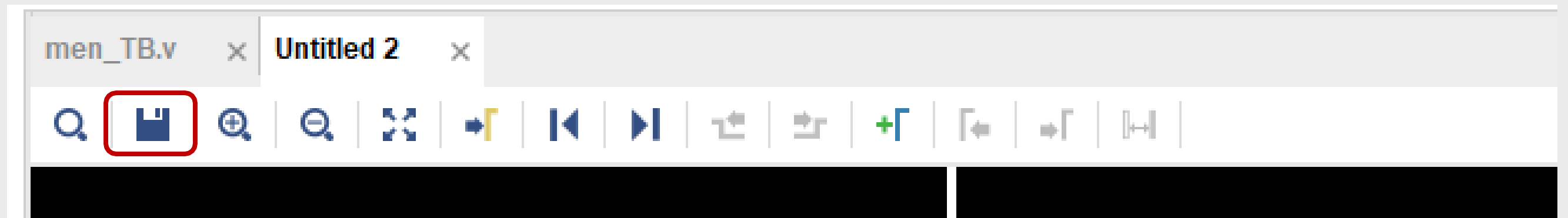
## 3. Radix :

1. Dec, Hex, etc.



# Xsim (5/5)

- After you arranged the signals in waveform, you can ‘Save Waveform Configuration’ (.wcfg)



# Outline

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# Synthesis & Implementation (1/3)

## IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

## SIMULATION

Run Simulation

## RTL ANALYSIS

> Open Elaborated Design

## SYNTHESIS

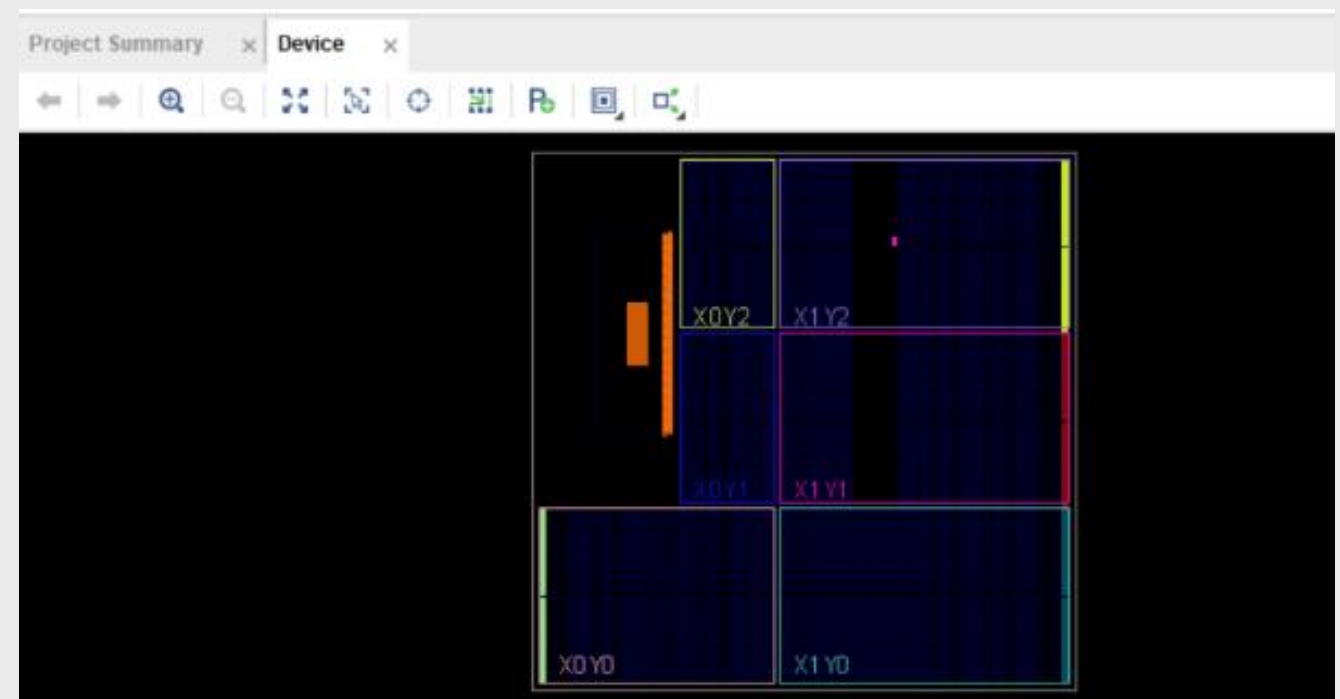
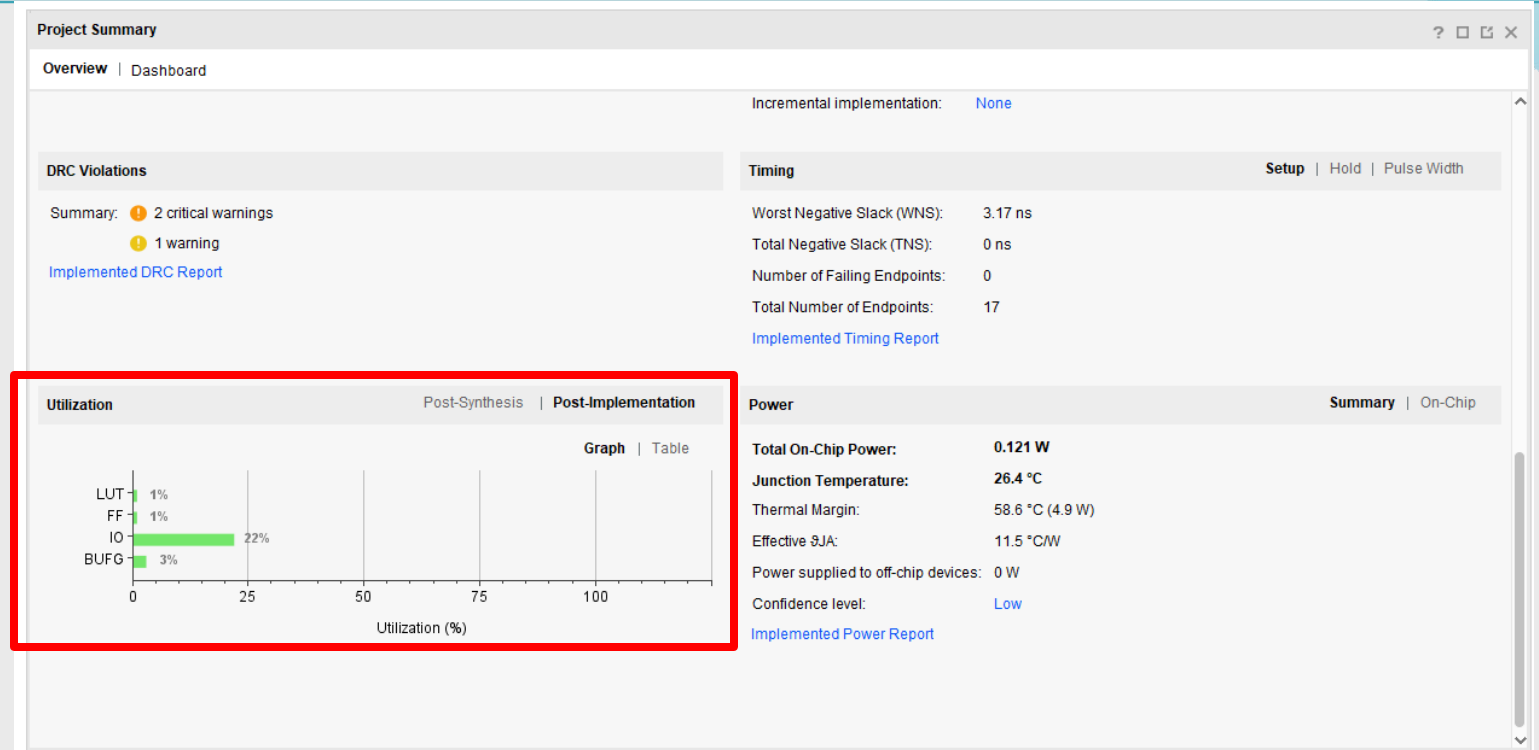
▶ Run Synthesis

> Open Synthesized Design

## IMPLEMENTATION

▶ Run Implementation

> Open Implemented Design



If you run implementation, vivado will ask you run synthesis first.

# Synthesis & Implementation (2/3)

- If all of the value is black font, this means the implementation is successful.

Tcl ConsoleMessagesLogReportsDesign Runs ×Timing

Q

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Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
▼ 🟢 synth_1 (active)	constrs_1	Synthesis Out-of-date								0	0	0.00	0	0
🟢 impl_1	constrs_1	Implementation Out-of-date	6.902	0.0...	0.037	0.0...	0.000	0.665	0	40	0	1.00	0	0

1. If implementation didn't success, it will show error part in red font
2. Please check if timing violation or area is exceeding the limit.

# Synthesis & Implementation (3/3)

---

- Resource :
  1. LUT : Look-up table  
Combinational circuit
  2. FF : Flip-Flop  
Register of sequential circuit
  3. BRAM/LUTRAM  
: Memory
  4. DSP : Digital signal processor  
Special arithmetic (multiplication, division, etc.)
  5. IO :  
Bit number of IO port.
  6. BUFG :  
Usually is used by clock source.

# Outline

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- 1. Download & Install**
- 2. Setup License**
- 3. Create Project**
- 4. Setting Constraint**
- 5. Xsim**
- 6. Synthesis & Implementation**
- 7. Summary**

# Summary (1/3)

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- FPGA Design Flow :

1. Write Verilog
2. Behavior Simulation
3. Setting Constraint
4. Synthesis
5. Implementation
6. Post-Implementation Functional simulation

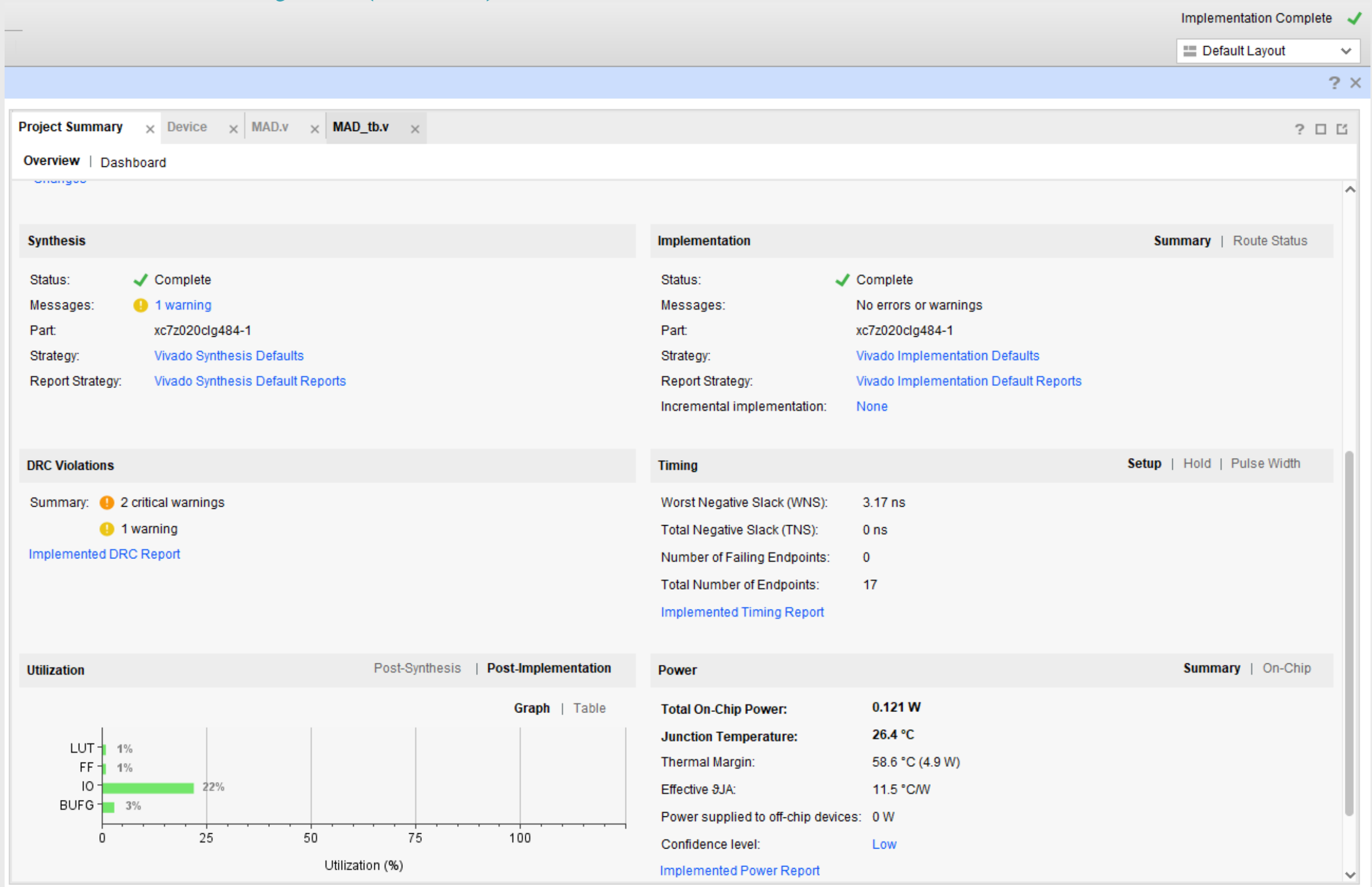
# Summary (2/3)

---

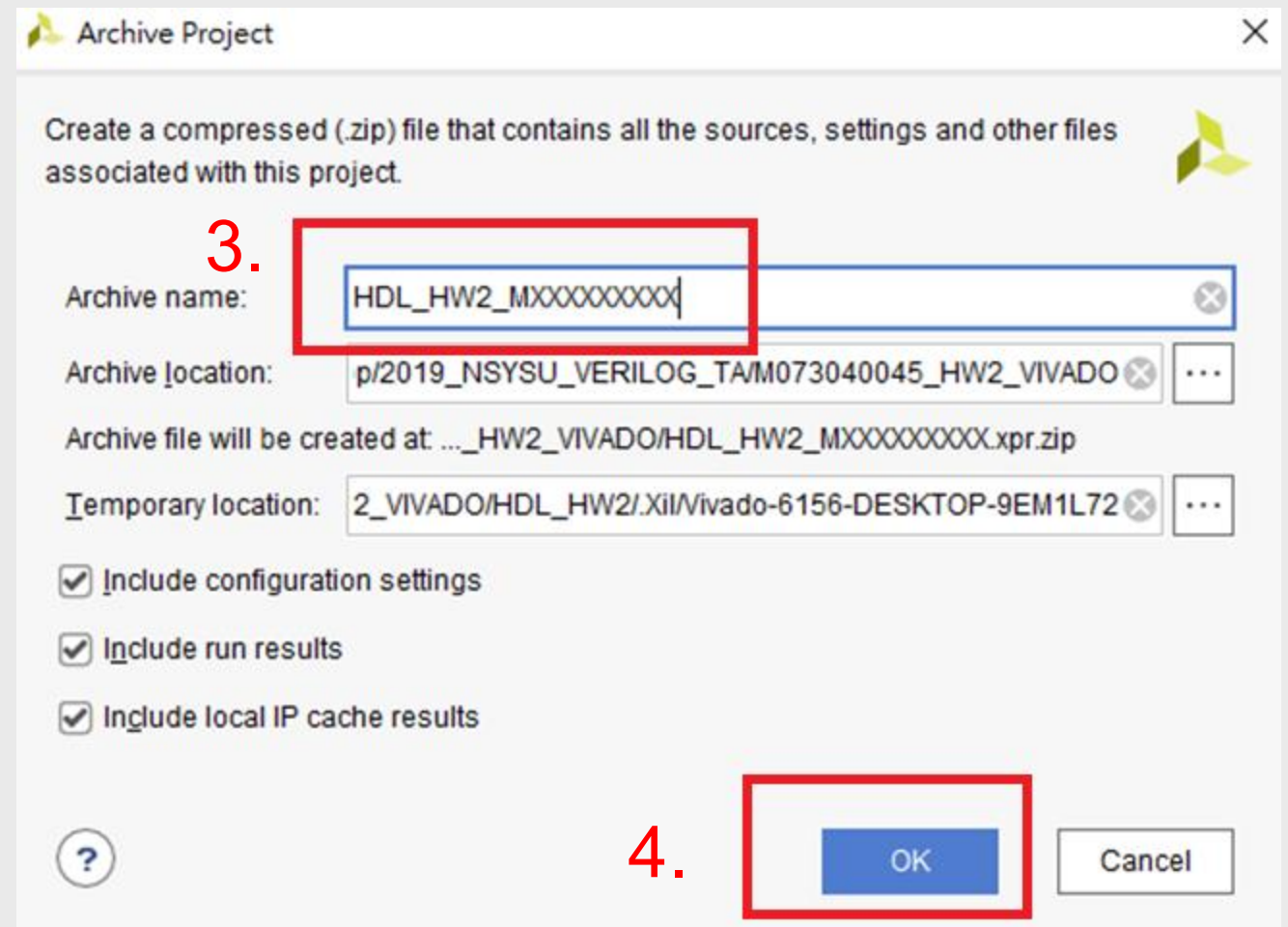
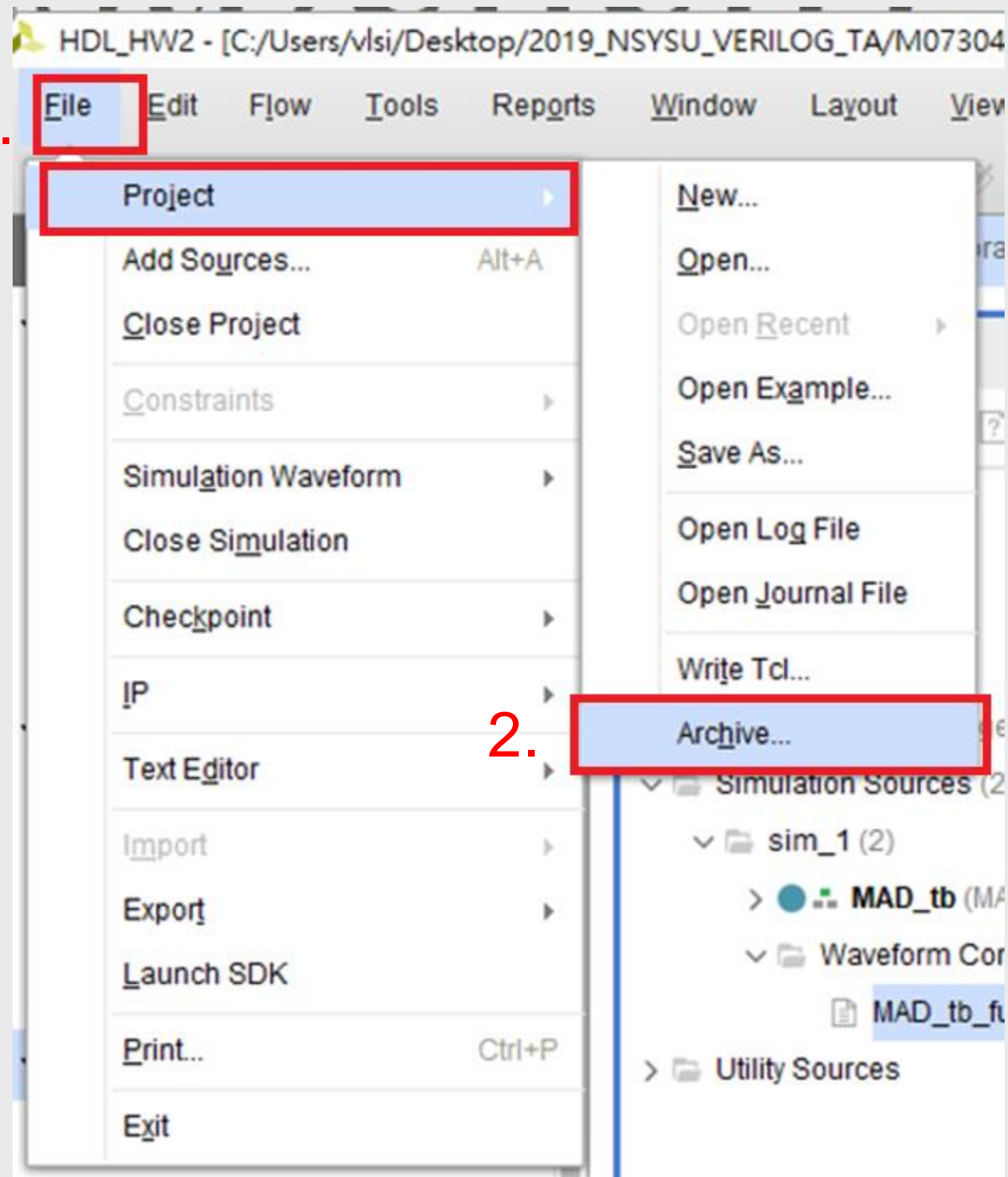
## 2. Design requirement :

- **Clock frequency at 100MHz.**
- **No error and critical warning after running implementation.**
- **You have to check the warnings will not cause your design incorrect.**

# Summary (3/3)



# 匯出壓縮檔(.xpr.zip)



Project完成後，可如左圖流程直接產生壓縮檔。

- 請將檔名修改成 **HDL\_HW4\_學號**
- 再把整個資料夾放入 **Server** 內 **HW4** 資料夾
- 繳交整個 **HW4** 資料夾到 **Homework-Submit**