

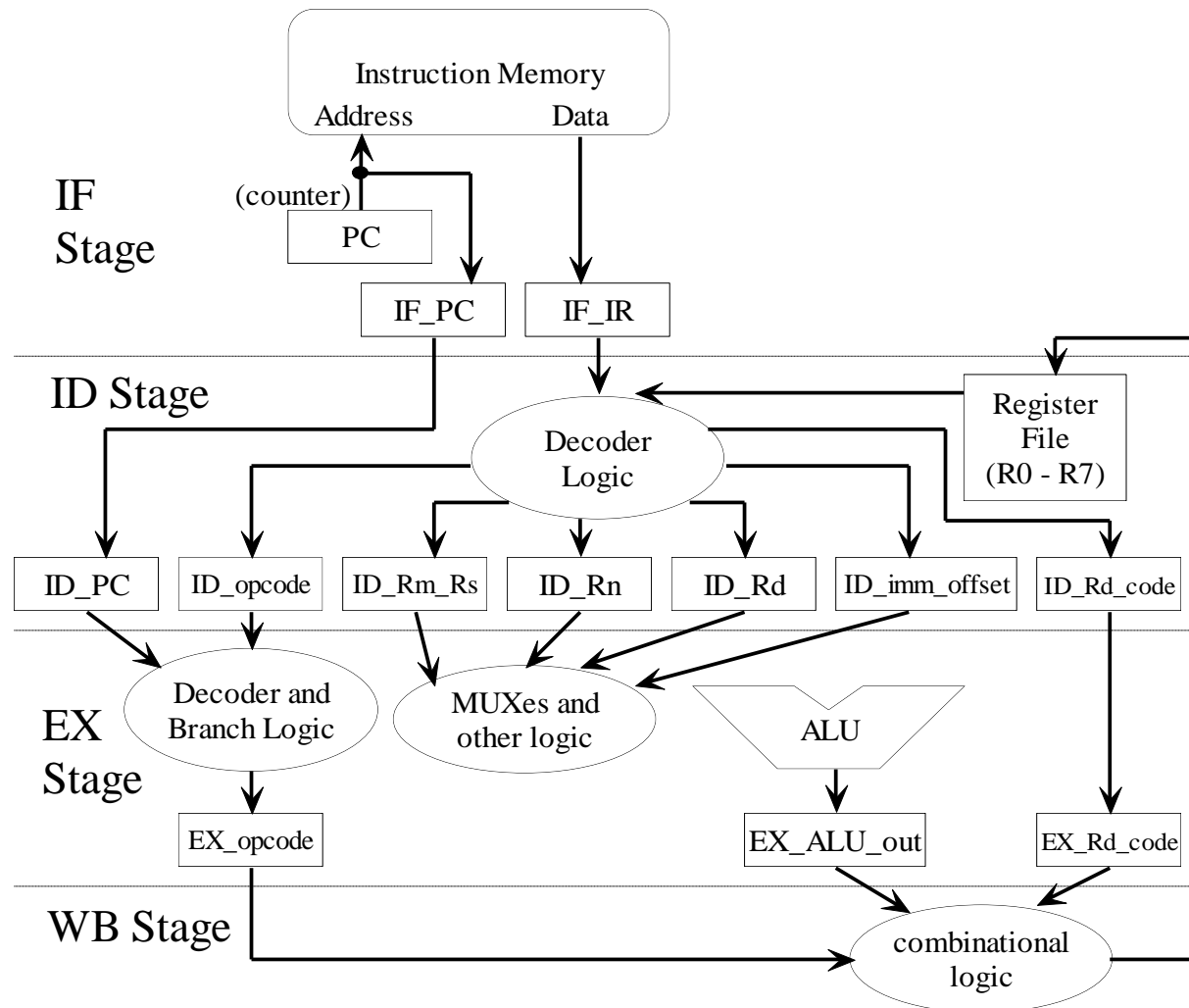
HDL HW3: Pipelined THUMB CPU and Placement and Routing (P&R)

Outlines

- debug the THUMB RSIC CPU code
 - reset some signals
- synthesize THUMB
 - find critical path of each pipelined stage
- use prime time to measure power
- perform automatic placement-and-routing (APR) and mark the four pipelined stages in the layout view

THUMB Architecture

- 4 pipelined stages: IF, ID, EX, WB
 - refer to lecture 05 slides and given codes



One Pipelined Stage Per Module

- debug the given pipelined THUMB codes
 - both RTL codes and testbench are given
- modify the codes so that each pipelined stage is in a separate module
 - easy identification of critical path of each stage
- synthesize with three different constraints
 - area-optimized
 - delay-optimized
 - in-between
- find the delay of each pipelined stage
 - from Synopsys DC synthesis report
- measure delay and power using PrimeTime

summary table

- area, delay (each stage, and critical), power (DC, PT)
 - power from Design Compiler (DC) synthesis report, or
 - power measured using PrimeTime (PT)
 - critical path delay measured by DC and by PT

constraint	area	delay (DC)					power	
		1 st	2 nd	3 rd	4 th	Critical	DC	PT
Delay-opt						DC(PT)		
Area-opt								
In-between								

Placement and Routing

- perform automatic placement and routing (APR)
- mark the four pipelined stages in the layout view

