Prime time

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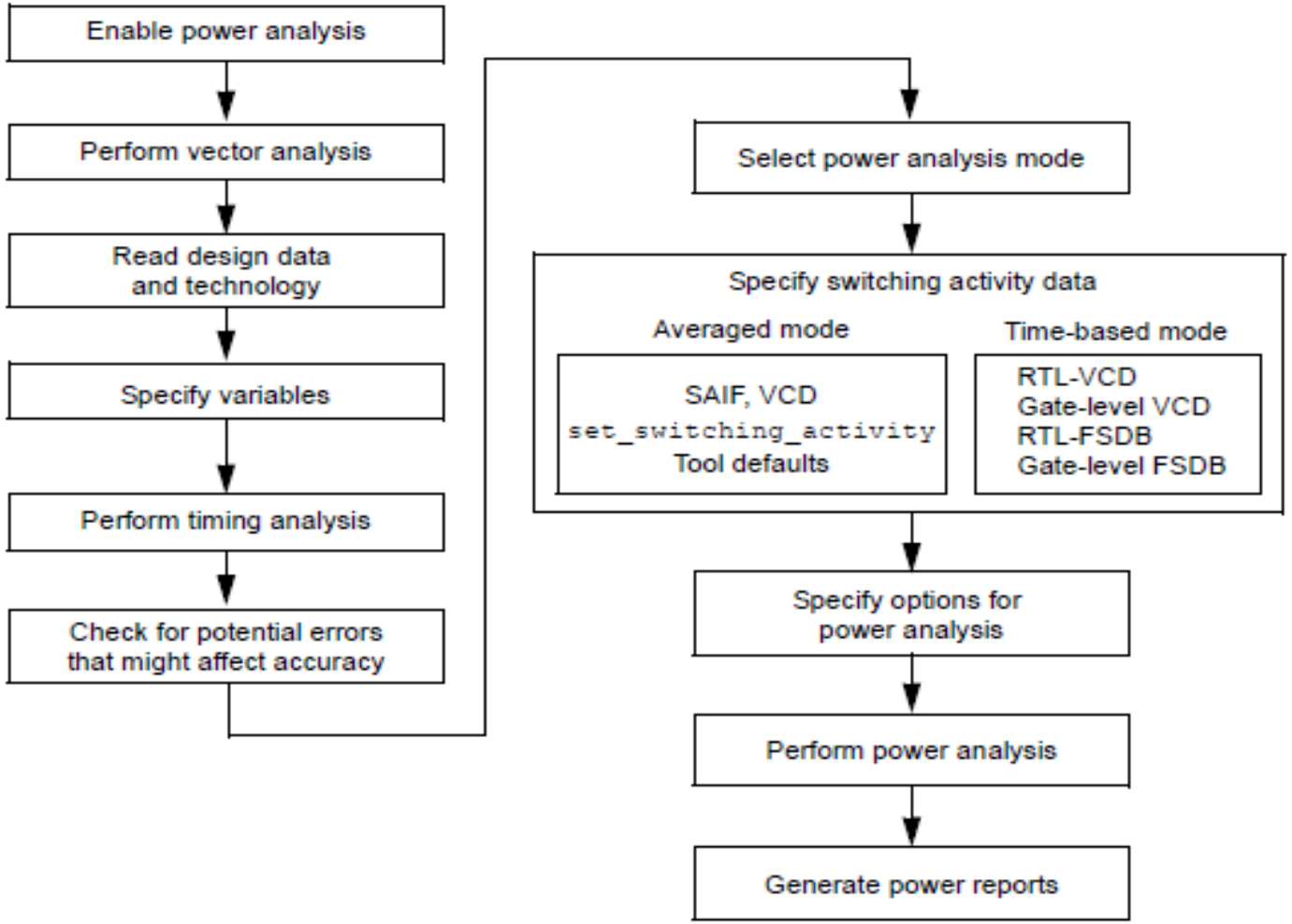
OUTLINE

01 Analysis format

02 Manual

Analysis format

Power Analysis Flow - Primetime PX



Analysis format

Simulation Activity Formats

- SAIF (Switching Activity Interchange Format)
  - T0 - duration of time found in logic 0 state.
  - T1 - duration of time found in logic 1 state.
  - TX - duration of time found in unknown “X” state
  - TC - sum of the rise (0-to-1) and fall (1-to-0) transitions that are captured during monitoring
  - IG - number of 0 - X - 0 and 1 - X - 1 glitches captured during monitoring
  - RISE - Rise transitions in a given state.
  - FALL - Fall transitions in a given state.
  - Toggle Rate (Tr) = TC / duration
  - Glitch Rate (Gr) = derate_glitch * IG
    - derate_glitch 0.5 (default)
- Wave file
  - **VCD** (Value Change Dump) → Prime time
  - FSDB(Fast Signal Data Base) → Verdi

Analysis format

Average Power Analysis

- Average Power analysis applications
  - Packaging selection
- The switching activity consists of toggle rates and static probabilities in average power analysis
  - Toggle Rate (Tr) for dynamic power
    - P(switching) = 0.5 * Cload * vdd^2 * Tr
    - P(internal) = $Energy_{int}$ * Tr
    - power_default_toggle_rate 0.1 (default)
  - Static Probability (Sp) for leakage power
    - Probability of logic 1 for a node
    - P(leak) = (Pleak0 * 1-Sp) + (Pleak1 * Sp)
    - power_default_static_probability 0.5 (default)
- Default toggle will be applied to the propagation starting point
  - primary inputs
  - black box outputs

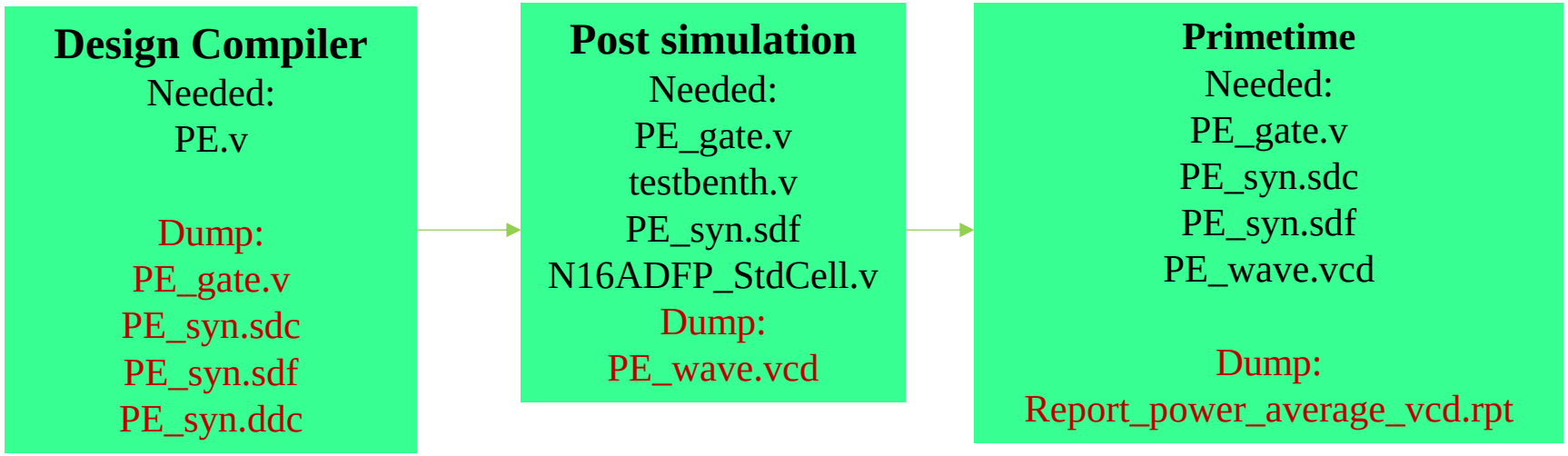
Analysis format

Time-Based Power Analysis

- Peak Power analysis application
  - IR drop analysis
- Peak power analysis types
  - Cycle accurate Peak power analysis
  - Event based Peak power analysis

manual

Primetime manual



manual

Design Compiler

Please have a look at the **Design Compiler.pptx**

- verilog (gate level netlist)
- ddc (save your design)
- sdc (Synopsys Design Constraints)
- sdf (Standard Delay Format)

PE_gate.v


PE_syn.ddc


PE_syn.sdc

PE_syn.sdf

manual

Post-synthesis simulation method 1


PE_gate.v


PE_syn.sdf


tb_datapath.v

- Testbenth

```
initial begin
        $dumpvars();
        $dumpfile("clockgating_wave.vcd");

        $sdf_annotate ("/home/m123040031/HDL_homework/HDL_HW2_M123040031/SYN/clock_gating/DC/clockgating_delay_syn.sdf", test);
end

clockgating test (.a (input_a), .b (input_b), .c (input_c), .s (input_s), .clk (clk), .rst (rst), .d (outcome_d));
```

- Use vcs to dump the file

1. tcsh
2. source post_sim.sh

```
1   #!/bin/tcsh
2
3   vcs -R -error=noMPD \
4   /home/m123040033/HDL/post_sim/TB.v \
5   /home/m123040033/HDL/behavior/adder_behavior.v \
6   /home/m123040033/HDL/behavior_reg/adder_behavior_reg.v \
7   /home/m123040033/HDL/dataflow/adder_dataflow.v \
8   /home/m123040033/HDL/dataflow_reg/adder_dataflow_reg.v \
9   /home/m123040033/HDL/structure/adder_structure.v \
10  /home/m123040033/HDL/structure_reg/adder_structure_reg.v \
11  /cad/CBDK/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/VERILOG/N16ADFP_StdCell.v \
12  +full64 \
13  +access+r +vcs+fsdbon +fsdb+mda +fsdbfile+6adder.fsdb +neg_tchk
```

testbench

Gate Level Netlist

Standard Cell

Output Waveform

建議使用絕對路徑

manual

Primetime

- 因為post_sim跑完生成的是 .fsdb檔案，但Primetime吃的是 .vcd檔，所以需要做轉檔的動作

- Fsdb轉vcd檔指令

  fsdb2vcd example.fsdb -o example.vcd

PE_wave.vcd

manual

Primetime

- verilog (gate level netlist)
- sdc (Synopsys Design Constraints)
- sdf (Standard Delay Format)
- vcd(wave file)

- Use Primetime
- pt_shell -f pt.tcl

manual

pt.tcl

```
module tb_datapath();
        reg [7:0]  in1,in2;
        wire [15:0] out;
        reg rst,clk,sel;
        reg [7:0] r1,r2;
        integer i;
        PE PE(.out(out),.in1(
```

pt.tcl

```
# source saifmap.ptpx.tcl
# report_name_mapping
set power_enable_analysis true
set power_analysis_mode averaged
set power_report_leakage_breakdowns true

read_verilog /home/m1230400xx/HDL/HW2/syn/gate_level_sim/PE_gate.v
current_design PE
link

read_sdc /home/m1230400xx/HDL/HW2/syn/gate_level_sim/PE_syn.sdc
read_sdf /home/m1230400xx/HDL/HW2/syn/gate_level_sim/PE_syn.sdf

check_timing
update_timing

read_vcd -strip_path tb_datapath/PE /home/m1230400xx/HDL/HW2/syn/gate_level_sim/PE_wave.vcd

check_power
update_power
report_power -hierarchy > report_power_average_vcd_hw2_gclk.rpt
```

gate level netlist

Your design module name

Testbench module name/ Your design instance name

*此圖只是對應ppt的操作範例，檔案路徑及名稱請根據自己命名與路徑或作業要求進行修改。

manual

Power average

(此範例與HW2不同)

Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
top	6.08e-04	4.38e-04	2.28e-04	1.27e-03	100.0
a1_h (adder_2)	2.65e-05	6.40e-05	1.63e-05	1.07e-04	8.4
r328 (adder_2_DW01_add_0)	5.93e-06	5.53e-06	2.38e-06	1.38e-05	1.1
r329 (adder_2_DW01_sub_0)	6.53e-06	6.60e-06	2.89e-06	1.60e-05	1.3
r330 (adder_2_DW_cmp_0)	5.26e-07	2.83e-06	4.73e-07	3.82e-06	0.3
a2_h (adder_1)	4.82e-06	5.34e-06	2.81e-06	1.30e-05	1.0
r328 (adder_1_DW01_add_0)	4.36e-06	3.02e-06	2.14e-06	9.52e-06	0.7
r329 (adder_1_DW01_sub_0)	5.93e-06	5.53e-06	2.38e-06	1.38e-05	1.1
r330 (adder_1_DW_cmp_0)	4.36e-06	3.02e-06	2.14e-06	9.52e-06	0.7
a3_h (adder1_1)	9.66e-07	2.78e-08	5.16e-08	1.05e-06	0.1
r328 (adder1_1_DW01_add_0)	4.82e-06	5.34e-06	2.81e-06	1.30e-05	1.0
r329 (adder1_1_DW01_sub_0)	4.36e-06	3.02e-06	2.14e-06	9.52e-06	0.7
r330 (adder1_1_DW_cmp_0)	6.87e-06	6.51e-06	2.12e-06	1.55e-05	1.2
p0 (pipeline0_1)	1.32e-04	1.50e-05	6.91e-06	1.54e-04	12.1
p2_1_h (pipeline2_1)	3.11e-05	9.22e-07	2.14e-06	3.42e-05	2.7
p1 (pipeline1_0)	2.98e-05	3.30e-06	1.65e-06	3.48e-05	2.7
p2 (pipeline1_7)	3.02e-05	2.96e-06	1.61e-06	3.48e-05	2.7
p3 (pipeline1_6)	2.97e-05	3.01e-06	1.57e-06	3.42e-05	2.7
p4 (pipeline1_5)	3.00e-05	3.61e-06	1.68e-06	3.53e-05	2.8
p_h (pipeline0_0)	3.37e-06	3.77e-06	7.96e-06	1.51e-05	1.2
clk_gate_C301 (SNPS_CLOCK_GATE_HIGH_top)					
	6.64e-07	0.000	4.91e-08	7.13e-07	0.1
p2_1 (pipeline2_0)	3.66e-05	4.67e-06	1.93e-06	4.32e-05	3.4
p0m (pipelinem_0)	9.66e-07	2.78e-08	5.16e-08	1.05e-06	0.1
n32 (normal32)	1.58e-06	6.57e-06	5.76e-06	1.39e-05	1.1
add_32 (normal32_DW01_add_2)	0.000	0.000	1.42e-06	1.42e-06	0.1
a1 (adder_0)	2.65e-05	6.40e-05	1.63e-05	1.07e-04	8.4
r328 (adder_0_DW01_add_0)	5.93e-06	5.53e-06	2.38e-06	1.38e-05	1.1
r329 (adder_0_DW01_sub_0)	6.53e-06	6.60e-06	2.89e-06	1.60e-05	1.3
r330 (adder_0_DW_cmp_0)	5.26e-07	2.83e-06	4.73e-07	3.82e-06	0.3
a2 (adder_3)	2.20e-05	5.78e-05	1.65e-05	9.63e-05	7.6
r328 (adder_3_DW01_add_0)	4.36e-06	3.02e-06	2.14e-06	9.52e-06	0.7
r329 (adder_3_DW01_sub_0)	4.82e-06	5.34e-06	2.81e-06	1.30e-05	1.0
r330 (adder_3_DW_cmp_0)	5.62e-07	3.06e-06	5.04e-07	4.13e-06	0.3
a3 (adder1_0)	5.37e-05	1.46e-04	1.72e-05	2.16e-04	17.0
r328 (adder1_0_DW01_add_0)	6.87e-06	6.51e-06	2.12e-06	1.55e-05	1.2
r329 (adder1_0_DW01_sub_0)	1.07e-05	1.18e-05	2.90e-06	2.54e-05	2.0
r330 (adder1_0_DW_cmp_0)	2.40e-06	1.20e-05	6.38e-07	1.50e-05	1.2
p1m (pipelinem_2)	9.66e-07	2.78e-08	5.16e-08	1.05e-06	0.1
p1_h (pipeline1_4)	2.67e-05	7.81e-07	1.76e-06	2.92e-05	2.3
p2_h (pipeline1_3)	2.69e-05	7.81e-07	1.81e-06	2.95e-05	2.3
p3_h (pipeline1_2)	2.66e-05	7.81e-07	1.73e-06	2.91e-05	2.3
m1_h (mul_4)	0.000	0.000	9.90e-06	9.90e-06	0.8
mult_28 (mul_4_DW_mult_uns_0)	0.000	0.000	9.31e-06	9.31e-06	0.7
p2m (pipelinem_1)	9.66e-07	2.78e-08	5.16e-08	1.05e-06	0.1
p4_h (pipeline1_1)	2.69e-05	7.81e-07	1.81e-06	2.95e-05	2.3
m2_h (mul_3)	0.000	0.000	9.90e-06	9.90e-06	0.8
mult_28 (mul_3_DW_mult_uns_0)	0.000	0.000	9.31e-06	9.31e-06	0.7

manual

Power average

with clock-gating

(此範例與HW2不同)

Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
top	5.21e-04	5.46e-05	2.17e-04	7.92e-04	100.0
a1_h (adder_2)	0.000	0.000	1.41e-05	1.41e-05	1.8
r328 (adder_2_DW01_add_0)	0.000	0.000	2.53e-06	2.53e-06	0.3
r329 (adder_2_DW01_sub_0)	0.000	0.000	2.97e-06	2.97e-06	0.4
r330 (adder_2_DW_cmp_0)	0.000	0.000	5.35e-07	5.35e-07	0.1
a2_h (adder_1)	0.000	0.000	1.51e-05	1.51e-05	1.9
r328 (adder_1_DW01_add_0)	0.000	0.000	2.12e-06	2.12e-06	0.3
r329 (adder_1_DW01_sub_0)	0.000	0.000	2.78e-06	2.78e-06	0.4
r330 (adder_1_DW_cmp_0)	0.000	0.000	5.35e-07	5.35e-07	0.1
a3_h (adder1_1)	0.000	0.000	1.52e-05	1.52e-05	1.9
r328 (adder1_1_DW01_add_0)	0.000	0.000	2.14e-06	2.14e-06	0.3
r329 (adder1_1_DW01_sub_0)	0.000	0.000	3.36e-06	3.36e-06	0.4
r330 (adder1_1_DW_cmp_0)	0.000	0.000	7.43e-07	7.43e-07	0.1
p0 (pipeline0_1)	1.22e-04	5.02e-06	6.34e-06	1.33e-04	16.8
p2_1_h (pipeline2_1)	3.01e-05	1.23e-06	1.76e-06	3.31e-05	4.2
p1 (pipeline1_0)	2.64e-05	1.04e-06	1.49e-06	2.89e-05	3.7
p2 (pipeline1_7)	2.62e-05	1.04e-06	1.48e-06	2.87e-05	3.6
p3 (pipeline1_6)	2.59e-05	1.04e-06	1.42e-06	2.84e-05	3.6
p4 (pipeline1_5)	2.66e-05	1.04e-06	1.53e-06	2.92e-05	3.7
p_h (pipeline0_0)	1.22e-04	5.02e-06	6.35e-06	1.33e-04	16.8
clk_gate_C301 (SNPS_CLOCK_GATE_HIGH_top)					
	9.44e-07	0.000	5.23e-08	9.96e-07	0.1
p2_1 (pipeline2_0)	3.03e-05	1.23e-06	1.76e-06	3.33e-05	4.2
p0m (pipelinem_0)	8.49e-07	3.70e-08	5.18e-08	9.38e-07	0.1
n32 (normal32)	3.01e-06	1.80e-05	5.81e-06	2.68e-05	3.4
add_32 (normal32_DW01_add_2)	4.49e-07	1.48e-06	1.43e-06	3.36e-06	0.4
a1 (adder_0)	0.000	0.000	1.53e-05	1.53e-05	1.9
r328 (adder_0_DW01_add_0)	0.000	0.000	2.30e-06	2.30e-06	0.3
r329 (adder_0_DW01_sub_0)	0.000	0.000	2.74e-06	2.74e-06	0.3
r330 (adder_0_DW_cmp_0)	0.000	0.000	5.27e-07	5.27e-07	0.1
a2 (adder_3)	0.000	0.000	1.58e-05	1.58e-05	2.0
r328 (adder_3_DW01_add_0)	0.000	0.000	2.08e-06	2.08e-06	0.3
r329 (adder_3_DW01_sub_0)	0.000	0.000	2.70e-06	2.70e-06	0.3
r330 (adder_3_DW_cmp_0)	0.000	0.000	5.27e-07	5.27e-07	0.1
a3 (adder1_0)	0.000	0.000	1.57e-05	1.57e-05	2.0
r328 (adder1_0_DW01_add_0)	0.000	0.000	2.07e-06	2.07e-06	0.3
r329 (adder1_0_DW01_sub_0)	0.000	0.000	2.77e-06	2.77e-06	0.4
r330 (adder1_0_DW_cmp_0)	0.000	0.000	7.36e-07	7.36e-07	0.1
p1m (pipelinem_2)	8.49e-07	3.70e-08	5.18e-08	9.38e-07	0.1
p1_h (pipeline1_4)	2.59e-05	1.04e-06	1.44e-06	2.84e-05	3.6
p2_h (pipeline1_3)	2.61e-05	1.04e-06	1.48e-06	2.86e-05	3.6
p3_h (pipeline1_2)	2.58e-05	1.04e-06	1.42e-06	2.83e-05	3.6
m1_h (mul_4)	0.000	0.000	9.93e-06	9.93e-06	1.3
mult_28 (mul_4_DW_mult_uns_0)	0.000	0.000	9.34e-06	9.34e-06	1.2
p2m (pipelinem_1)	8.49e-07	3.70e-08	5.18e-08	9.38e-07	0.1
p4_h (pipeline1_1)	2.61e-05	1.04e-06	1.48e-06	2.86e-05	3.6
m2_h (mul_3)	0.000	0.000	9.93e-06	9.93e-06	1.3
mult_28 (mul_3_DW_mult_uns_0)	0.000	0.000	9.34e-06	9.34e-06	1.2

Total Power下降


Thank
you