Delay of each pipeline stage

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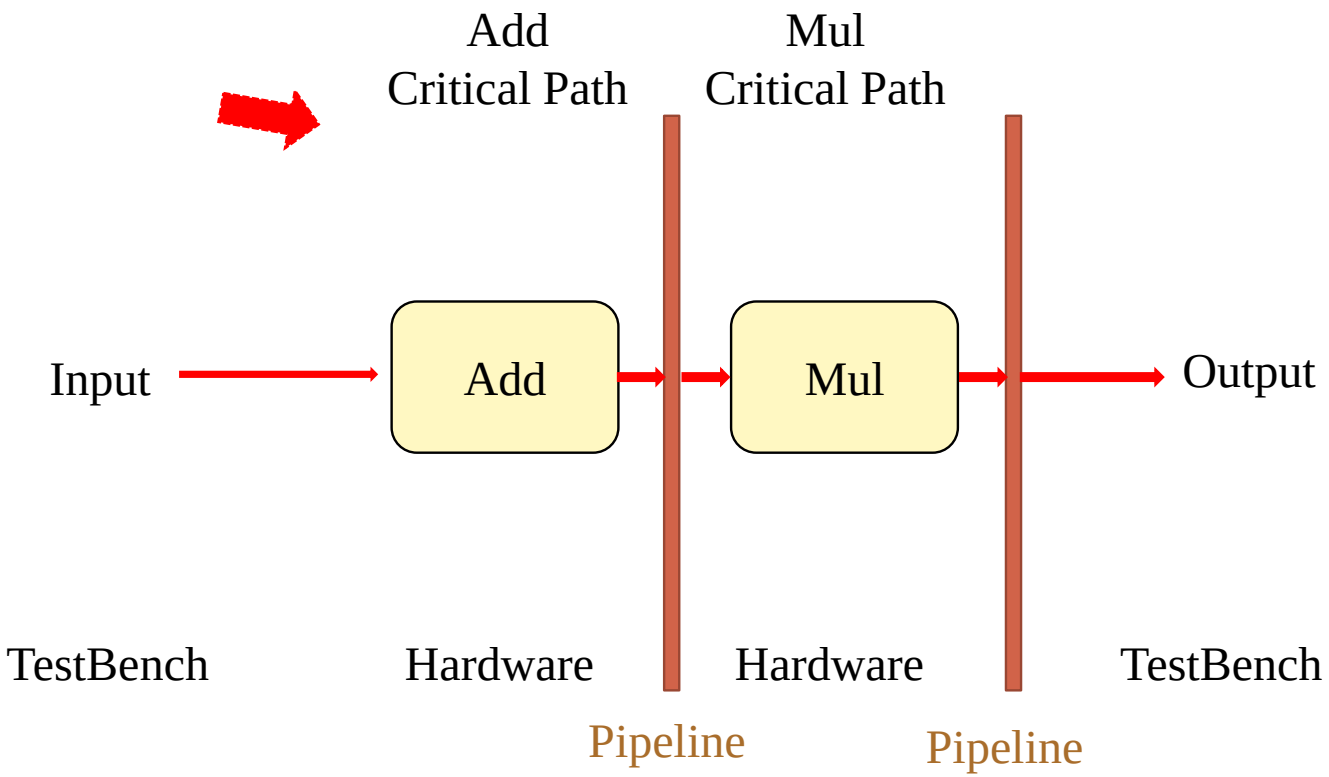
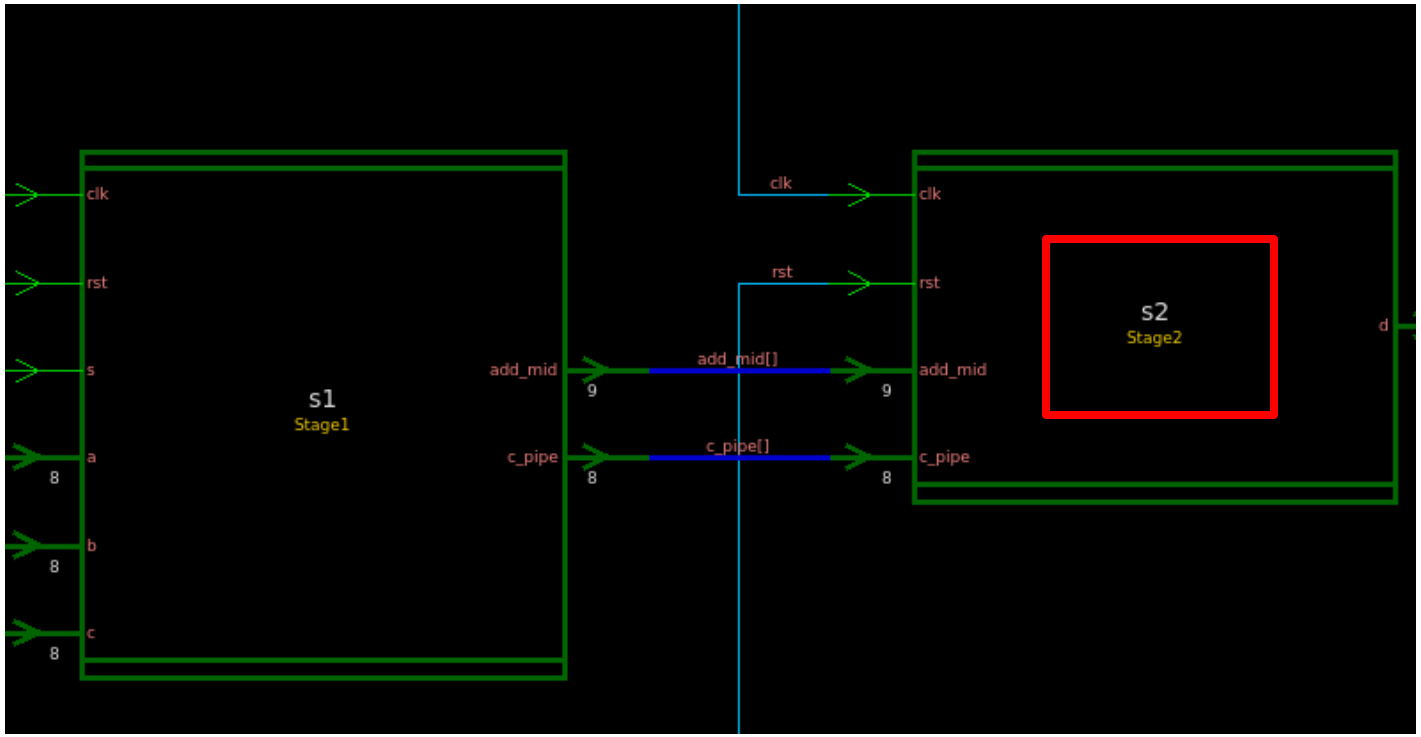
Report Timing

- Pipeline Critical Path
  - 單位：ns



Report Timing

- 如果直接report timing
- Design Compiler會Report Pipeline的Critical Path 也就是乘法器的delay



tcl說明

- 1.如果combinaitonal跟sequential分module寫
- 用上面的report

```
step1 s1(.sum(sum), .a(a), .b(b), .s(s));
pipe1 p1(.pipe1_sum(pipe1_sum), .pipe1_c(pipe1_c), .sum(sum), .c(c), .clk(clk), .rst(rst));
step2 s2(.d_out(d_out), .sum(pipe1_sum), .c(pipe1_c));
pipe2 p2(.d(d), .d_in(d_out), .clk(clk), .rst(rst));
```

```
uplevel #0 { report_timing  -through { s1/* } -path full -delay max -
uplevel #0 { report_timing  -through { s2/* } -path full -delay max -
# 如果combinational跟sequential寫在同一個module
# module name = s1/s2
# uplevel #0 { report_timing  -to { s1/*/D } -path full -delay max -n
# uplevel #0 { report_timing  -to { s2/*/D } -path full -delay max -n
```

- 2.如果combinational跟sequential寫在同一個module
- 用下面的report

```
Stage1 s1(.clk(clk), .rst(rst), .a(a), .b(b), .c(c), .s(s), .add_mid(add_mid), .c_pipe(c_pipe));
Stage2 s2(.clk(clk), .rst(rst), .add_mid(add_mid), .c_pipe(c_pipe), .d(d));
# 如果combinaitonal跟sequential分module寫
# combinational module name = s1/s2
# uplevel #0 { report_timing  -through { s1/* } -path full -delay
# uplevel #0 { report_timing  -through { s2/* } -path full -delay
# 如果combinational跟sequential寫在同一個module
# module name = s1/s2
uplevel #0 { report_timing  -to { s1/*/D } -path full -delay max
uplevel #0 { report_timing  -to { s2/*/D } -path full -delay max
```

Stage1 Delay(Add)

```
pipelined          ZeroWireload          N16ADFP_StdCellss0p72vm40c_ccs

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                 0.0000     0.0000
clock network delay (ideal)                           0.0000     0.0000
input external delay                                  0.0000     0.0000 r
b[0] (in)                                             0.0000     0.0000 r
s1/b[0] (Stage1)                                      0.0000     0.0000 r
s1/sub_31/B[0] (Stage1_DW01_sub_0)                    0.0000     0.0000 r
s1/sub_31/U9/ZN (CKND1BWP16P90LVT)                    0.0068     0.0068 f
s1/sub_31/U7/Z (OR2D1BWP16P90LVT)                     0.0160     0.0227 f
s1/sub_31/U2_1/CO (FA1D1BWP16P90LVT)                  0.0262     0.0490 f
s1/sub_31/U2_2/CO (FA1D1BWP16P90LVT)                  0.0276     0.0766 f
s1/sub_31/U2_3/CO (FA1D1BWP16P90LVT)                  0.0276     0.1042 f
s1/sub_31/U2_4/CO (FA1D1BWP16P90LVT)                  0.0276     0.1318 f
s1/sub_31/U2_5/CO (FA1D1BWP16P90LVT)                  0.0276     0.1595 f
s1/sub_31/U2_6/CO (FA1D1BWP16P90LVT)                  0.0276     0.1871 f
s1/sub_31/U2_7/S (FA1D1BWP16P90LVT)                   0.0391     0.2262 r
s1/sub_31/DIFF[7] (Stage1_DW01_sub_0)                 0.0000     0.2262 r
s1/U12/Z (MUX2D1BWP16P90LVT)                          0.0151     0.2413 r
s1/add_mid_reg_7_/D (DFCNQD2BWP16P90LVT)              0.0000     0.2413 r
data arrival time                                                0.2413

clock clk (rise edge)                                 0.2700     0.2700
clock network delay (ideal)                           0.0000     0.2700
s1/add_mid_reg_7_/CP (DFCNQD2BWP16P90LVT)             0.0000     0.2700 r
library setup time                                   -0.0143     0.2557
data required time                                               0.2557
-----------------------------------------------------------------------------
data required time                                               0.2557
data arrival time                                               -0.2413
-----------------------------------------------------------------------------
slack (MET)                                                      0.0144
```

Stage2 Delay (Mul)

Point	Incr	Path	
clock clk (rise edge)	0.0000	0.0000	
clock network delay (ideal)	0.0000	0.0000	
s1/c_pipe_reg_1_/CP (DFCNQD2BWP16P90LVT)	0.0000	0.0000	r
s1/c_pipe_reg_1_/Q (DFCNQD2BWP16P90LVT)	0.0426	0.0426	f
s1/c_pipe[1] (Stage1)	0.0000	0.0426	f
s2/c_pipe[1] (Stage2)	0.0000	0.0426	f
s2/mult_49/a[1] (Stage2_DW_mult_uns_2)	0.0000	0.0426	f
s2/mult_49/U550/Z (BUFFD4BWP16P90LVT)	0.0117	0.0543	f
s2/mult_49/U500/ZN (ND2D1BWP16P90)	0.0093	0.0636	r
s2/mult_49/U447/ZN (ND2D2BWP16P90LVT)	0.0120	0.0756	f
s2/mult_49/U490/ZN (ND2D2BWP16P90LVT)	0.0110	0.0866	r
s2/mult_49/U423/ZN (OAI22D4BWP16P90LVT)	0.0101	0.0967	f
s2/mult_49/U355/ZN (ND2D1BWP16P90LVT)	0.0073	0.1040	r
s2/mult_49/U408/ZN (ND3D1BWP16P90LVT)	0.0162	0.1201	f
s2/mult_49/U405/ZN (ND2D1BWP16P90LVT)	0.0083	0.1284	r
s2/mult_49/U407/ZN (ND3D1BWP16P90LVT)	0.0151	0.1436	f
s2/mult_49/U374/Z (XOR2D2BWP16P90LVT)	0.0269	0.1705	r
s2/mult_49/U463/Z (XOR2D2BWP16P90LVT)	0.0195	0.1900	f
s2/mult_49/U345/ZN (NR2D2BWP16P90LVT)	0.0124	0.2024	r
s2/mult_49/U470/ZN (OAI21D2BWP16P90LVT)	0.0129	0.2153	f
s2/mult_49/U593/ZN (AOI21D1BWP16P90LVT)	0.0101	0.2254	r
s2/mult_49/U594/ZN (OAI21D1BWP16P90LVT)	0.0120	0.2374	f
s2/mult_49/U597/ZN (XNR2D1BWP16P90LVT)	0.0178	0.2553	r
s2/mult_49/product[13] (Stage2_DW_mult_uns_2)	0.0000	0.2553	r
s2/d_reg_13_/D (DFCNQD2BWP16P90LVT)	0.0000	0.2553	r
data arrival time		0.2553	
clock clk (rise edge)	0.2700	0.2700	
clock network delay (ideal)	0.0000	0.2700	
s2/d_reg_13_/CP (DFCNQD2BWP16P90LVT)	0.0000	0.2700	r
library setup time	-0.0145	0.2555	
data required time		0.2555	
data required time		0.2555	
data arrival time		-0.2553	
slack (MET)		0.0003	

Output Delay

```
Point                                                   Incr       Path
-----------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
s2/d_reg_15_/CP (DFCNQD2BWP16P90LVT)                    0.00       0.00 r
s2/d_reg_15_/Q (DFCNQD2BWP16P90LVT)                     0.04       0.04 f
s2/d[15] (Stage2)                                       0.00       0.04 f
d[15] (out)                                             0.00       0.04 f
data arrival time                                                  0.04

clock clk (rise edge)                                   0.27       0.27
clock network delay (ideal)                             0.00       0.27
output external delay                                   0.00       0.27
data required time                                                 0.27
-----------------------------------------------------------------------
data required time                                                 0.27
data arrival time                                                 -0.04
-----------------------------------------------------------------------
slack (MET)                                                        0.23
```