

Xilinx Vivado Tutorial

2025/10/13
EC5015-VLSILab

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Outline

- 1. Download & Install**
- 2. Setup License**
- 3. Create Project**
- 4. Setting Constraint**
- 5. Xsim**
- 6. Synthesis & Implementation**
- 7. Summary**

Download & Install (1/12)

1. 連結至Xilinx官網 Website:

<https://www.xilinx.com/products/design-tools/vivado.html>

2. Resources & Support->Downloads-> Vivado ML Developer Tools

The screenshot shows the AMD Xilinx website's navigation bar at the top, featuring the AMD and Xilinx logos, followed by links for Products, Solutions, and Resources & Support (which is underlined). A vertical sidebar on the left contains links for Downloads, Developer Resources, Partner Resources, and Support. The main content area displays several categories: EPYC Processors, Radeon Graphics & AMD Chipsets, Adaptive SoCs & FPGAs, Ryzen Processors, Ethernet Adapters, and Vivado ML Developer Tools. Under each category, there are sub-links such as Client & Data Center Tech Docs, Drivers, Vitis Software Platform, EPYC White Papers & Briefs, Radeon ProRender Plug-ins, Vitis Accelerated Libraries, EPYC Tuning Guides, PRO Certified ISV Applications, Vitis Embedded Platforms, Ryzen Master Overclocking Utility, NIC Software & Downloads, StoreMI, and PRO Manageability Tools for IT Administrators. At the bottom of the page is a red button labeled "Download Now".

Download & Install (2/12)

3. 選擇Vivado Archive
4. 選擇2018.3並下載Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation裡的All OS installer Single-File Download

Version

[2023.1](#)

[2022.2](#)

[2022.1](#)

Vivado Archive

[ISE Archive](#)

[CAE Vendor Libraries](#)

[Archive](#)

Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Note: Download verification is only supported with Google Chrome and Microsoft Edge web browsers.

Download Includes

[Vivado Design Suite HLx Editions \(All Editions\)](#)

Download Type

[Full Product Installation](#)

Last Updated

Dec 10, 2018

Answers

[2018.x - Vivado Known Issues](#)

Documentation

[Release Notes](#)

Support Forums

[Installation and Licensing](#)

點這個

[!\[\]\(5bd3139e49b8ec618dddaa46174de8b0_img.jpg\) Vivado HLx 2018.3: All OS installer Single-File Download \(TAR/GZIP - 18.97 GB\)](#)

MD5 SUM Value : 8a3a75f26d0e20de21fc673ad9d40d0f

Download Verification [i](#)

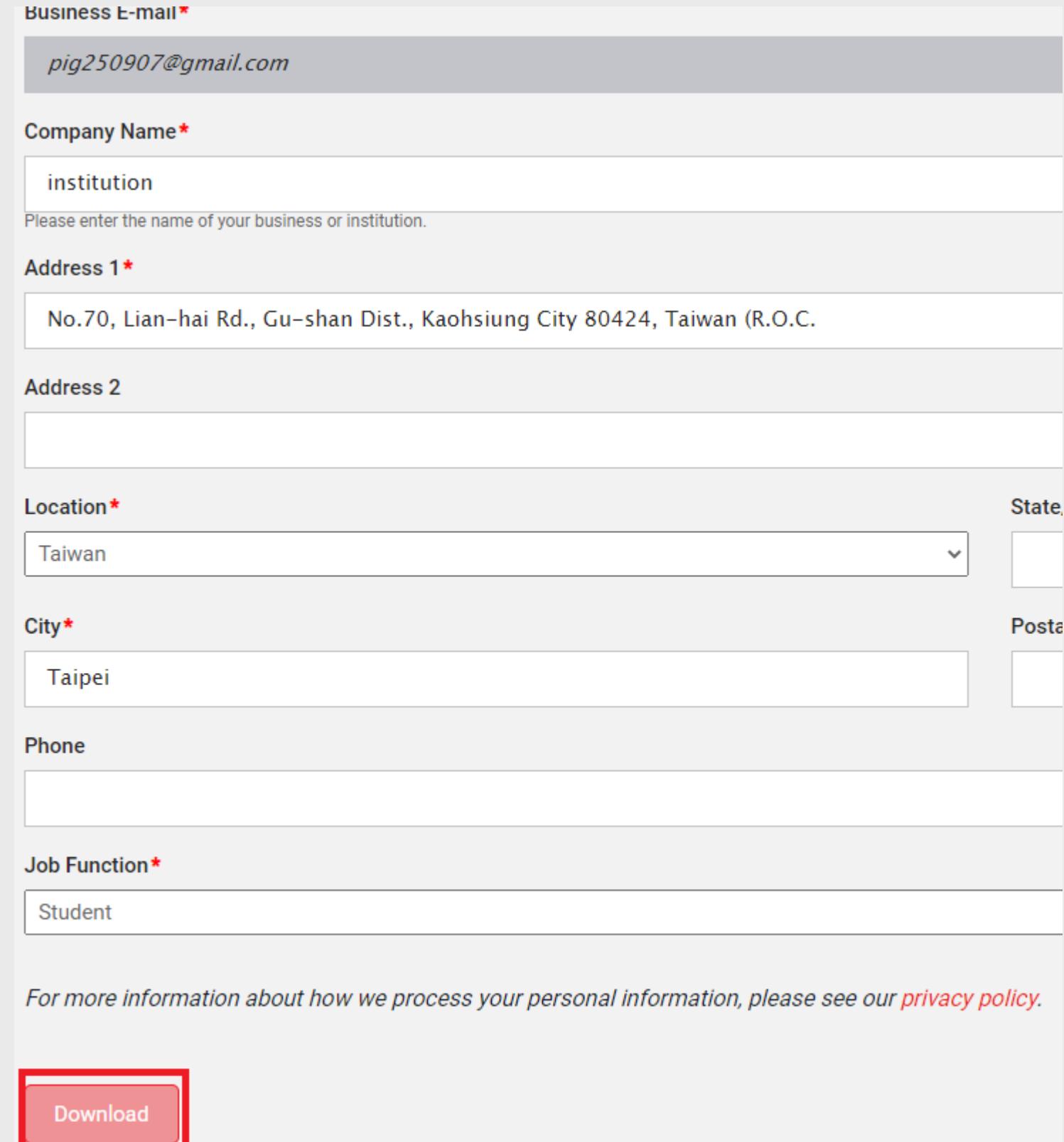
[Digests](#) [Signature](#) [Public Key](#)

Download & Install (2/12)

5. 註冊一個帳號，此帳號然後之後安裝會用到
6. 辦好後就能下載



The AMD login page features the AMD logo at the top left. Below it is a large "登入" (Login) button. The main form has two input fields: "電子郵件地址" (Email Address) and "密碼" (Password). A "登入" (Login) button is located below the password field. To the right of the password field is a small "或" (Or) link, followed by a "創建密碼" (Create Password) button. At the bottom of the page are links for "忘記/重設密碼？" (Forgot/Reset Password?), "幫助" (Help), "使用條款" (Terms of Use), and "隱私權" (Privacy).



The registration form consists of several input fields:

- Business E-mail***: pig250907@gmail.com
- Company Name***: institution
Please enter the name of your business or institution.
- Address 1***: No.70, Lian-hai Rd., Gu-shan Dist., Kaohsiung City 80424, Taiwan (R.O.C.)
- Address 2**: (empty field)
- Location***: Taiwan
- City***: Taipei
- Phone**: (empty field)
- Job Function***: Student

At the bottom, a note states: "For more information about how we process your personal information, please see our [privacy policy](#)". A prominent red "Download" button is located at the bottom center.

Download & Install (3/12)

1. Extract vivado.
2. execute installer
 - Windows :
 - A. Go to folder of vivado
 - B. Double-Click xsetup.exe
 - Linux :
 - A. Open terminal
 - B. cd <path to folder of vivado>
 - C. sudo ./xsetup

Download & Install (4/12)

Vivado 2017.4 Installer - Welcome

Welcome

We are glad you've chosen Xilinx as your platform development partner. This program can install the Vivado Design Environment, Software Development Kit and Documentation Navigator.

Supported operating systems for Vivado 2017.4 are:

- Windows 7.1: 64-bit
- Windows 10.0 Creators Update: 64-bit
- Red Hat Enterprise Linux 6.6-6.9: 64-bit
- Red Hat Enterprise Linux 7.2-7.3: 64-bit
- CentOS Linux 6.6-6.9: 64-bit
- CentOS Linux 7.2-7.3: 64-bit
- SUSE Enterprise Linux 11.4: 64-bit
- SUSE Enterprise Linux 12.2: 64-bit
- Ubuntu Linux 16.04.2 LTS: 64-bit - Additional library installation required

Note: This release requires upgrading your license server tools to the Flex 11.14.1 versions. Please confirm with your license admin that the correct version of the license server tools are installed and available, before running the tools.

Note: 32-bit machine support is now only available through HW Server standalone product installers

Note: This installation program will not install cable drivers on Linux. This item will need to be installed separately, with administrative privileges.

To reduce installation time, we recommend that you disable any anti-virus software before continuing.

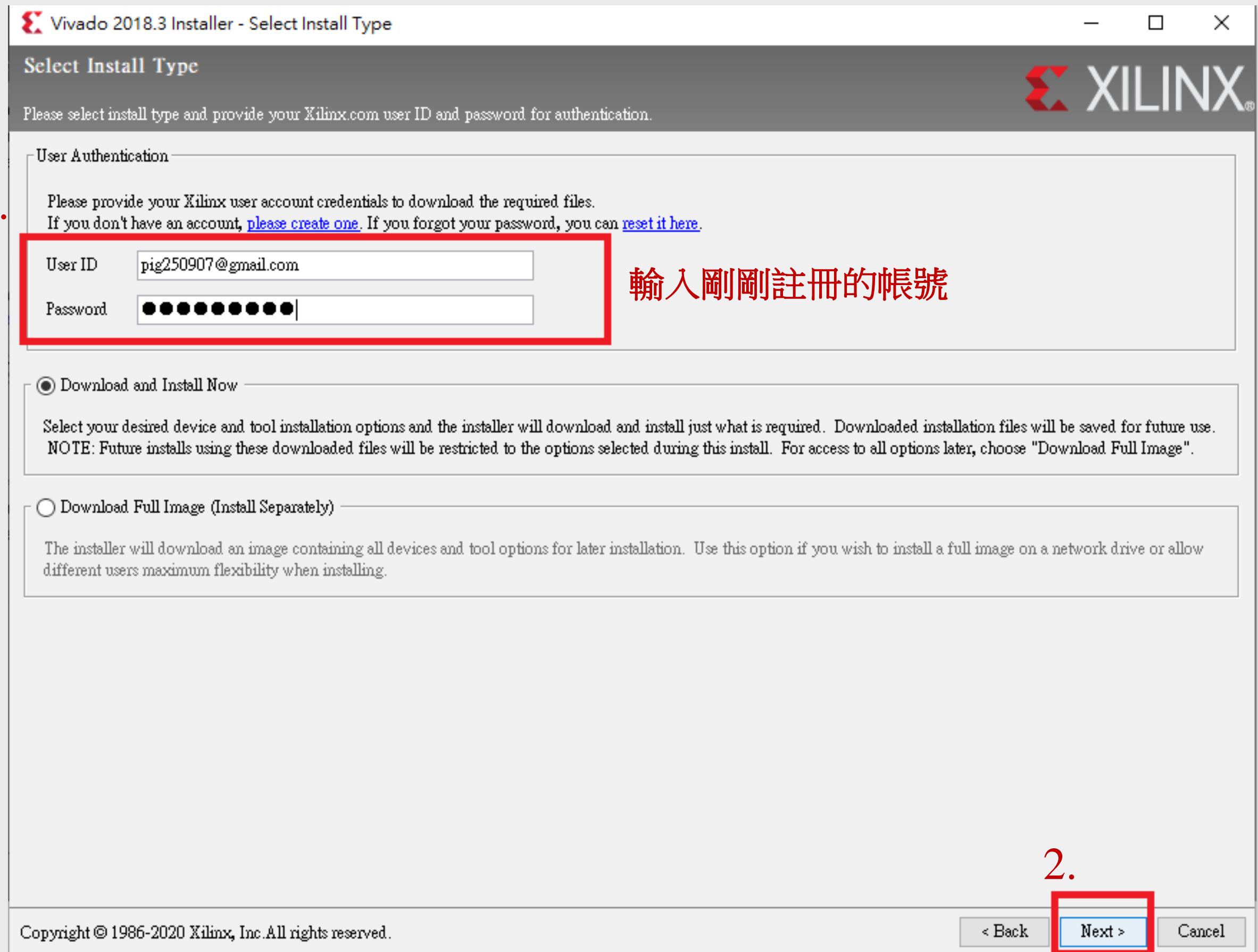
XILINX ALL PROGRAMMABLE.

1.

Copyright © 1986-2018 Xilinx, Inc. All rights reserved.

Preferences < Back Next > Cancel

Download & Install (5/12)



Download & Install (5/12)

Vivado 2017.4 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

Xilinx Inc. End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

1. I Agree

WebTalk Terms And Conditions

By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(a) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

I Agree

Third Party Software End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

2.

< Back Next > Cancel

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Download & Install (6/12)

Vivado 2017.4 Installer - Select Edition to Install

Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

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Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

Vivado HL Design Edition

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

Vivado HL System Edition

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

Documentation Navigator (Standalone)

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

1.

2.

< Back Next > Cancel

Copyright © 1986-2018 Xilinx, Inc. All rights reserved.

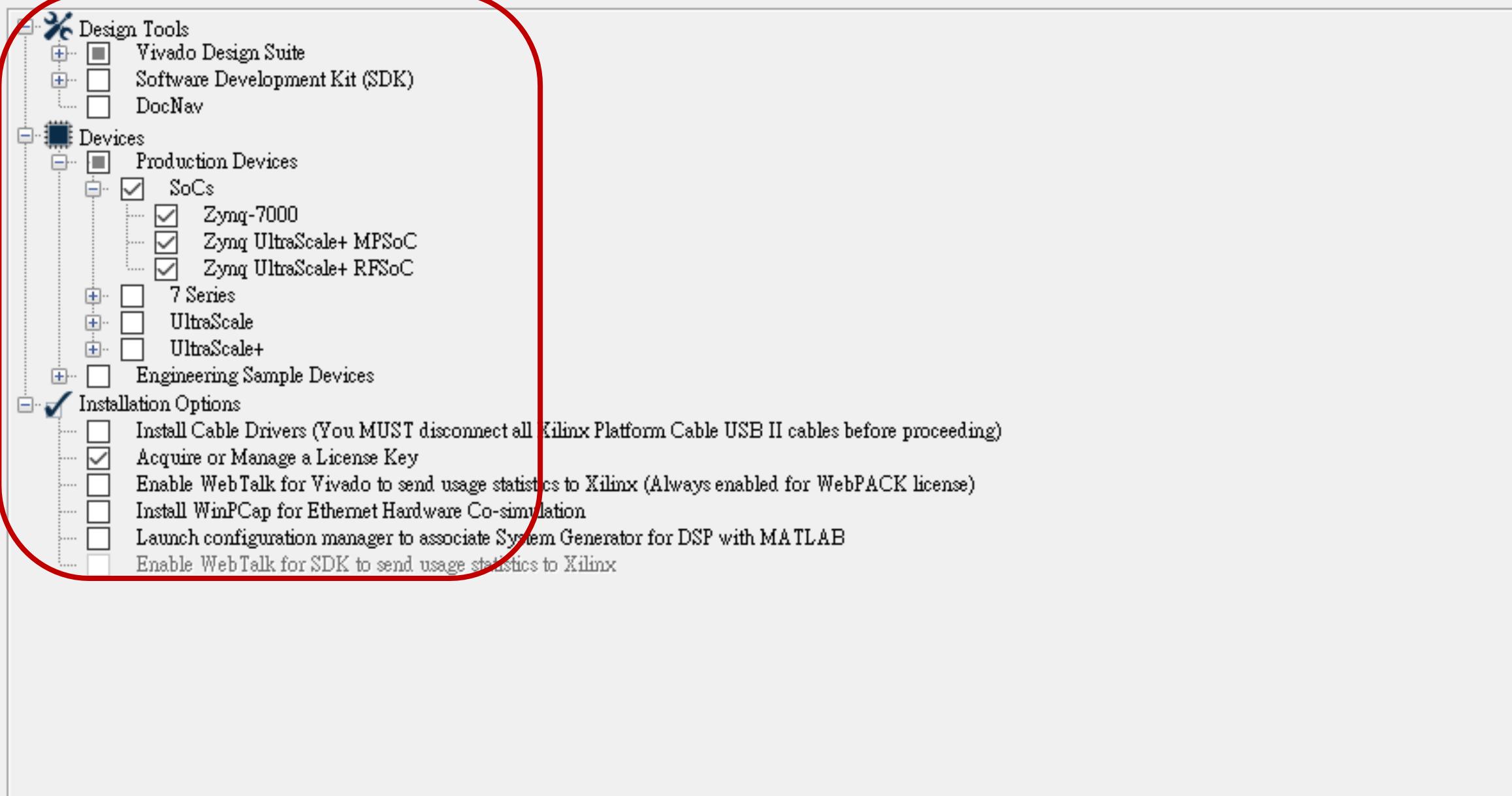
Download & Install (7/12)

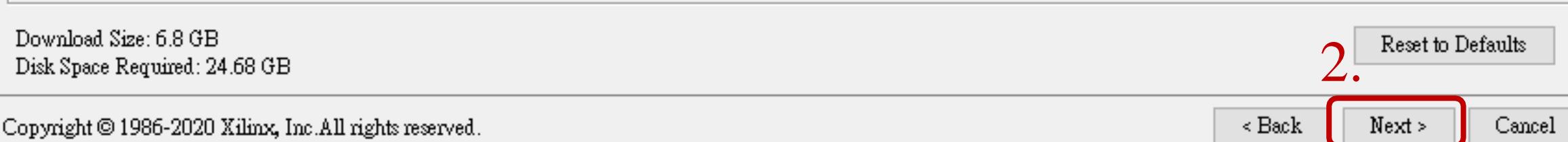
Vivado 2018.3 Installer - Vivado HL System Edition

Vivado HL System Edition

Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.

XILINX

1. 

2. 

Design Tools

- Vivado Design Suite
- Software Development Kit (SDK)
- DocNav

Devices

- Production Devices
 - SoCs
 - Zynq-7000
 - Zynq UltraScale+ MPSoC
 - Zynq UltraScale+ RFSoC
 - 7 Series
 - UltraScale
 - UltraScale+
- Engineering Sample Devices

Installation Options

- Install Cable Drivers (You MUST disconnect all Xilinx Platform Cable USB II cables before proceeding)
- Acquire or Manage a License Key
- Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)
- Install WinPCap for Ethernet Hardware Co-simulation
- Launch configuration manager to associate System Generator for DSP with MATLAB
- Enable WebTalk for SDK to send usage statistics to Xilinx

Download Size: 6.8 GB

Disk Space Required: 24.68 GB

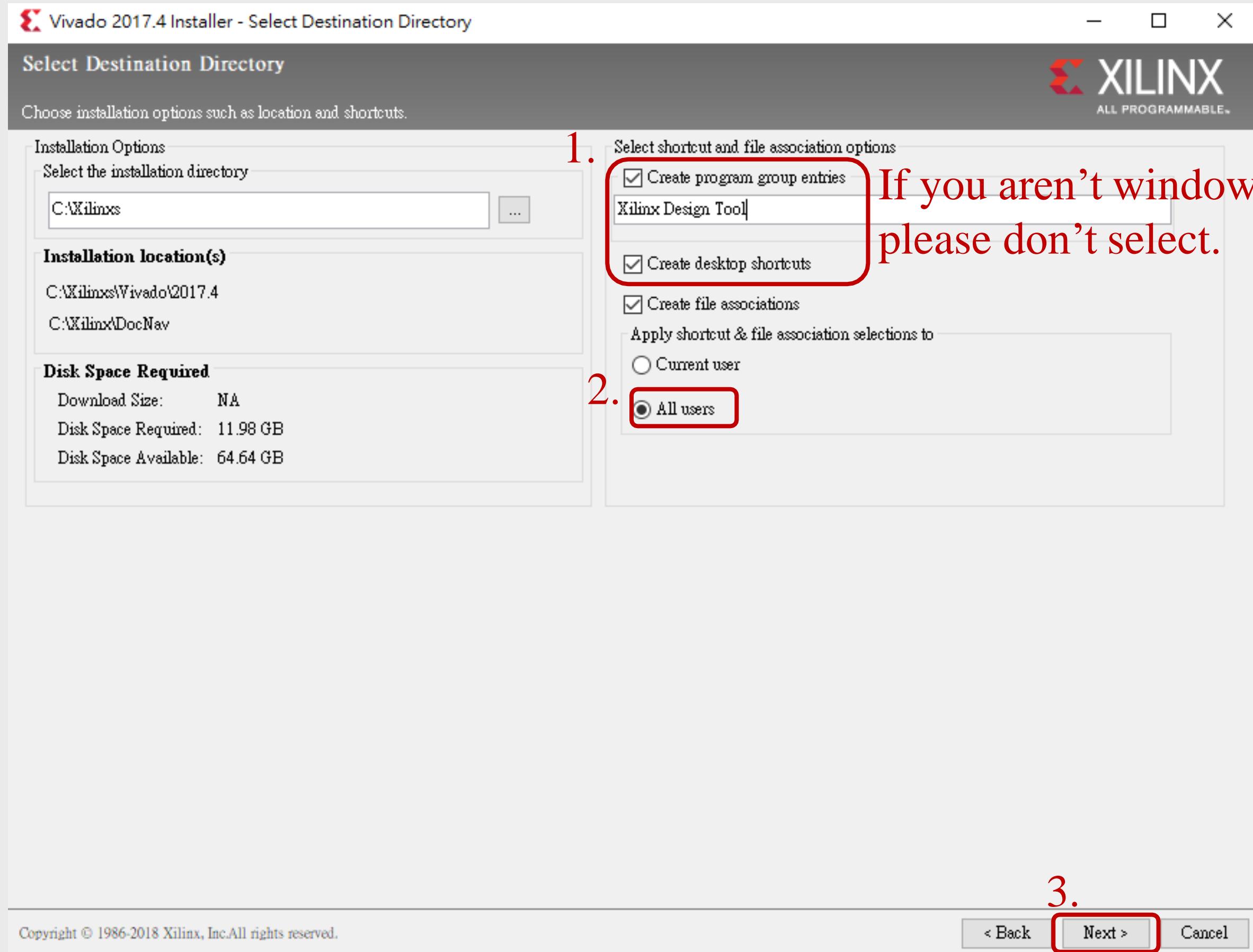
Reset to Defaults

< Back

Next >

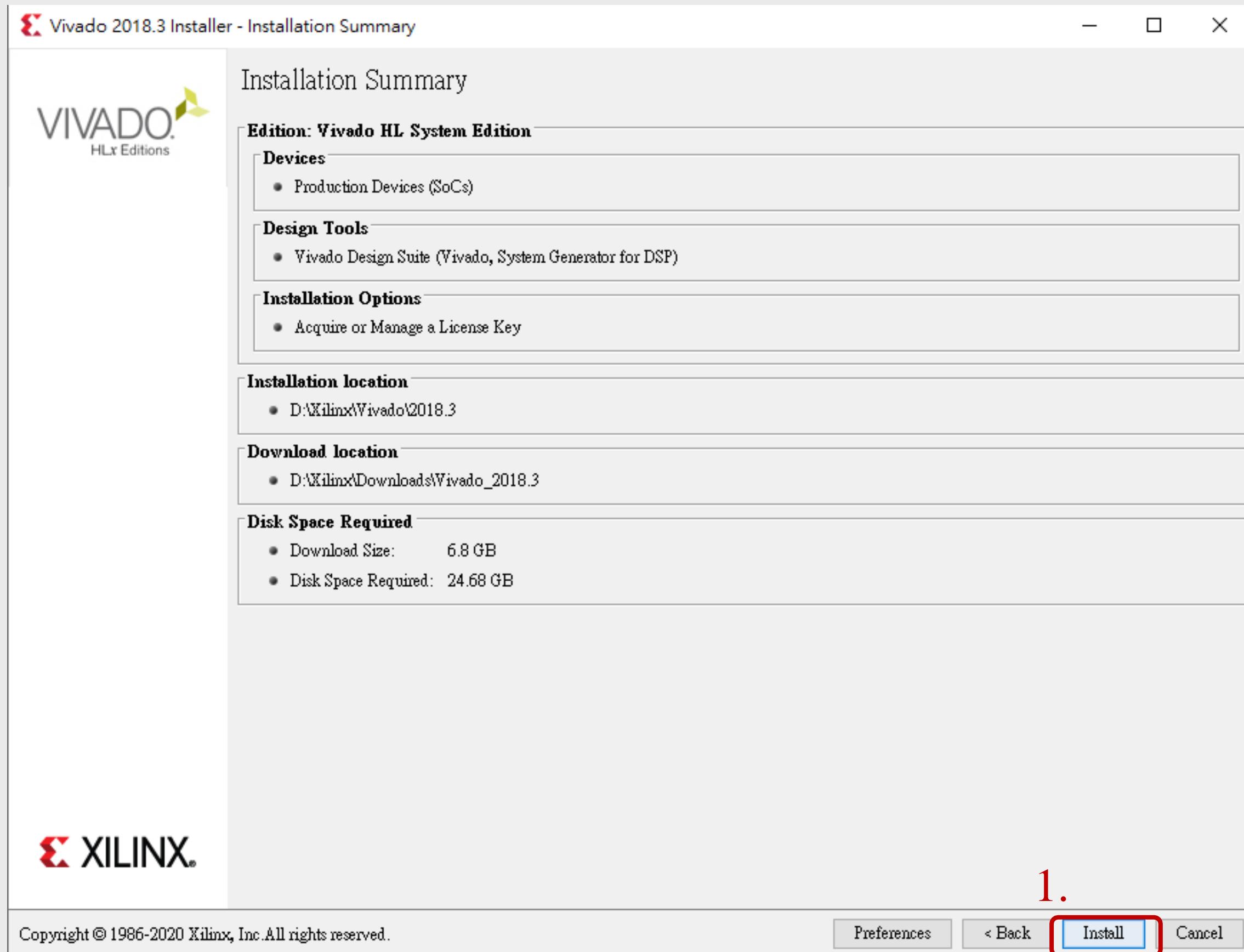
Cancel

Download & Install (8/12)



Download & Install (9/12)

- 如安裝完成後遇到License，可先至18頁設定。



Download & Install (10/12) **(Linux Only)**

If you use Linux, you need to set environment variable.

1. Open terminal
2. cd ~
3. gedit ./bashrc
4. Paste the following code to blank position
 - ◆ source <path to vivado>/settings64.sh
5. Save & Exit

Download & Install (11/11)

After installing vivado, you can open vivado by following :

1. Window :

- ◆ Double-Click the icon



2. Linux :

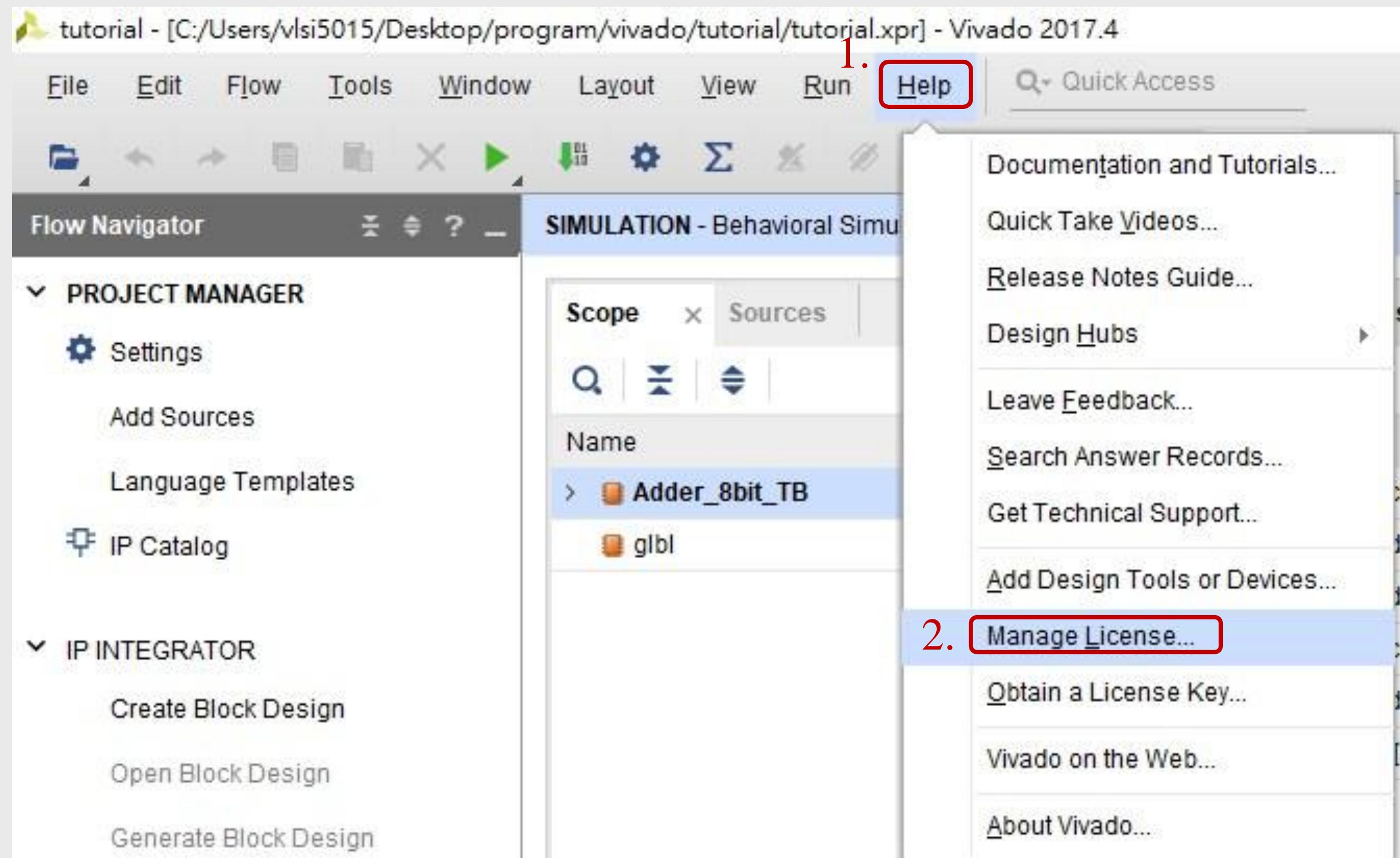
A. Open terminal

B. vivado &

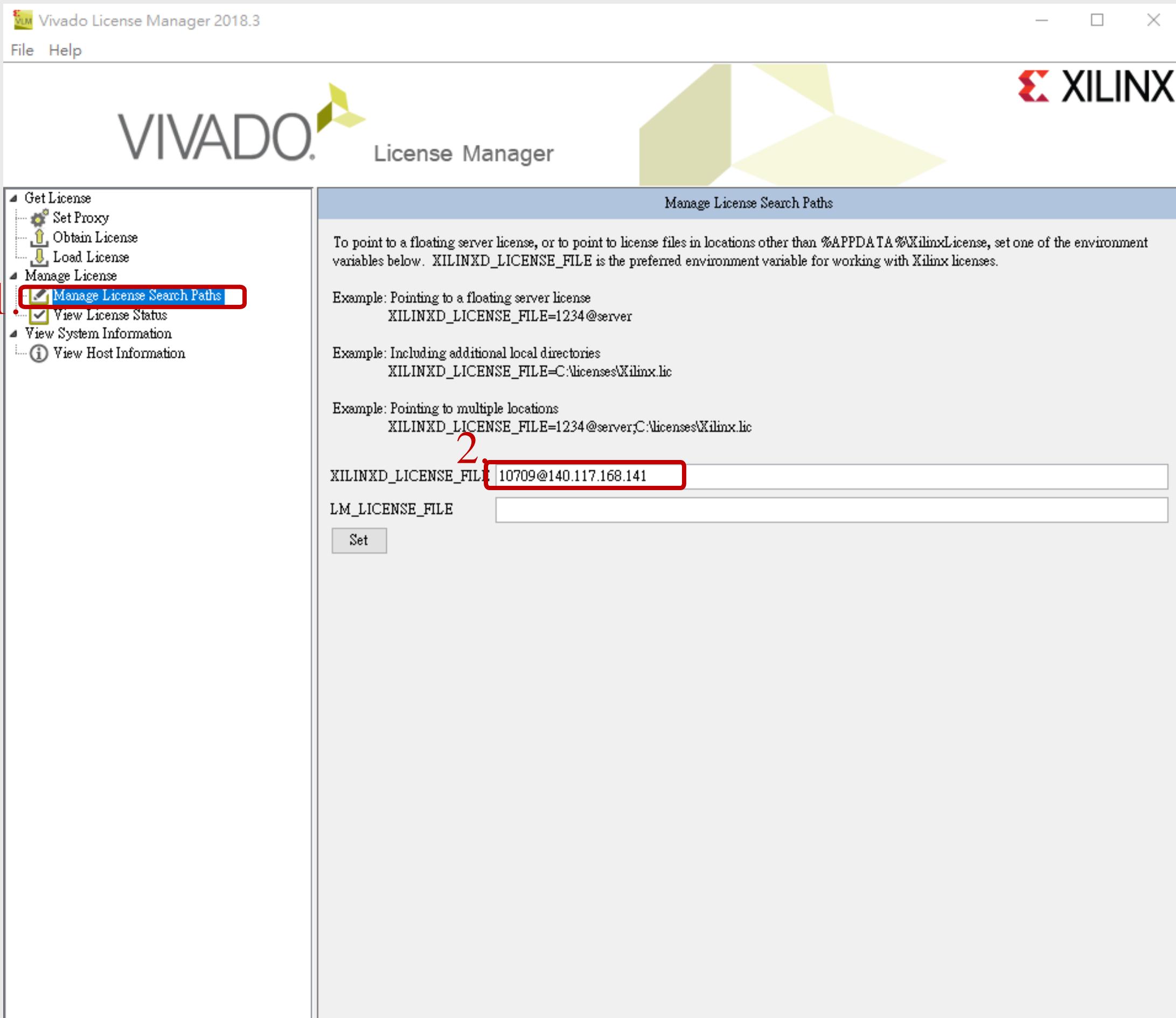
Outline

1. Download & Install
2. Setup License(可略過)
3. Create Project
4. Setting Constraint
5. Xsim
6. Synthesis & Implementation
7. Summary

Setup License (1/4)



Setup License (2/4) (Windows)



Setup License (3/4) (Linux)

1. Open terminal
2. cd ~
3. gedit ./bashrc
4. Paste the following code to blank position
 - ◆ export XILINXD_LICENSE_FILE=10709@140.117.168.141
5. Save & Exit

Setup License (4/4)

VLM Vivado License Manager 2017.4

File Help

VIVADO License Manager

XILINX ALL PROGRAMMABLE

View License Status

Certificate Based Licenses:

Filter: Hide Free Built-in Licenses

1. **View License Status**

2.

| License Name | Tools/IP | Expiration Date | Version Limit | License Type | Location | # |
|------------------------|----------|-----------------|---------------|--------------|--|----|
| PartialReconfiguration | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| PartialReconfiguration | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| PlanAhead | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| SDK | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| SDK | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| SDSoC_Tools | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| Simulation | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| Simulation | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| Synthesis | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| SysGen | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| Vivado_System_Edition | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |
| XC7Z010 | Tools | Permanent | 2019.03 | Nodelocked | C:\Users\wlsi5015\AppData\Local\Temp\XILINX\l... | Ur |

Activation Based Licenses:

NOTE: Support for activation based licenses has been deprecated. Your existing activation licenses have been replaced with certificate based licenses and added into your licensing account.

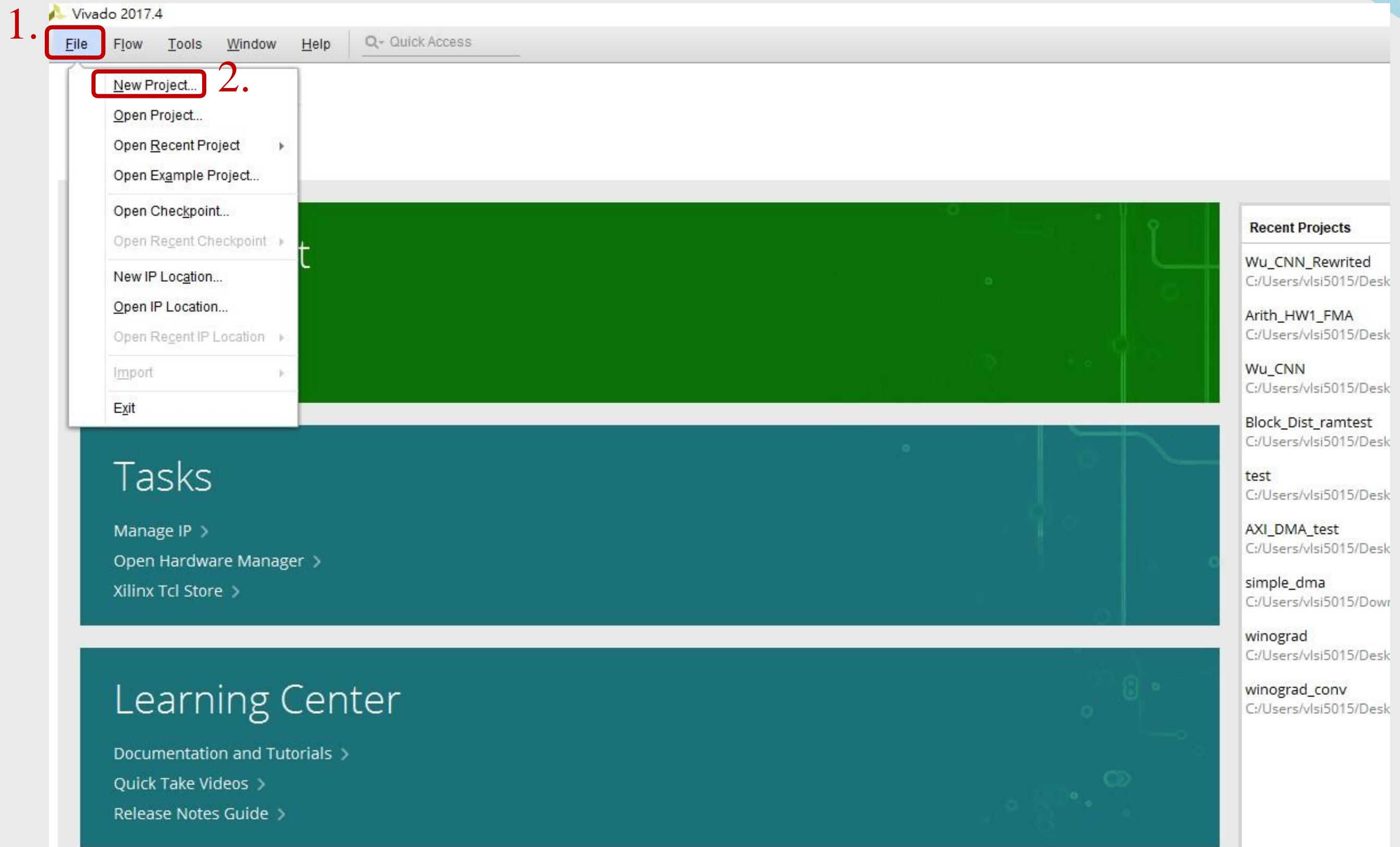
| License Name | Tools/IP | Expiration Date | Version Limit | Server/Client | Location | # of S |
|--------------|----------|-----------------|---------------|---------------|----------|--------|
| | | | | | | |

3. If you set license successfully, you will see a lot of items in this field.

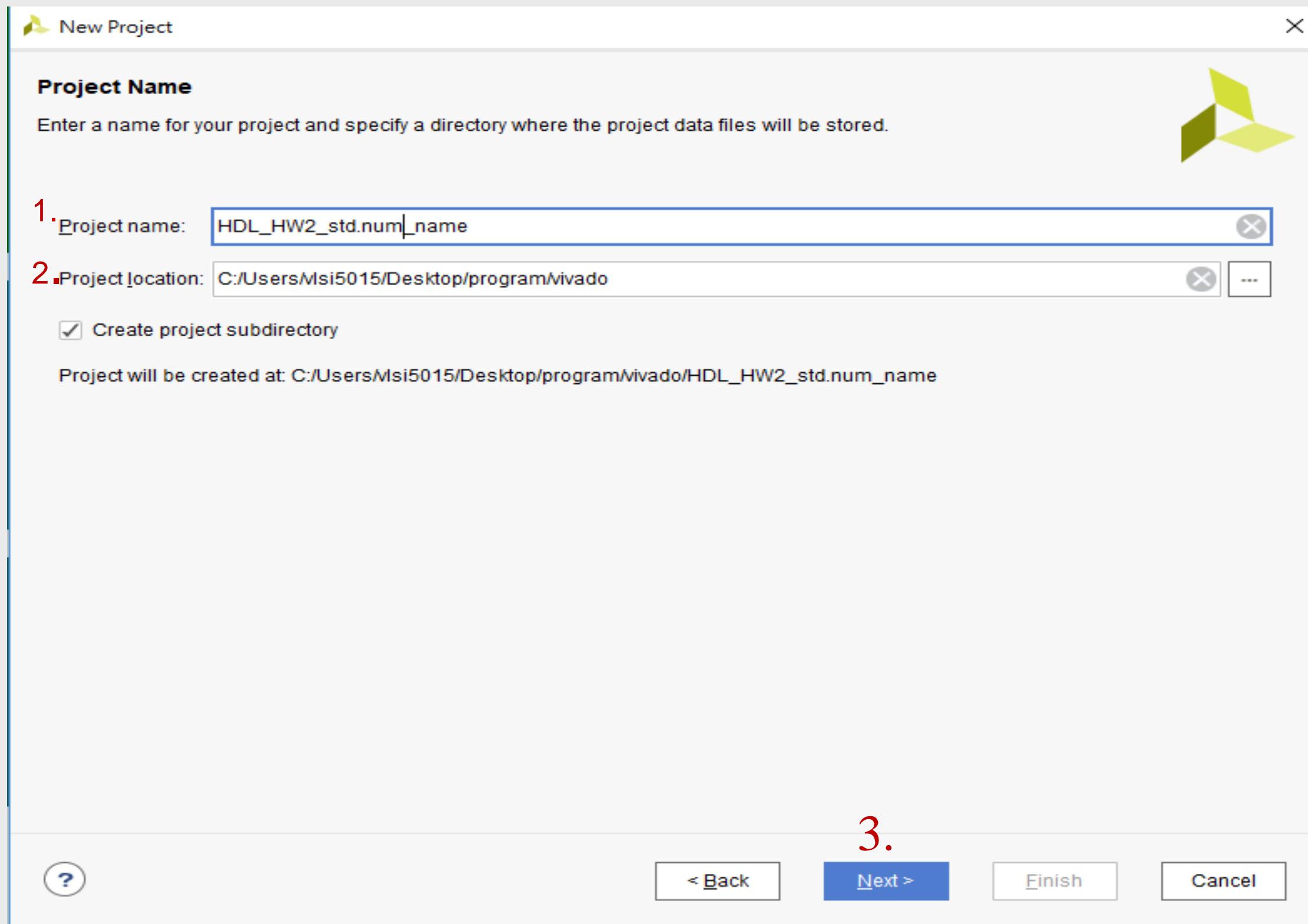
Outline

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Create Project (1/8)



Create Project (2/8)



Create Project (3/8)

New Project X

Project Type
Specify the type of project to create.



1. RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

2. Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

We add source codes later
or you can add now by unselecting this option.

3. < Back Next > Finish Cancel

Create Project (4/8)

New Project >

Default Part
Choose a default Xilinx part or board for your project.

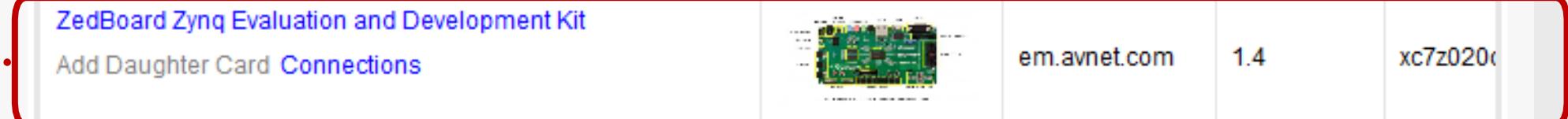
Parts | **Boards** 1.

Reset All Filters

Vendor: All Name: All

Search: (1 match)

| Display Name | Preview | Vendor | File Version | Part |
|---|---|--------------|--------------|----------|
| ZedBoard Zynq Evaluation and Development Kit Add Daughter Card Connections |  | em.avnet.com | 1.4 | xc7z020c |

2. 

? < Back 3. Next > Finish Cancel

Create Project (5/8)

New Project X

VIVADO
HLx Editions

New Project Summary

- i** A new RTL project named 'HDL_HW2_std.num_name' will be created.
- i** The default part and product family for the new project:
Default Board: ZedBoard Zynq Evaluation and Development Kit
Default Part: xc7z020clg484-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg484
Speed Grade: -1

XILINX ALL PROGRAMMABLE To create the project, click Finish

1.

< Back Next > **Finish** Cancel

Create Project (6/8)

The screenshot shows the Vivado Project Manager interface. The left sidebar contains a tree view of project components:

- PROJECT MANAGER**:
 - Settings (highlighted with a red box)
 - Add Sources (highlighted with a red box)
 - Language Templates
 - IP Catalog
- IP INTEGRATOR**:
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION**:
 - Run Simulation
- RTL ANALYSIS**:
 - Open Elaborated Design
- SYNTHESIS**:
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION**:
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG**:
 - Generate Bitstream
 - Open Hardware Manager

The main area displays the **PROJECT MANAGER - tutorial** window. It includes:

- Sources** panel: Shows Design Sources, Constraints, and Simulation Sources (with sim_1 selected).
- Project Summary** panel:

| | |
|---------------------|--|
| Settings | Edit |
| Project name: | tutorial |
| Project location: | C:/Users/lsi5015/Desktop/program/vivado/tutorial |
| Product family: | Zynq-7000 |
| Project part: | ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1) |
| Top module name: | Not defined |
| Target language: | Verilog |
| Simulator language: | Mixed |
- Board Part** panel:

| | |
|------------------|---|
| Display name: | ZedBoard Zynq Evaluation and Development Kit |
| Board part name: | em.avnet.com:zed:part0:1.3 |
| Connectors: | |
| Repository path: | C:/Xilinx/Vivado/2017.4/data/boards/board_files |
| URL: | http://www.zedboard.org |
| Board overview: | ZedBoard Zynq Evaluation and Development Kit |
- Synthesis** panel:

| | |
|-----------|-----------------------|
| Status: | Not started |
| Messages: | No errors or warnings |
- Implementation** panel:

| | |
|-----------|--|
| Status: | |
| Messages: | |
- Design Runs** panel:

| Name | Constraints | Status | WNS | TNS | WHS | THS | TPWS | Total Power | Failed Routes | LUT | FF | BRAMs | URAM | DSP | Start | Elapsed | Run Strategy |
|---------|-------------|-------------|-----|-----|-----|-----|------|-------------|---------------|-----|----|-------|------|-----|-------|---------|------------------|
| synth_1 | constrs_1 | Not started | | | | | | | | | | | | | | | Vivado Synth |
| impl_1 | constrs_1 | Not started | | | | | | | | | | | | | | | Vivado Implement |

Create Project (7/8)

Add Sources X

VIVADO
HLx Editions

Add Sources
This guides you through the process of adding and creating sources for your project

1.

- Add or create constraints
- Add or create design sources
- Add or create simulation sources

Constraint
Source code
Testbench

2.

[? Help](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Create Project (8/8)

Add Sources X

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.



1. Add Files Add Directories Create File

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

2. < Back Next > Finish Cancel

?

Outline

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Setting Constraint (1/5)

1. All you have to do is setting clock frequency, because the homework only asks you complete running implementation

2. There are two ways to set timing constraint
 - A. Create .xdc file and write constraint.
 - B. Use GUI

Setting Constraint (2/5) (.xdc)

1. Create xdc file.

2. Write the below constraint to .xdc file.

create_clock -period 10.000 -name clk -waveform {0.000 5.000}

[get_ports clk]

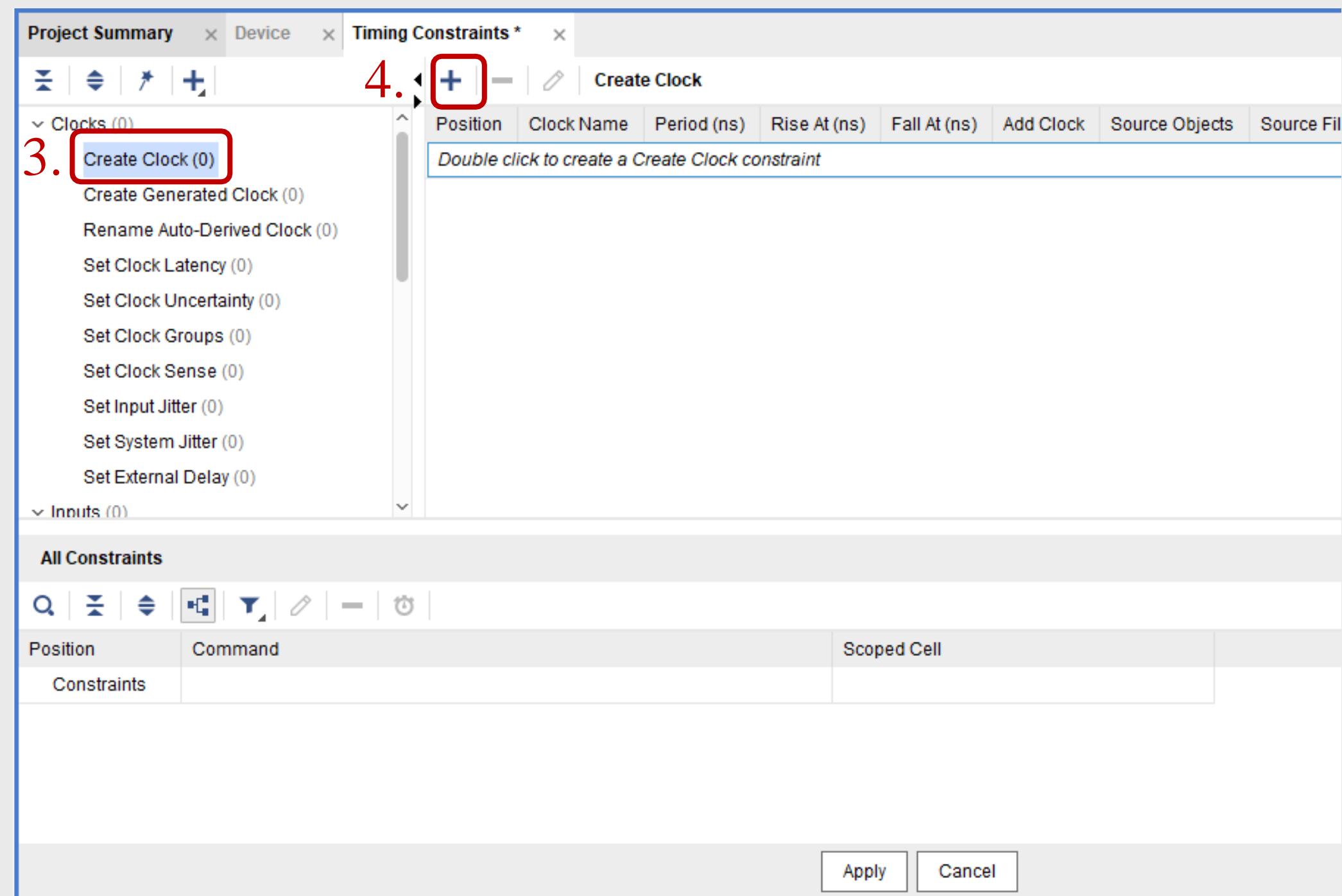
3. Explain :

1. Create_clock : Create an independent clock source signal
2. {0.000 5.000} : posedge at 0.0ns, negedge at 5.0ns
3. [get_ports clk] : Send clock signal to clk of Verilog's input port

Setting Constraint (3/5) (GUI)

- ▼ SYNTHESIS
 - ▶ Run Synthesis
 - ▼ Open Synthesized Design
 - Constraints Wizard
 - 2. **Edit Timing Constraints**
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
- ▼ IMPLEMENTATION
 - ▶ Run Implementation
 - ▼ Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction

1. You must run synthesis once after creating project.



Setting Constraint (4/5) (GUI)

The screenshot shows the Vivado GUI with two open dialogs:

- Create Clock Dialog (Left):** Shows fields for Clock name (clk), Source objects (empty), Waveform (Period: 10 ns, Rise at: 0 ns, Fall at: 5 ns), and a checkbox for 'Add this clock to the existing clock (no overwriting)'. A red box highlights the 'Clock name' field.
- Specify Clock Source Objects Dialog (Right):** Shows a search interface with 'Find names of type: I/O Ports'. A red box highlights the 'Find' button.

Red numbers 1 through 6 indicate steps:

1. Set the Clock name to clk.
2. Click the '...' button in the Specify Clock Source Objects dialog to open the search interface.
3. After Clicking 'Find', vivado will show result in the right field.
4. Find clk port and move from left field to right.
5. Set the selected clk port.
6. Click OK in the Create Clock dialog.

Below the dialogs, a results list shows 'Found: 51' items, with 'clk' selected. A red box highlights the 'Selected: 1' field.

Setting Constraint (5/5) (GUI)

The screenshot shows the Vivado Timing Constraints interface. In the top navigation bar, the 'Timing Constraints' tab is selected. On the left, a tree view shows 'Clocks (1)' with 'Create Clock (1)' selected. The main area displays a table for creating a clock constraint:

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File |
|----------|------------|-------------|--------------|--------------|--------------------------|-----------------|----------------|
| 2 | clk | 10.000 | 0.000 | 5.000 | <input type="checkbox"/> | [get_ports clk] | <unsaved co... |

A tooltip below the table says 'Double click to create a Create Clock constraint'. In the bottom section, under 'All Constraints', there is a table:

| Position | Command | Scoped Cell |
|-------------------------|---|-------------|
| Constraints | 1. | |
| 2 <unsaved constraints> | | |
| 2 | create_clock -period 10.000 -name clk -waveform {0.000 5.000} [get_ports clk] | |

The constraint '2' is highlighted with a red box. In the bottom right corner of the application window, there are 'Apply' and 'Cancel' buttons, with 'Apply' also highlighted by a red box.

3. Finally, you have to check the timing

2.
Apply Cancel

constraint written correctly in the .xdc file.

Outline

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Xsim

(1/7)

The screenshot shows the Xilinx Vivado interface with the 'SIMULATION' section selected in the left sidebar. A red box highlights the 'Settings' icon under 'PROJECT MANAGER'. The main window displays the 'Settings' dialog for 'Simulation'.

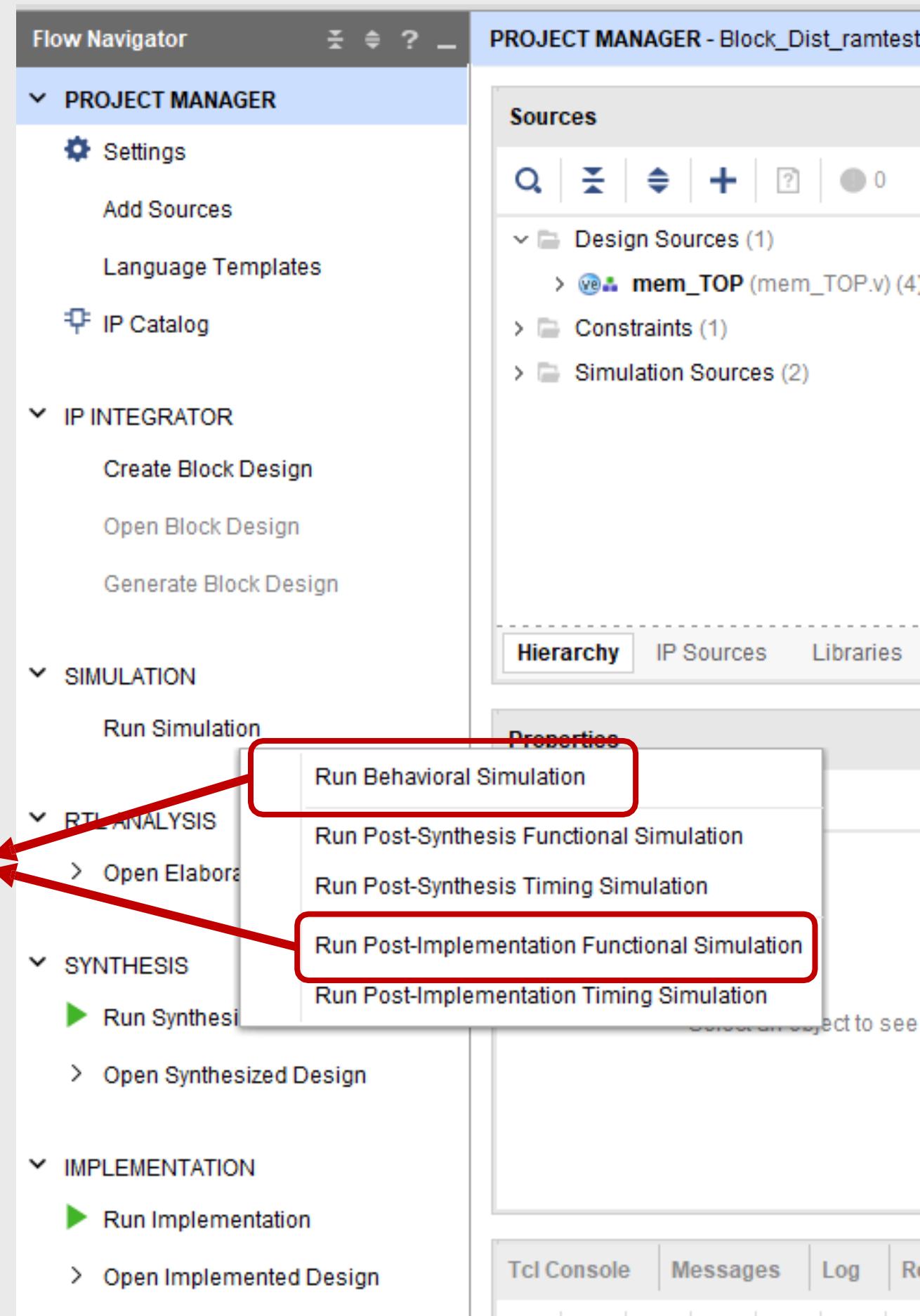
1. Click on the 'Settings' icon in the Project Manager.
2. Select the 'Simulation' tab in the Project Settings.
3. In the 'Tool Settings' tab, click on the 'Simulation' tab.
4. Under 'Tool Settings', enter '-all' in the 'xsim.simulate.runtime*' field. A red box highlights this step, and the text 'Enter -all' is overlaid.
5. Click the 'OK' button at the bottom right of the dialog.

Annotations:

- Step 1: 'Settings' icon highlighted with a red box.
- Step 2: 'Simulation' tab highlighted with a red box.
- Step 3: 'Simulation' tab in the tool settings highlighted with a red box.
- Step 4: 'xsim.simulate.runtime*' field with '-all' entered, highlighted with a red box. The text 'Enter -all' is overlaid.
- Step 5: 'OK' button highlighted with a red box.

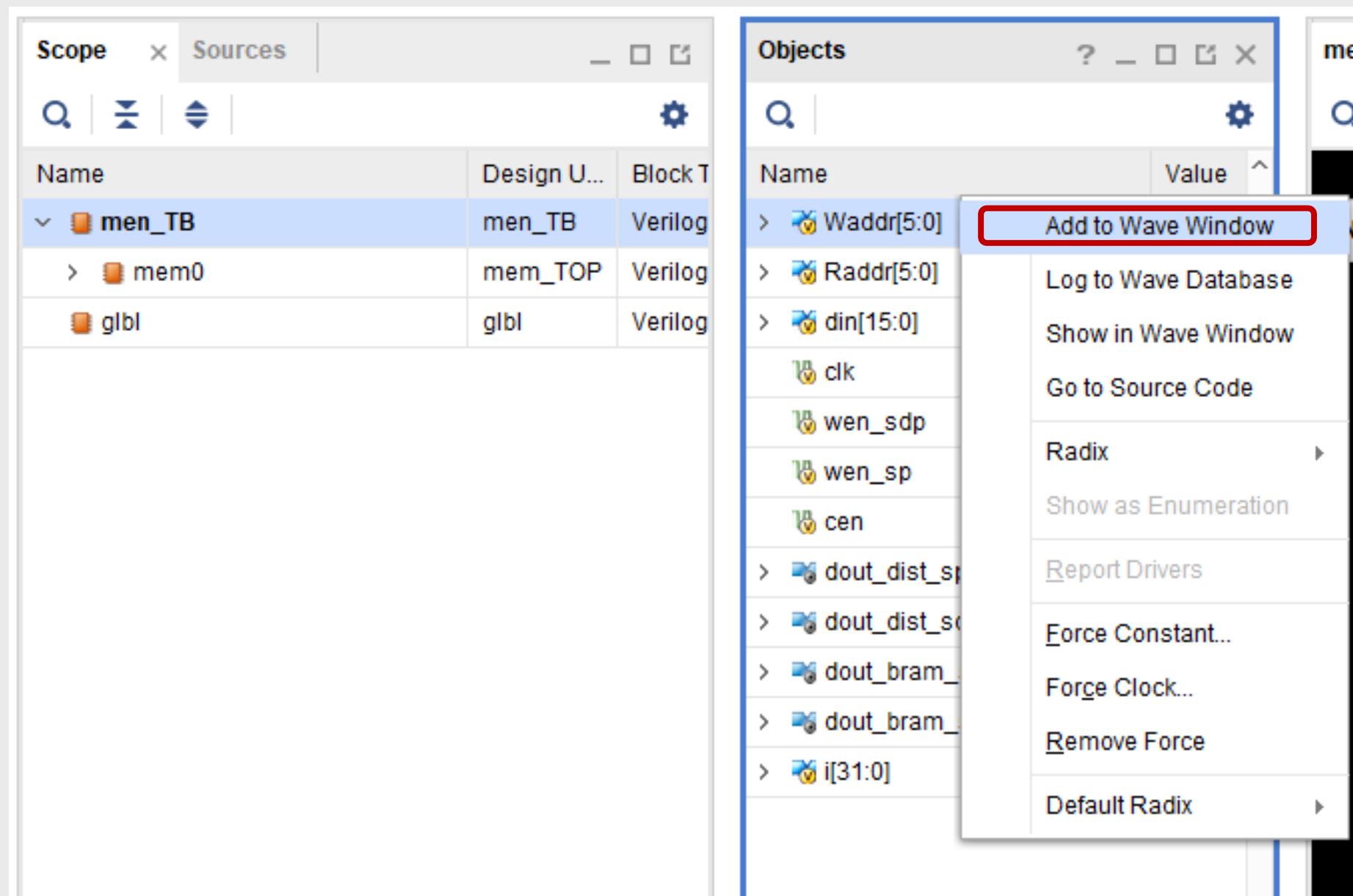
Xsim

(2/7)

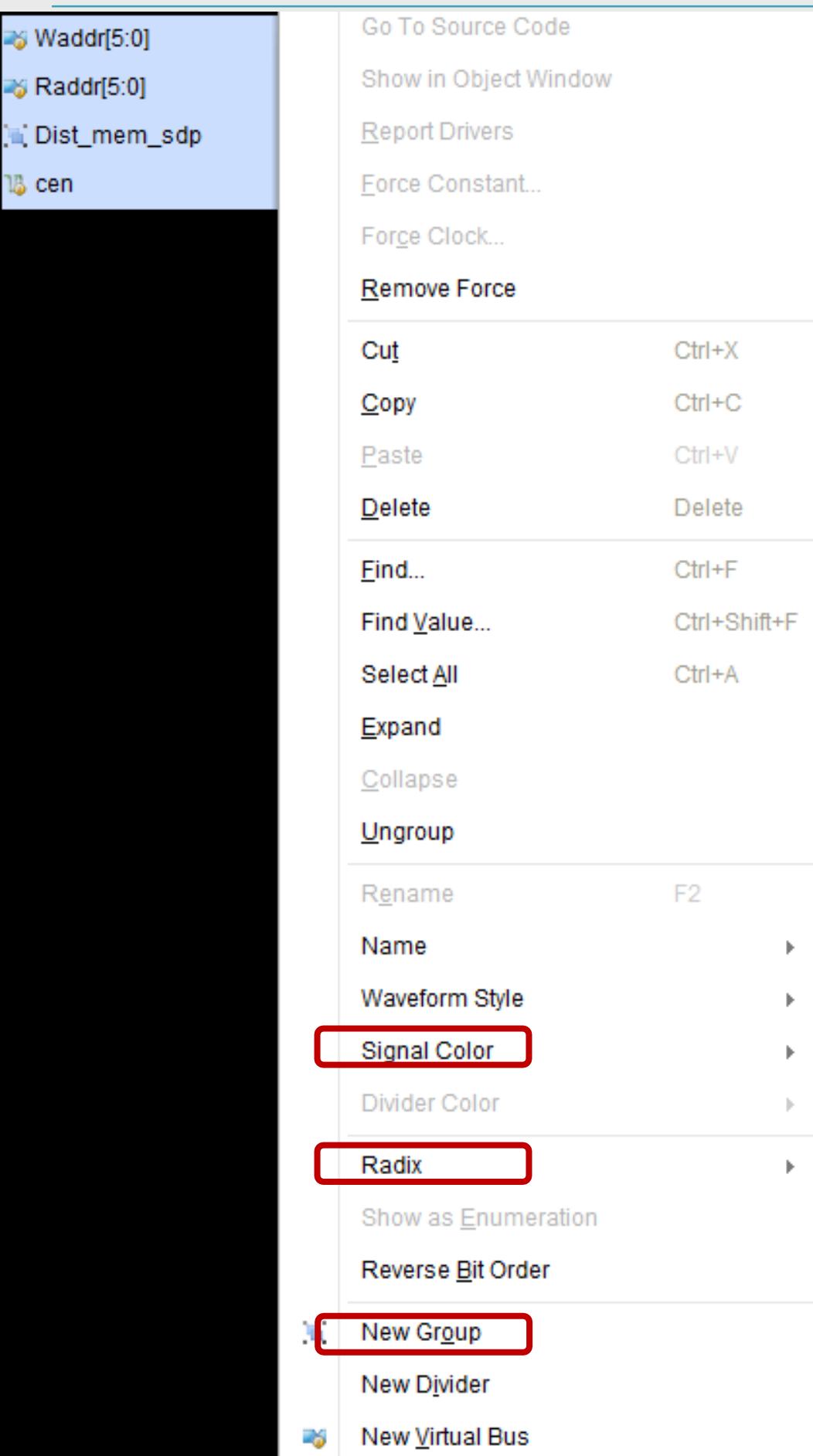


We mainly use
these two
Simulation

Xsim (3/7)



- You can add some signals which you want to observe.



- There are three ways to help you observe waveform efficiently.

1. New Group :

Fold several signals into one row.

2. Signal Color

: Change

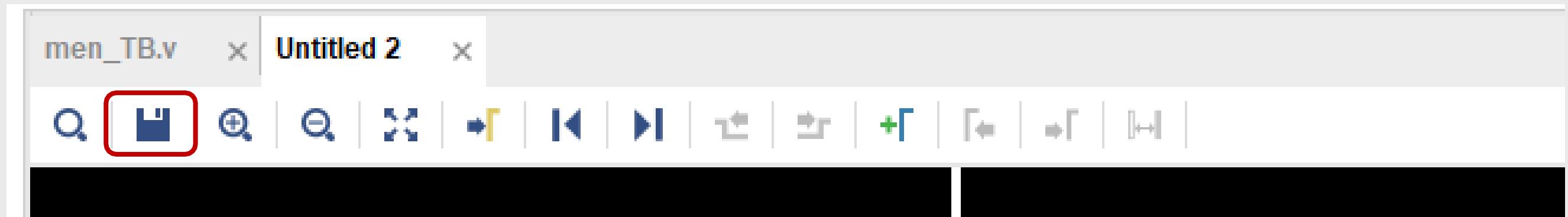
color

3. Radix :

1. Dec, Hex, etc.

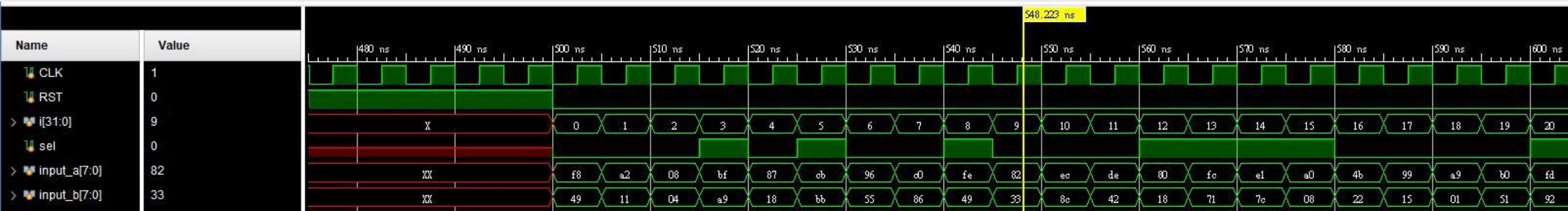
Xsim (5/5)

- After you arranged the signals in waveform, you can ‘Save Waveform Configuration’ (.wcfg)



Xsim (5/5)

- 截圖 pre/post sim 波型(共兩張)

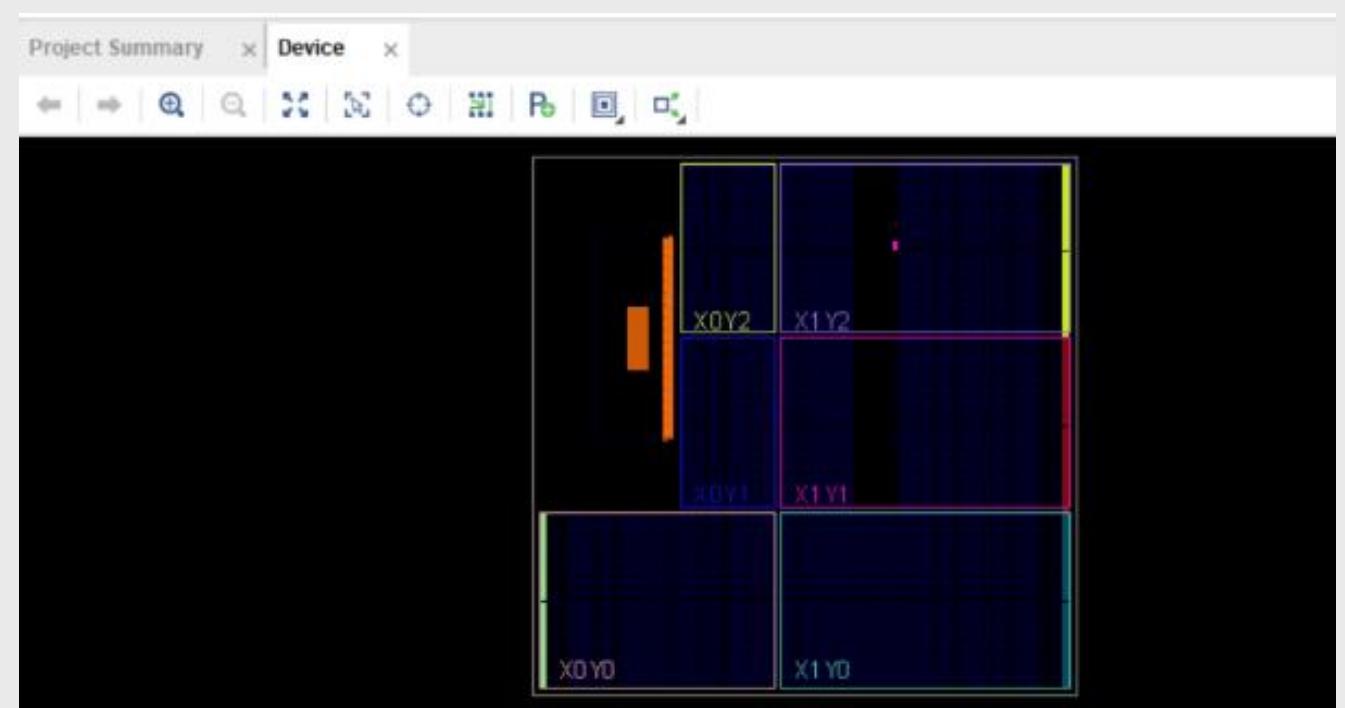
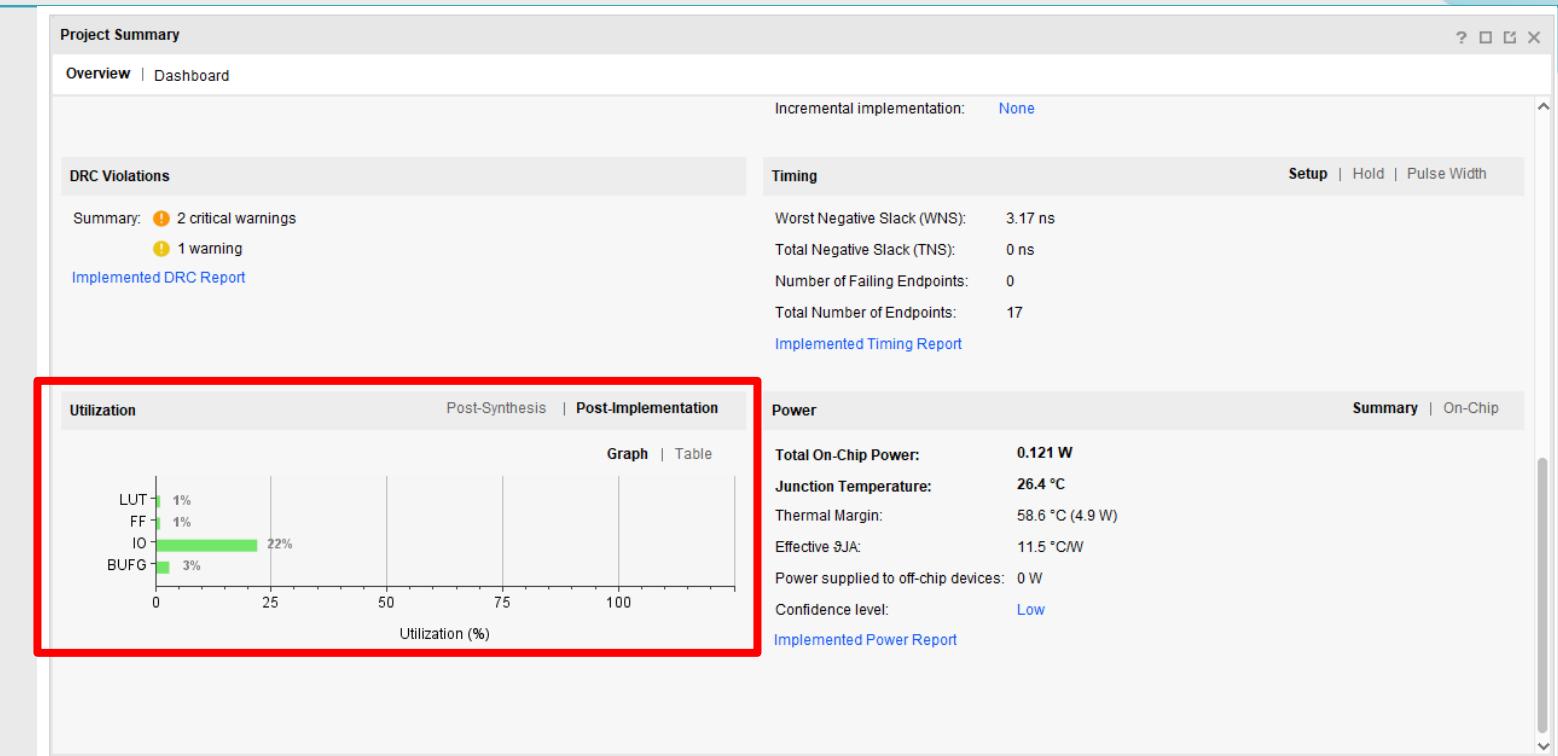


Outline

1. Download & Install
2. Setup License
3. Create Project
4. Setting Constraint
5. Xsim
6. **Synthesis & Implementation**
7. Summary

Synthesis & Implementation (1/3)

- ▼ IP INTEGRATOR
 - [Create Block Design](#)
 - [Open Block Design](#)
 - [Generate Block Design](#)
- ▼ SIMULATION
 - [Run Simulation](#)
- ▼ RTL ANALYSIS
 - > [Open Elaborated Design](#)
- ▼ SYNTHESIS
 - ▶ [Run Synthesis](#)
 - > [Open Synthesized Design](#)
- ▼ IMPLEMENTATION
 - ▶ [Run Implementation](#)
 - > [Open Implemented Design](#)



If you run implementation, vivado will ask you run synthesis first.

Synthesis & Implementation (2/3)

- If all of the value is black font, this means the implementation is successful.

| Tcl Console | Messages | Log | Reports | Design Runs | x | Timing | | | | | | | | | | | | | |
|--------------------|----------|-------------|---------|----------------------------|---|--------|-------|--------|-------|--------|-------|-------------|---------------|-----|----|-------|------|-----|--|
| | | | | | | | | | | | | | | | | | | | |
| Name | | Constraints | | Status | | | WNS | TNS | WHS | THS | TPWS | Total Power | Failed Routes | LUT | FF | BRAMs | URAM | DSP | |
| ✓ synth_1 (active) | | constrs_1 | | Synthesis Out-of-date | | | | | | | | | | 0 | 0 | 0.00 | 0 | 0 | |
| ✓ impl_1 | | constrs_1 | | Implementation Out-of-date | | | 6.902 | 0.0... | 0.037 | 0.0... | 0.000 | 0.665 | 0 | 40 | 0 | 1.00 | 0 | 0 | |

- If implementation didn't success, it will show error part in red font
- Please check if timing violation or area is exceeding the limit.

Synthesis & Implementation (3/3)

- Resource :
 1. LUT : Look-up table
Combinational circuit
 2. FF : Flip-Flop
Register of sequential circuit
 3. BRAM/LUTRAM : Memory
 4. DSP : Digital signal processor
Special arithmetic (multiplication, division, etc.)
 5. IO :
Bit number of IO port.
 6. BUFG :
Usually is used by clock source.

Outline

1. Download & Install
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Summary (1/3)

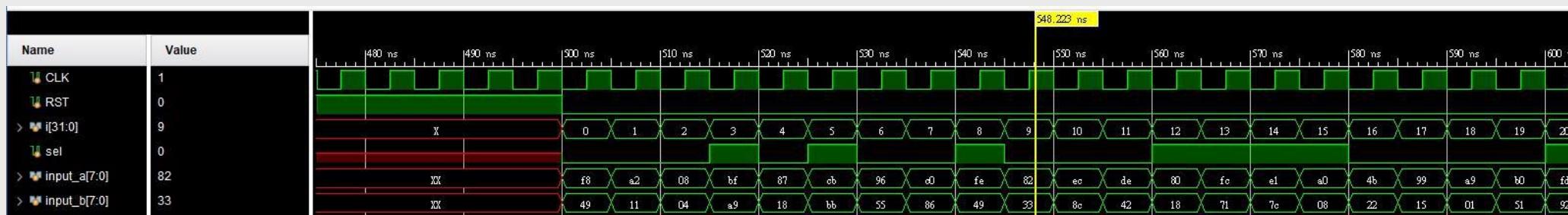
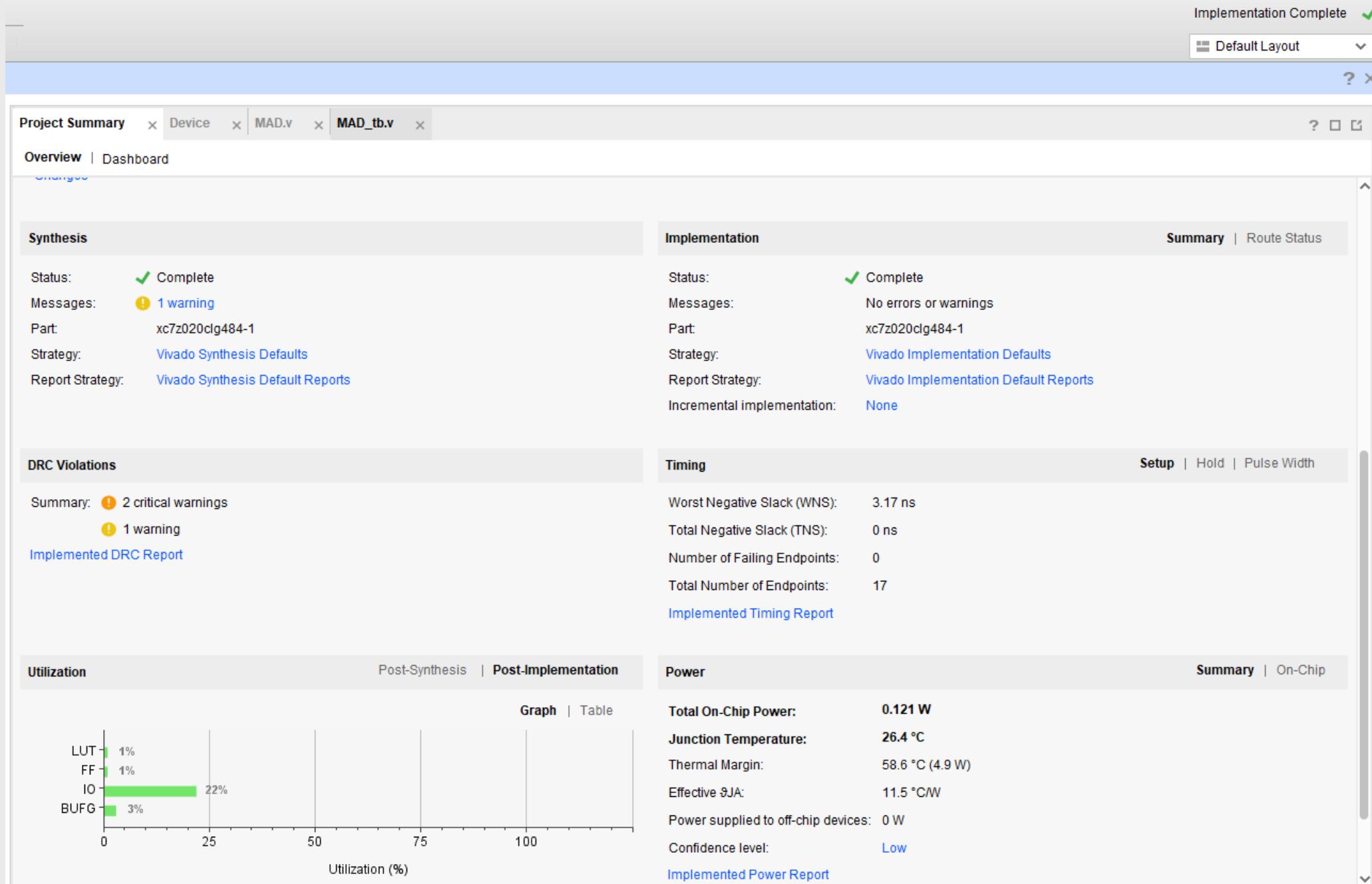
- FPGA Design Flow :
 1. Write Verilog
 2. Behavior Simulation
 3. Setting Constraint
 4. Synthesis
 5. Implementation
 6. Post-Implementation Functional simulation

Summary (2/3)

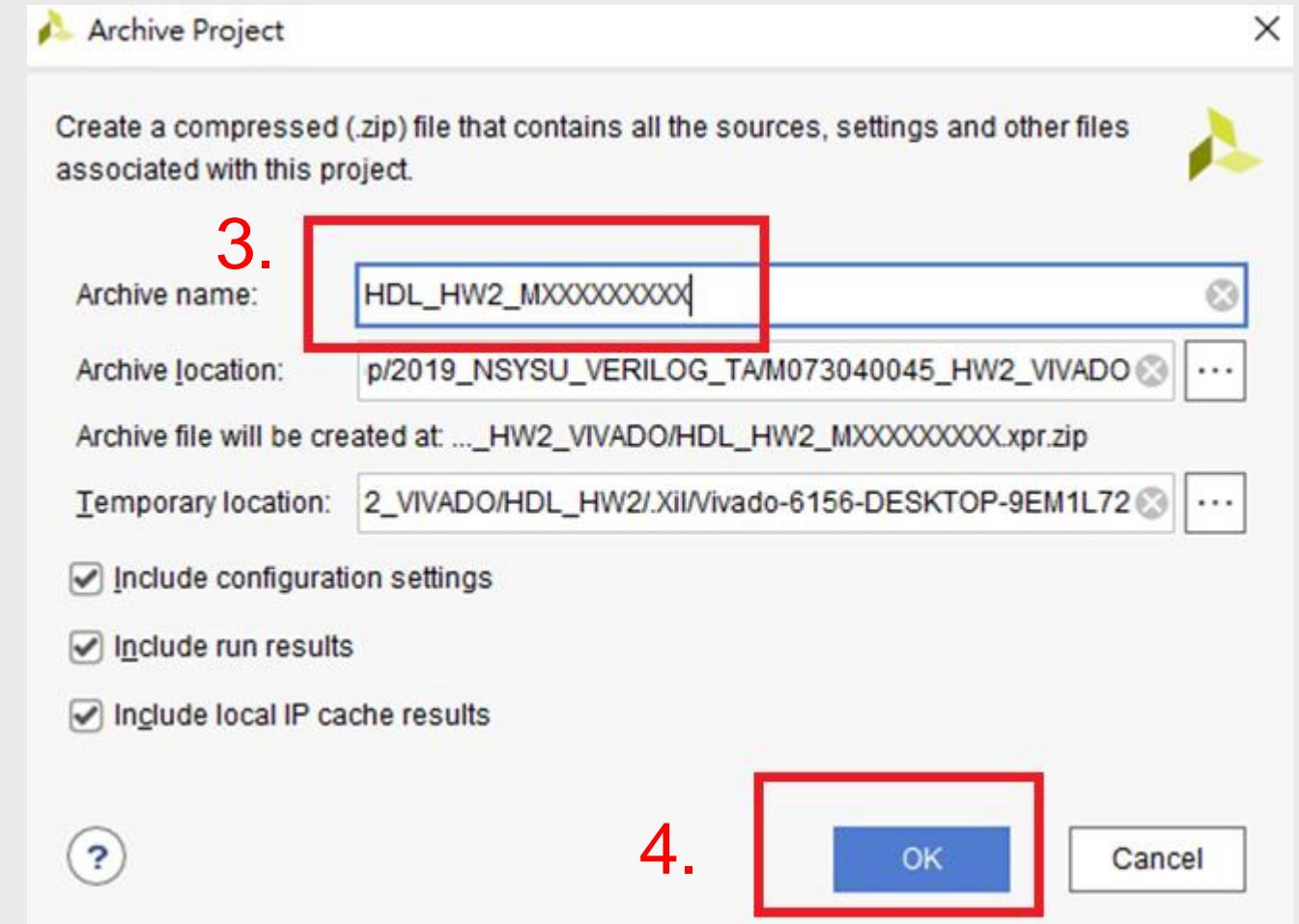
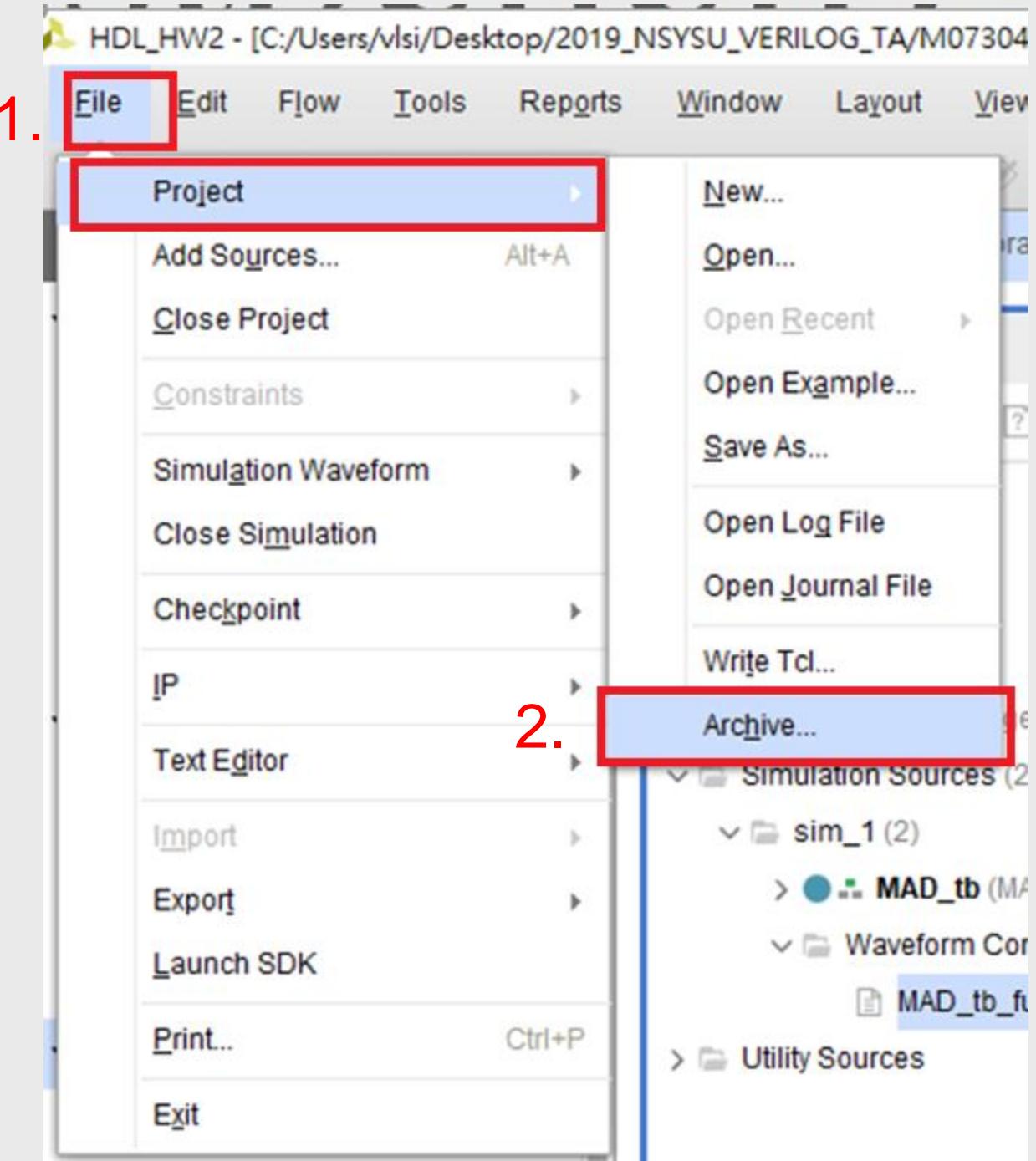
2. Design requirement :

- Clock frequency at 100MHz(Clock=10ns).
- No error and critical warning after running implementation.
- You have to check the warnings will not cause your design incorrect.

Summary (3/3)



匯出壓縮檔(.xpr.zip)



Project完成後，可如左圖流程直接產生壓縮檔。

在繳交vivado檔案時，請將vivado壓縮檔路徑裡的檔名.wdb刪除，以免檔案過大，其他同學無法上傳。
該路徑為 project名稱
(HDL_HWx_MXXXXXX).sim/sim_1/beav/xsim 以及
(HDL_HWx_MXXXXXX).sim/sim_1/impl/func /xsim
請確保壓縮檔裡的這兩個資料夾裡沒有.wdb檔。

整理檔案

整理成一包Vivado資料夾
放進Server HW2裡面一起繳交

Pipeline.xdc

Behavior.wcfg

post-imp.wcfg

.xpr.zip