Xilinx Vivado Tutorial

2025/10/13
EC5015-VLSILab

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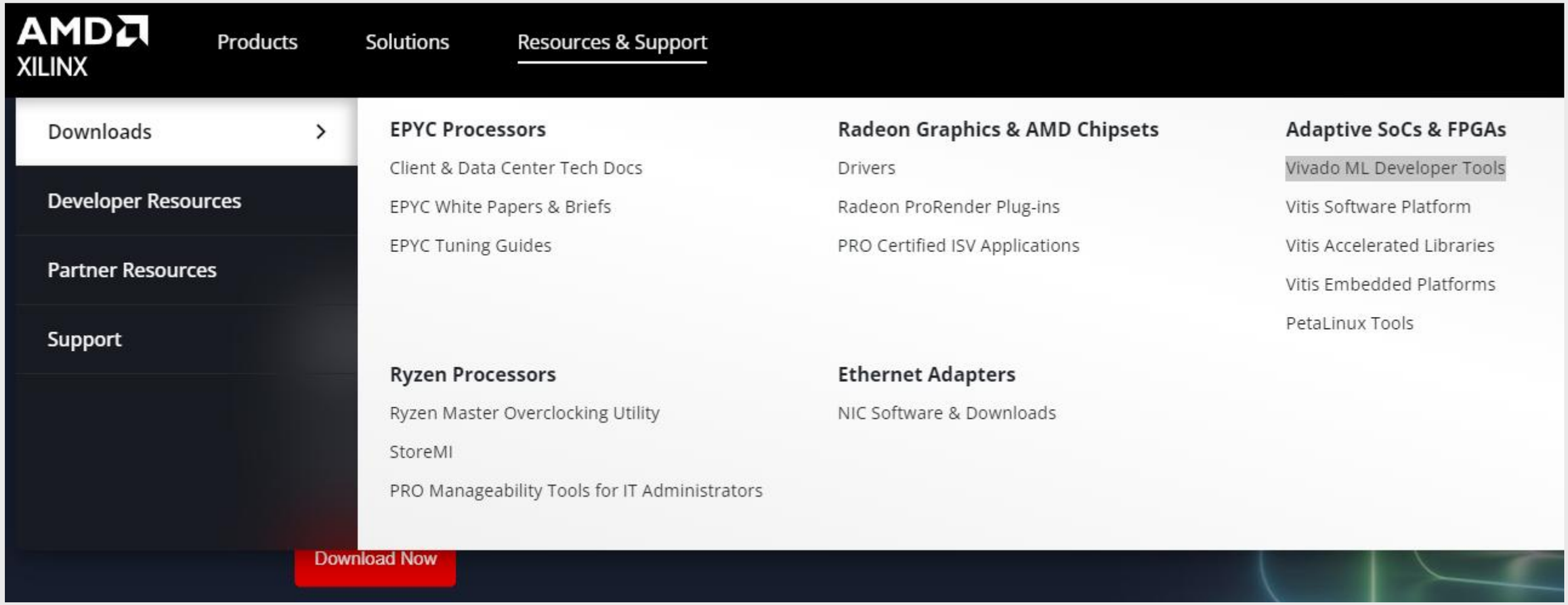
Outline

1. **Download & Install**
2. **Setup License**
3. **Create Project**
4. **Setting Constraint**
5. **Xsim**
6. **Synthesis & Implementation**
7. **Summary**

Download & Install (1/12)

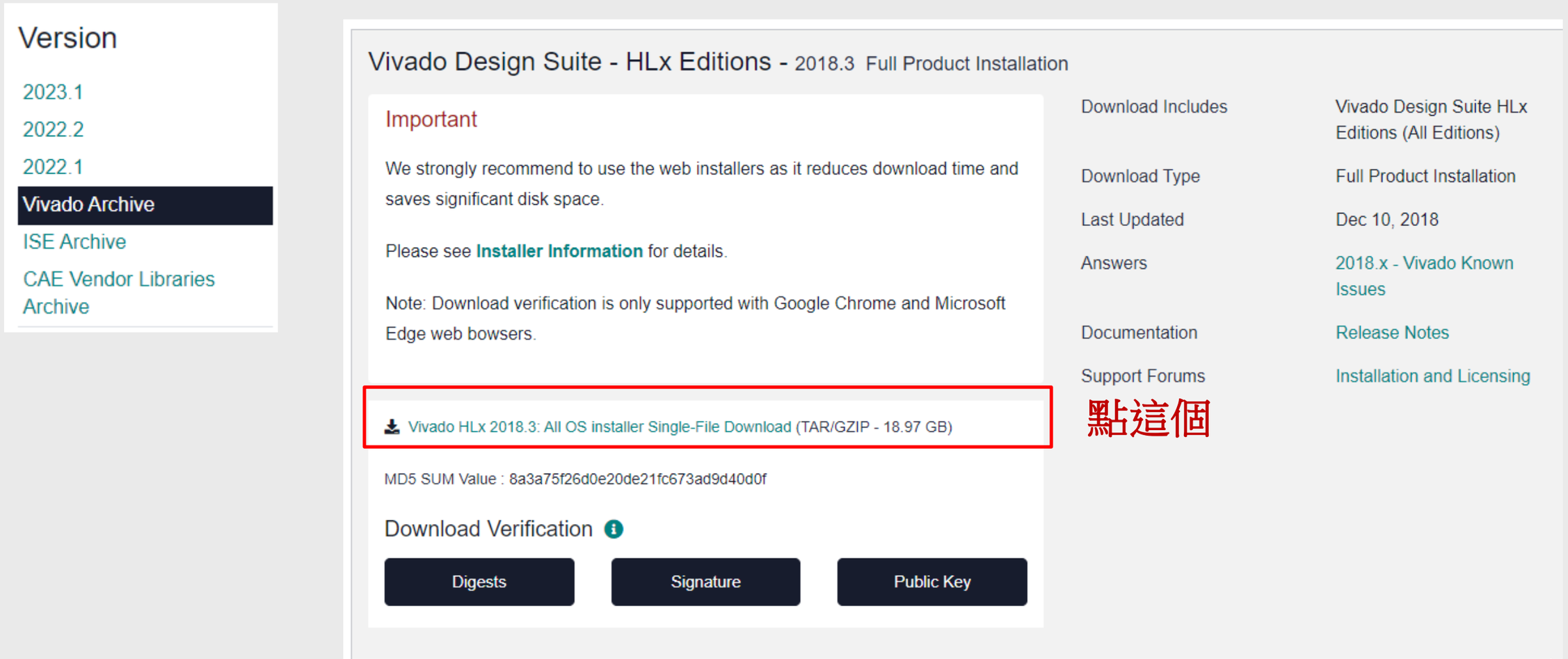
1. 連結至Xilinx官網 Website:
   https://www.xilinx.com/products/design-tools/vivado.html

2. Resources &Support->Downloads-> Vivado ML Developer Tools



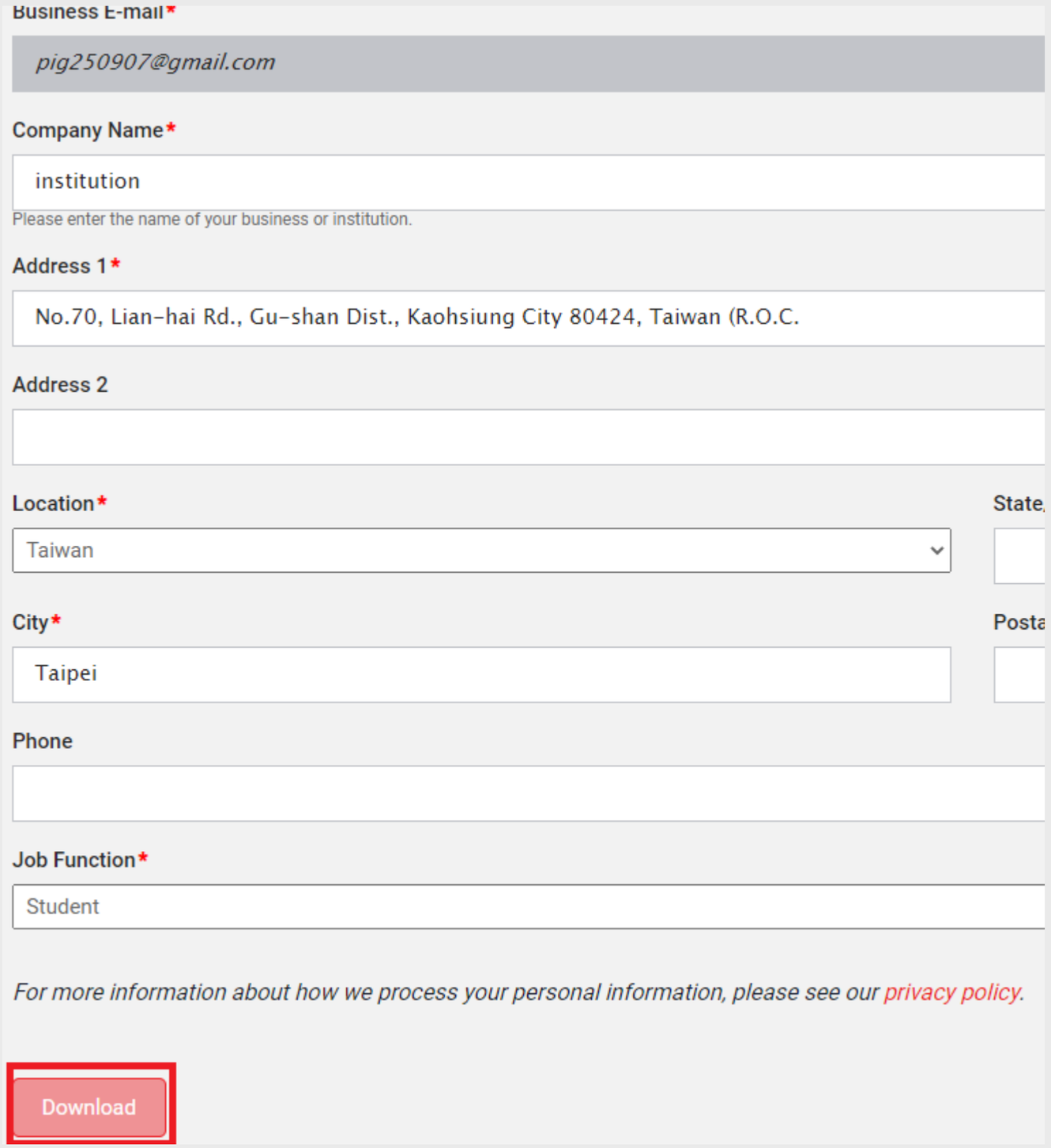
Download & Install (2/12)

3. 選擇Vivado Archive
4. 選擇2018.3並下載Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation裡的All OS installer Single-File Download



Download & Install (2/12)

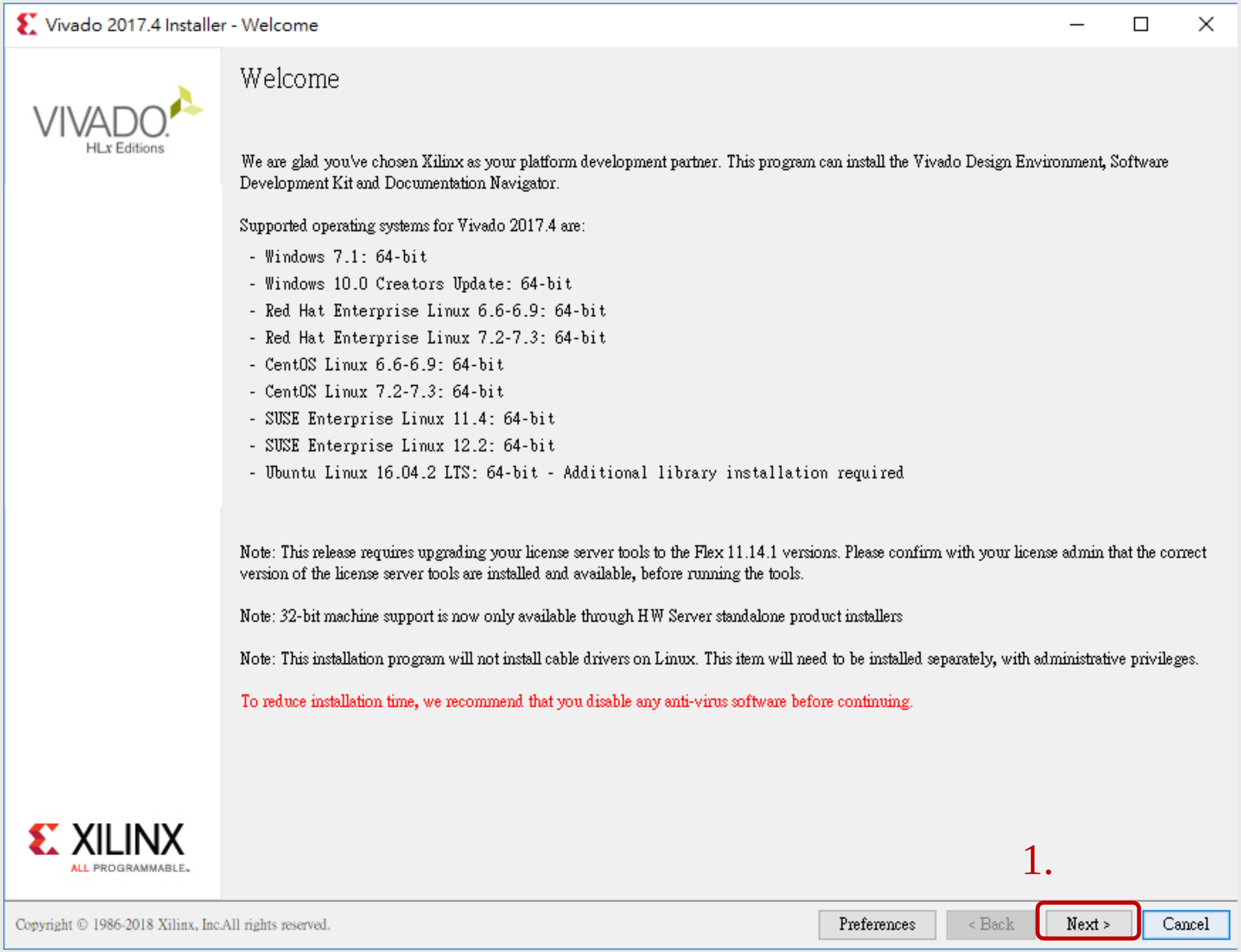
5. 註冊一個帳號，此帳號然後之後安裝會用到
6. 辦好後就能下載



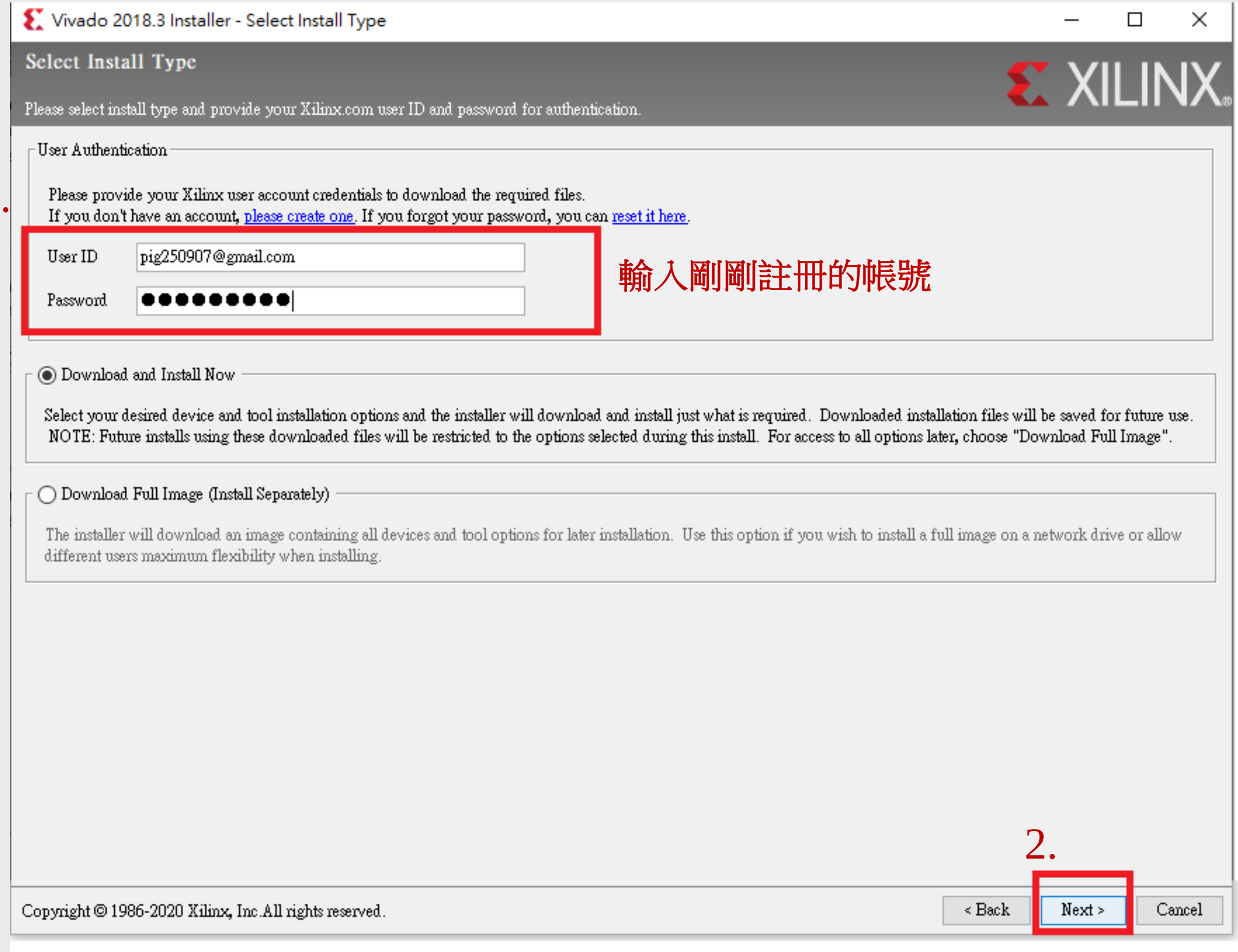
Download & Install (3/12)

1. Exunzip vivado.
2. execute installer
   - Windows：
     A. Go to folder of vivado
     B. Double-Click xsetup.exe
   - Linux：
     A. Open terminal
     B. cd <path to folder of vivado>
     C. sudo ./xsetup

Download & Install (4/12)



Download & Install (5/12)

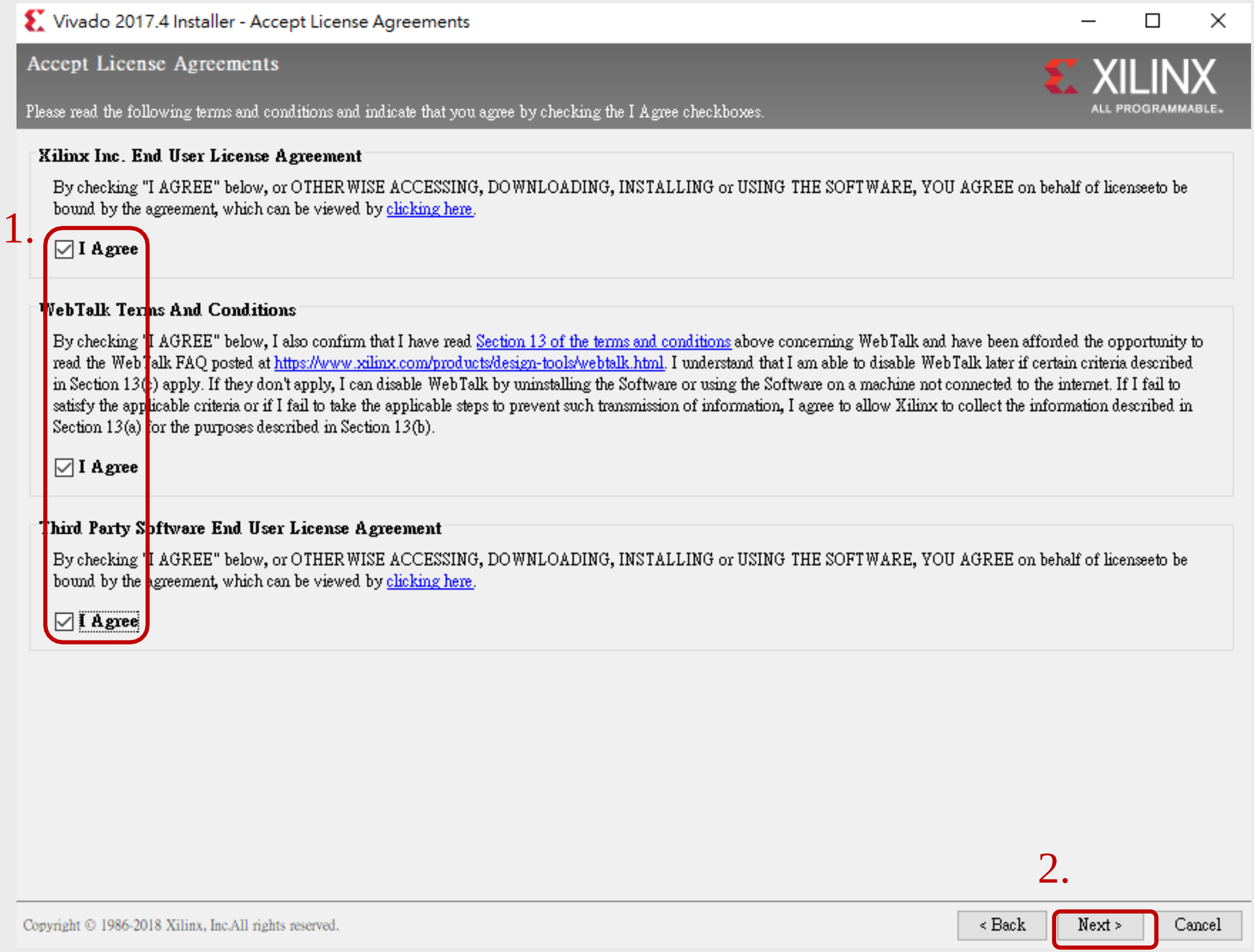


1.

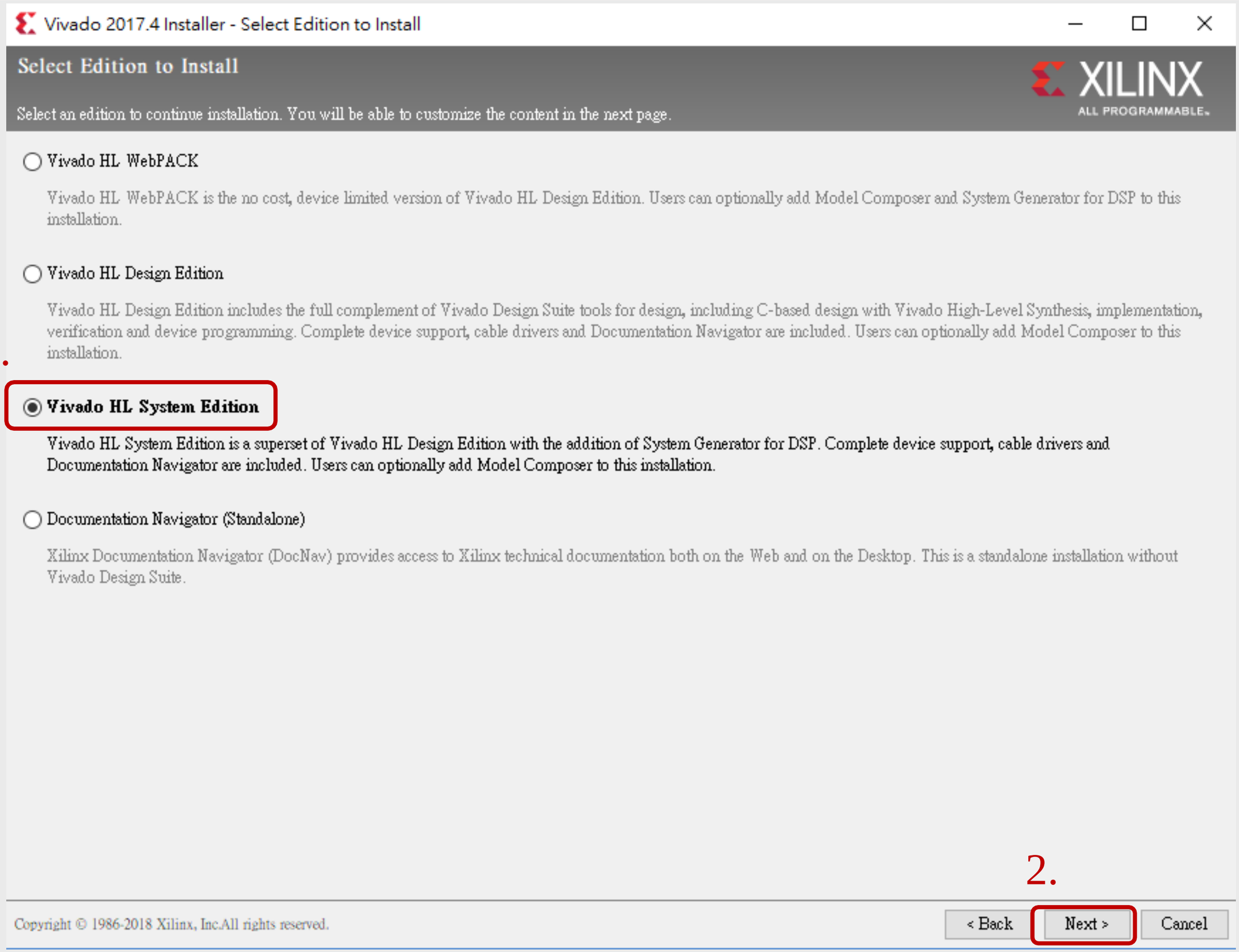
輸入剛剛註冊的帳號

2.

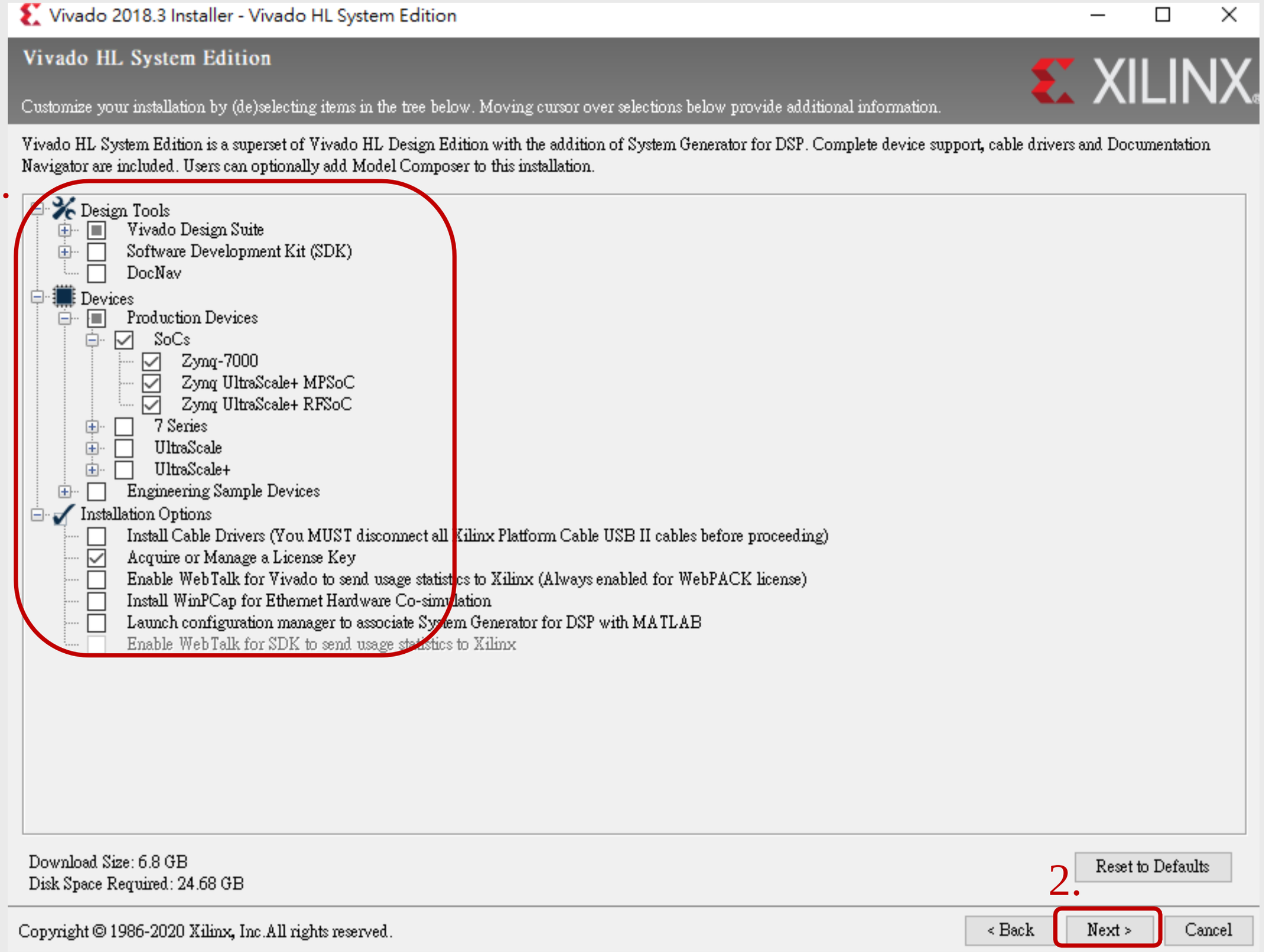
Download & Install (5/12)



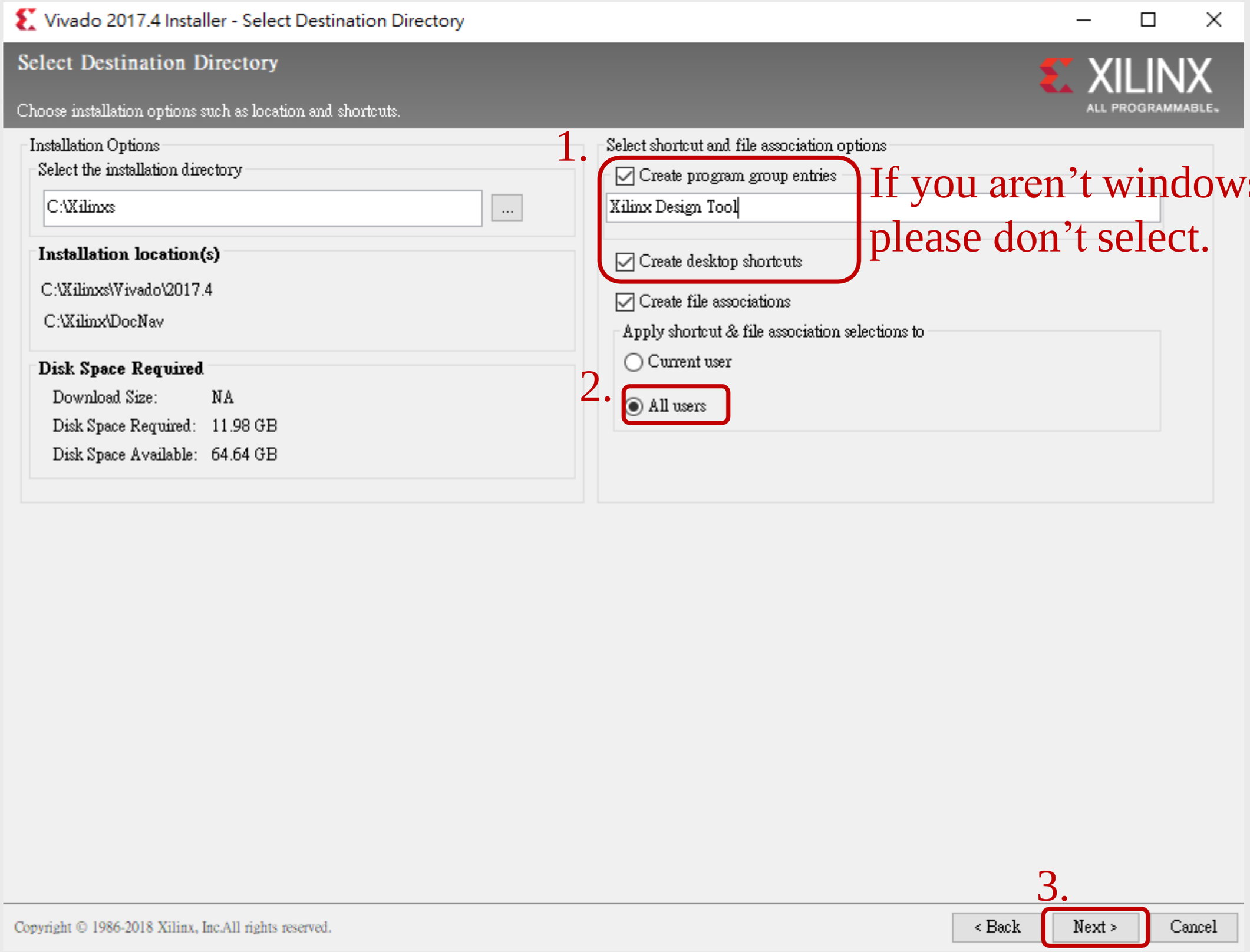
Download & Install (6/12)



Download & Install (7/12)

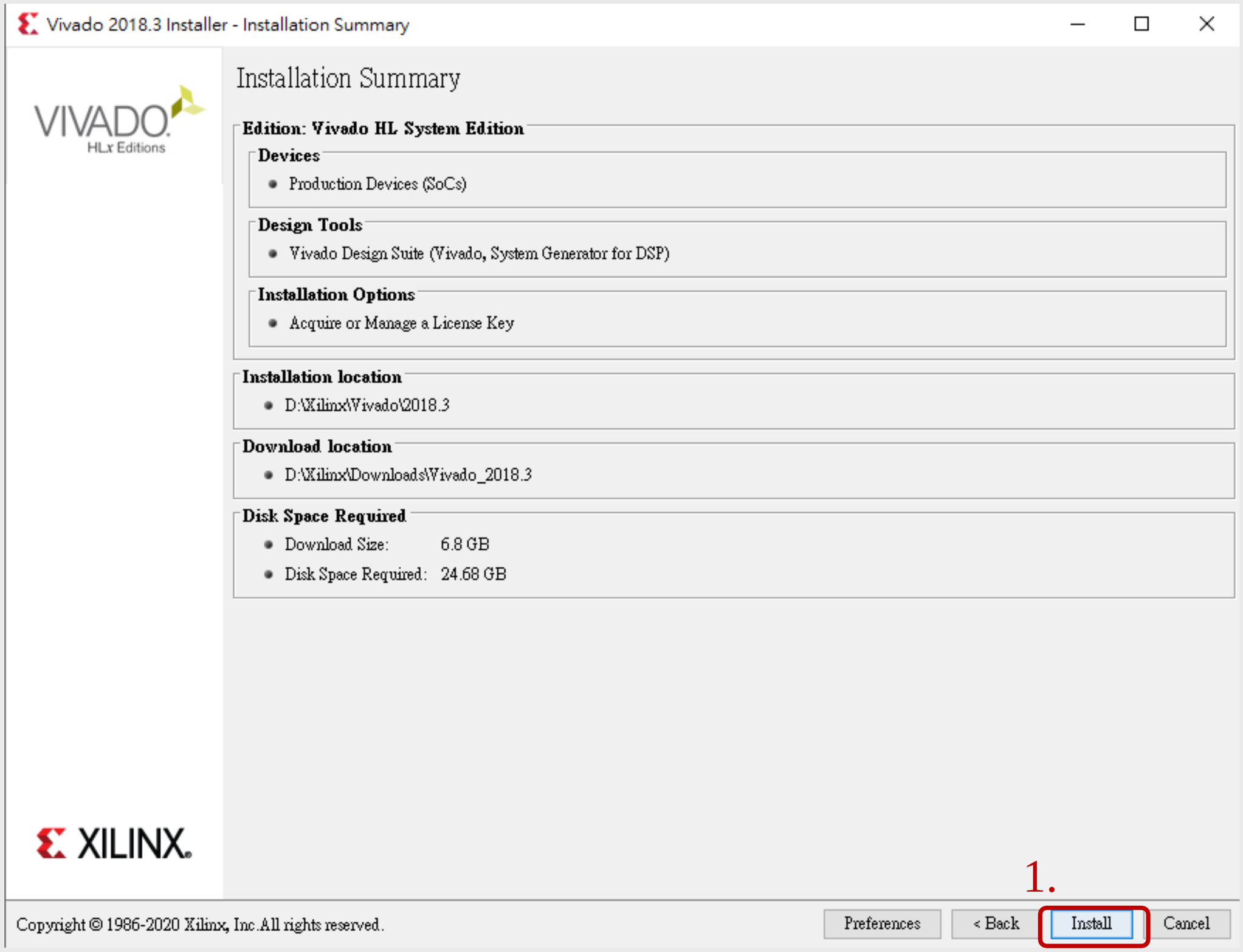


Download & Install (8/12)



Download & Install (9/12)

- 如安裝完成後遇到License，可先至18頁設定。



Download & Install (10/12) (Linux Only)

If you use Linux, you need to set environment variable.

1. Open terminal
2. cd ~
3. gedit ./.bashrc
4. Paste the following code to blank position
   - source <path to vivado>/settings64.sh
5. Save & Exit

Download & Install (11/11)

After installing vivado, you can open vivado by following：

1. Window：
   - Double-Click the icon 

2. Linux：
   A. Open terminal
   B. vivado &

Outline

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3. **Create Project**
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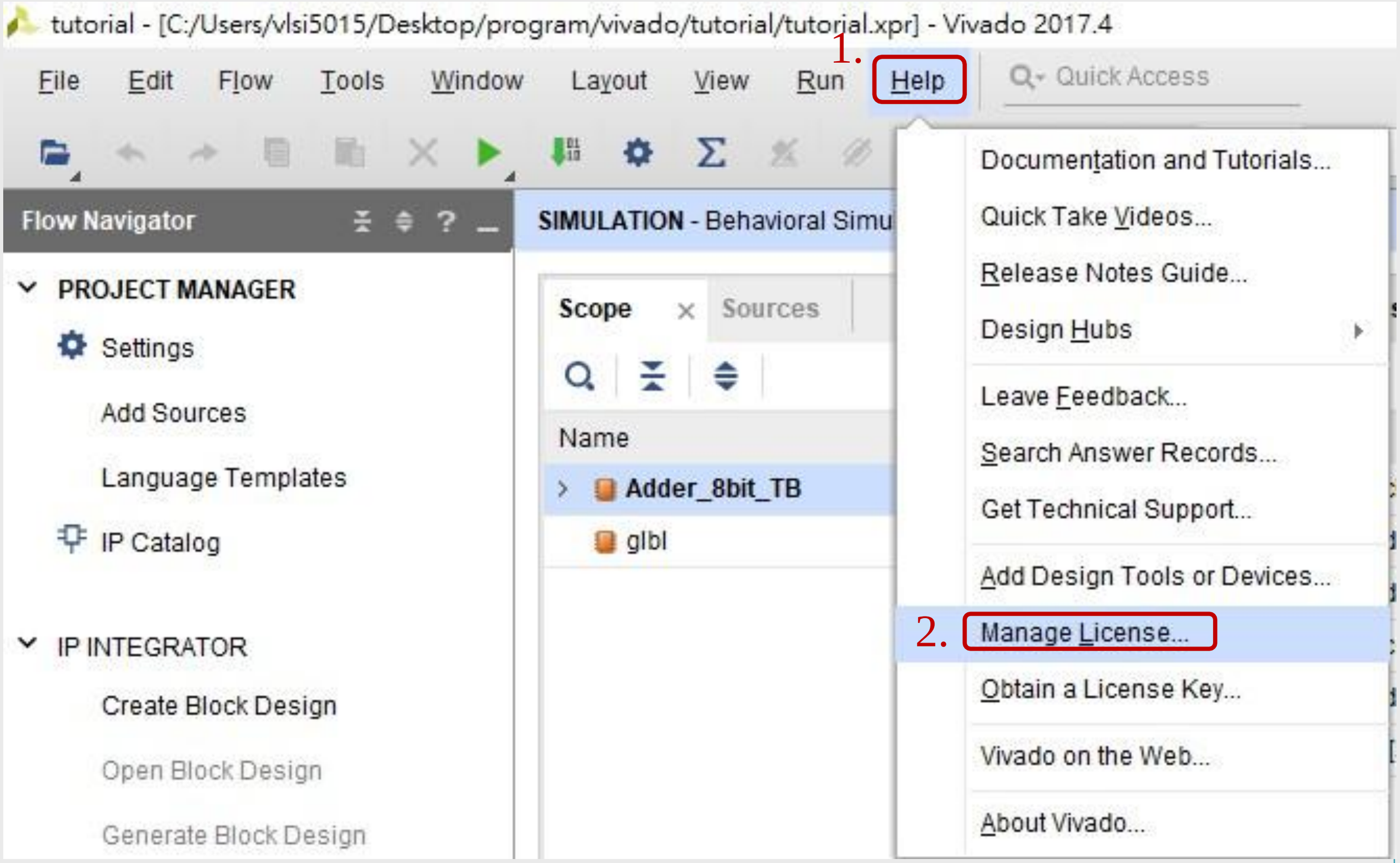
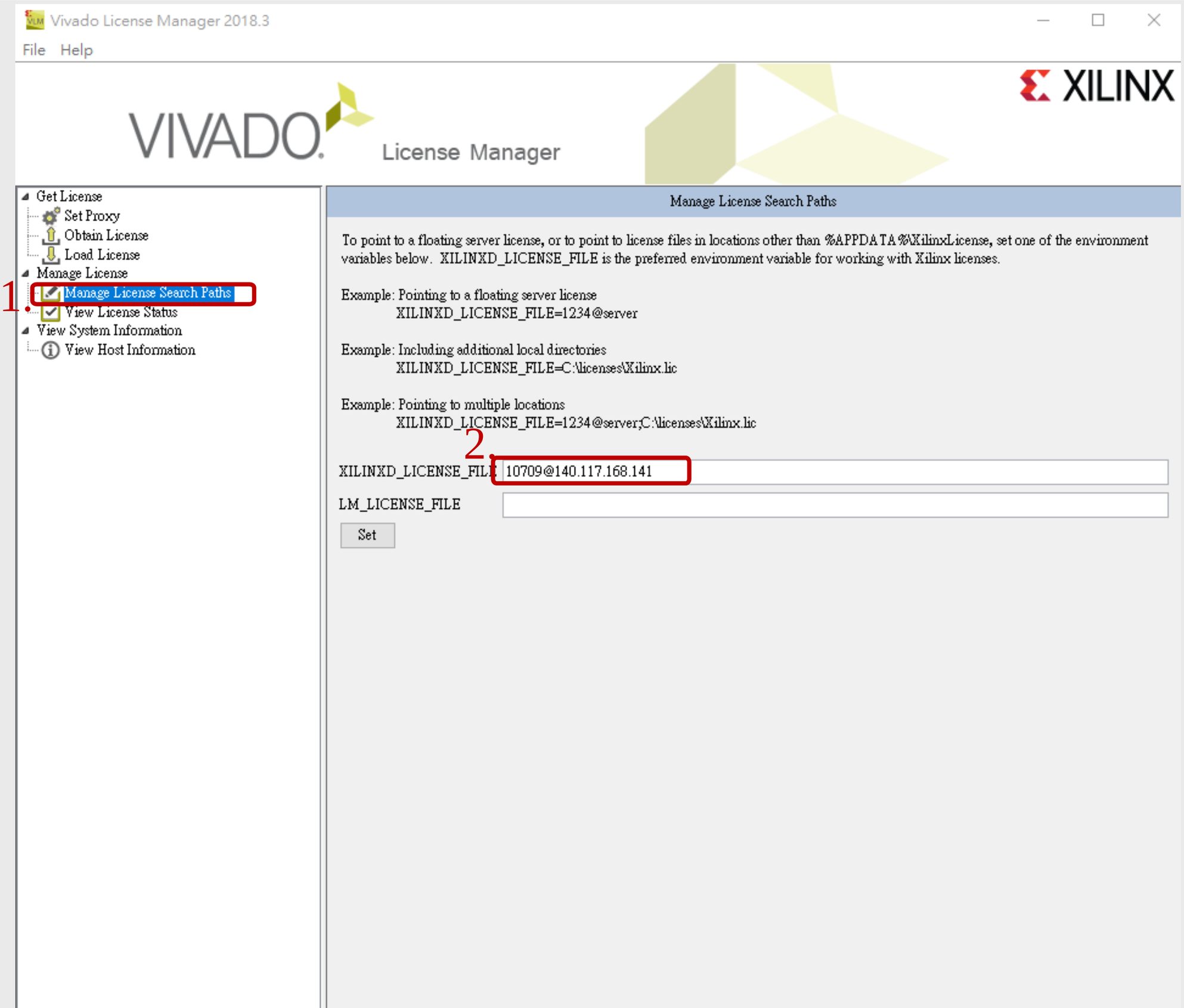
Setup License (1/4)



Setup License (2/4) (Windows)



Setup License (3/4) (Linux)

1. Open terminal
2. cd ~
3. gedit ./.bashrc
4. Paste the following code to blank position
   - export XILINXD_LICENSE_FILE=10709@140.117.168.141
5. Save & Exit

Setup License (4/4)

Vivado License Manager 2017.4

File Help

VIVADO License Manager

XILINX ALL PROGRAMMABLE

- Get License
  - Set Proxy
  - Obtain License
  - Load License
- Manage License
  - Manage License Search Paths
  - View License Status
- View System Information
  - View Host Information

1.

View License Status

2.

Filter: Hide Free Built-in Licenses

Certificate Based Licenses:

License Name	Tools/IP	Expiration Date	Version Limit	License Type	Location	#
PartialReconfiguration	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
PartialReconfiguration	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
PlanAhead	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
SDK	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
SDK	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
SDSoC_Tools	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
Simulation	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
Simulation	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
Synthesis	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
SysGen	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
Vivado_System_Edition	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur
XC7Z010	Tools	Permanent	2019.03	Nodelocked	C:\Users\wlsi5015\AppD...	Ur

Activation Based Licenses:

NOTE: Support for activation based licenses has been deprecated. Your existing activation licenses have been replaced with certificate based licenses and added into your licensing account.

License Name	Tools/IP	Expiration Date	Version Limit	Server/Client	Location	# of S

3.If you set license successfully, you will see a lot of items in this field.

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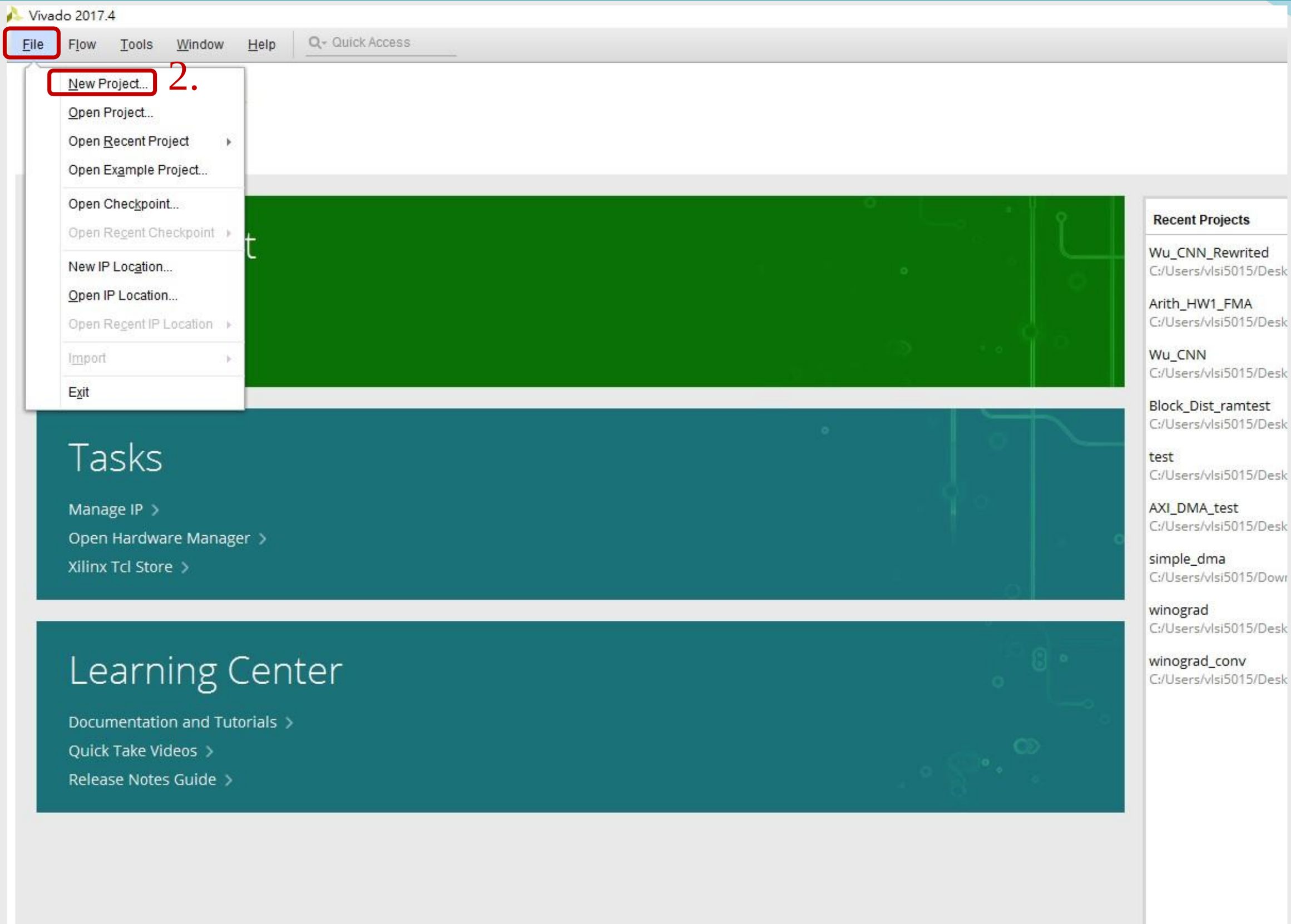
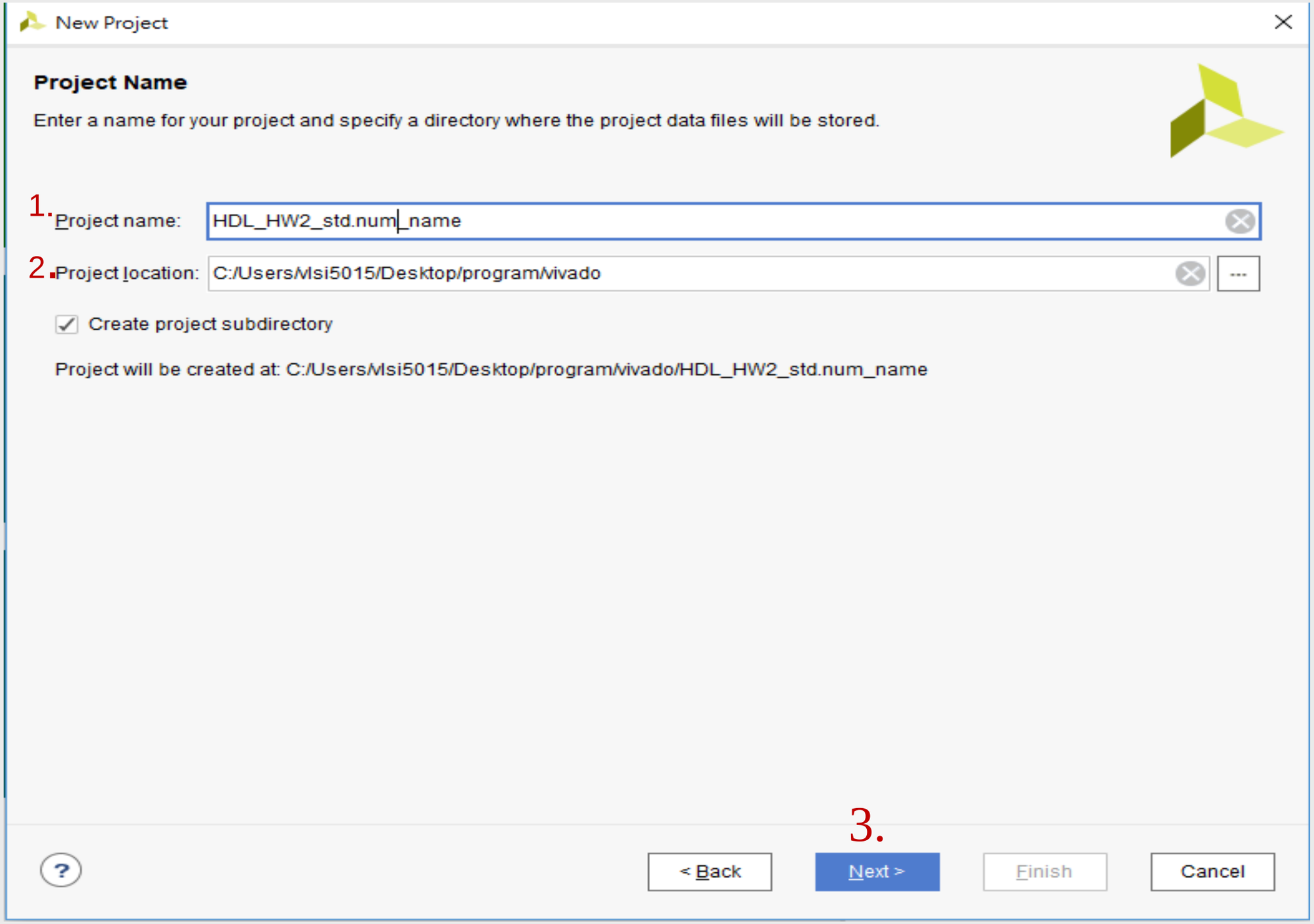
Create Project (1/8)

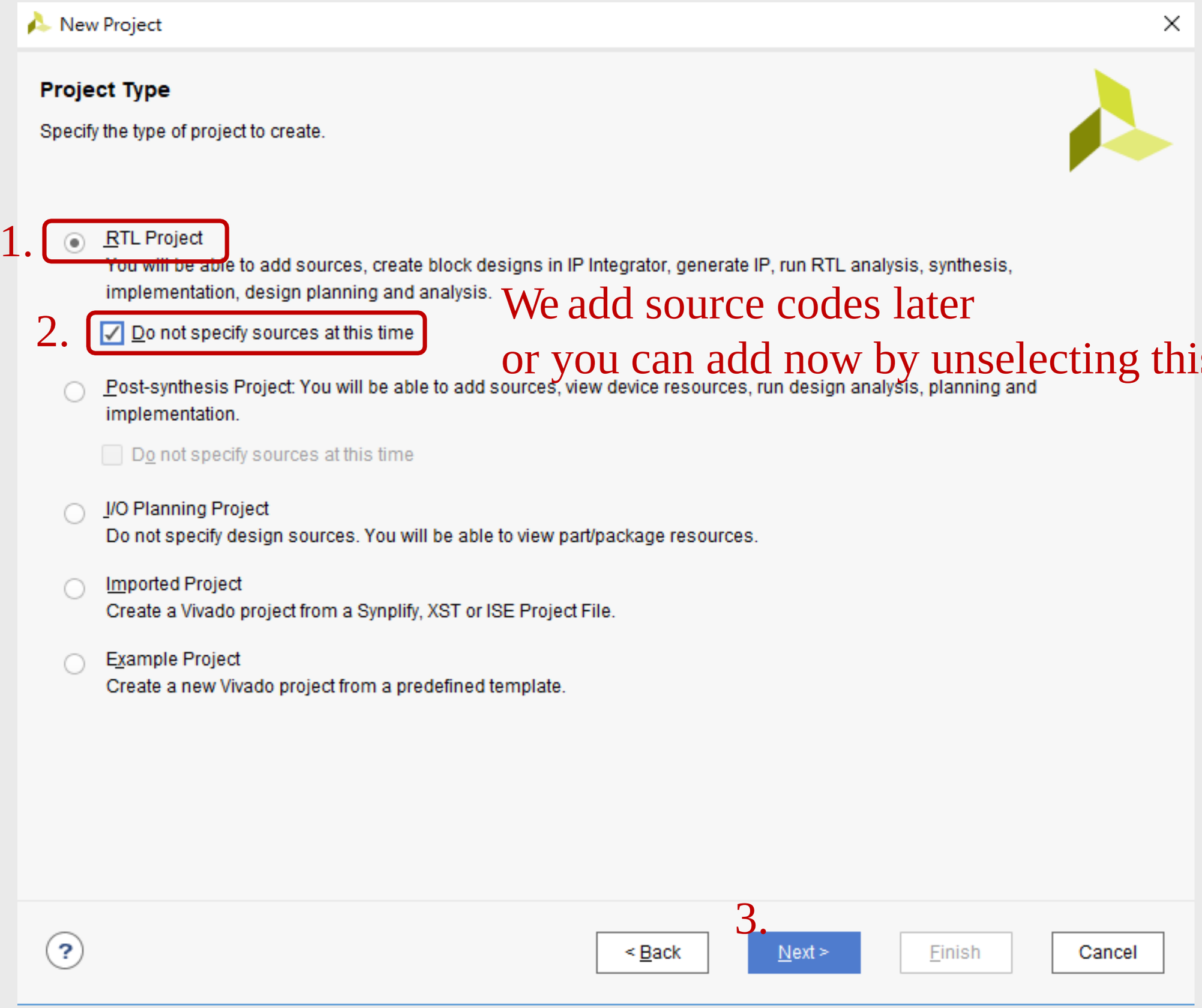
1.



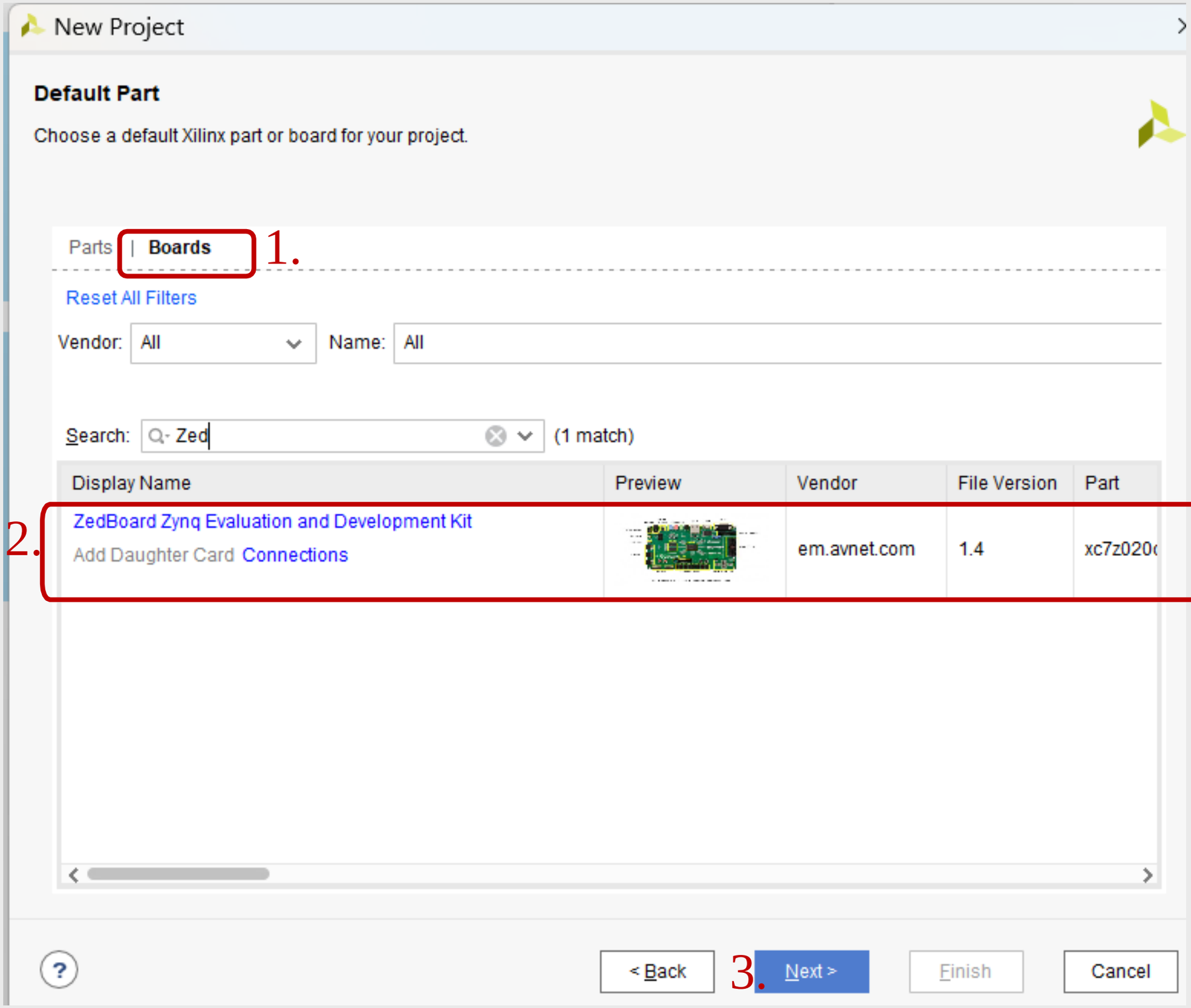
Create Project (2/8)



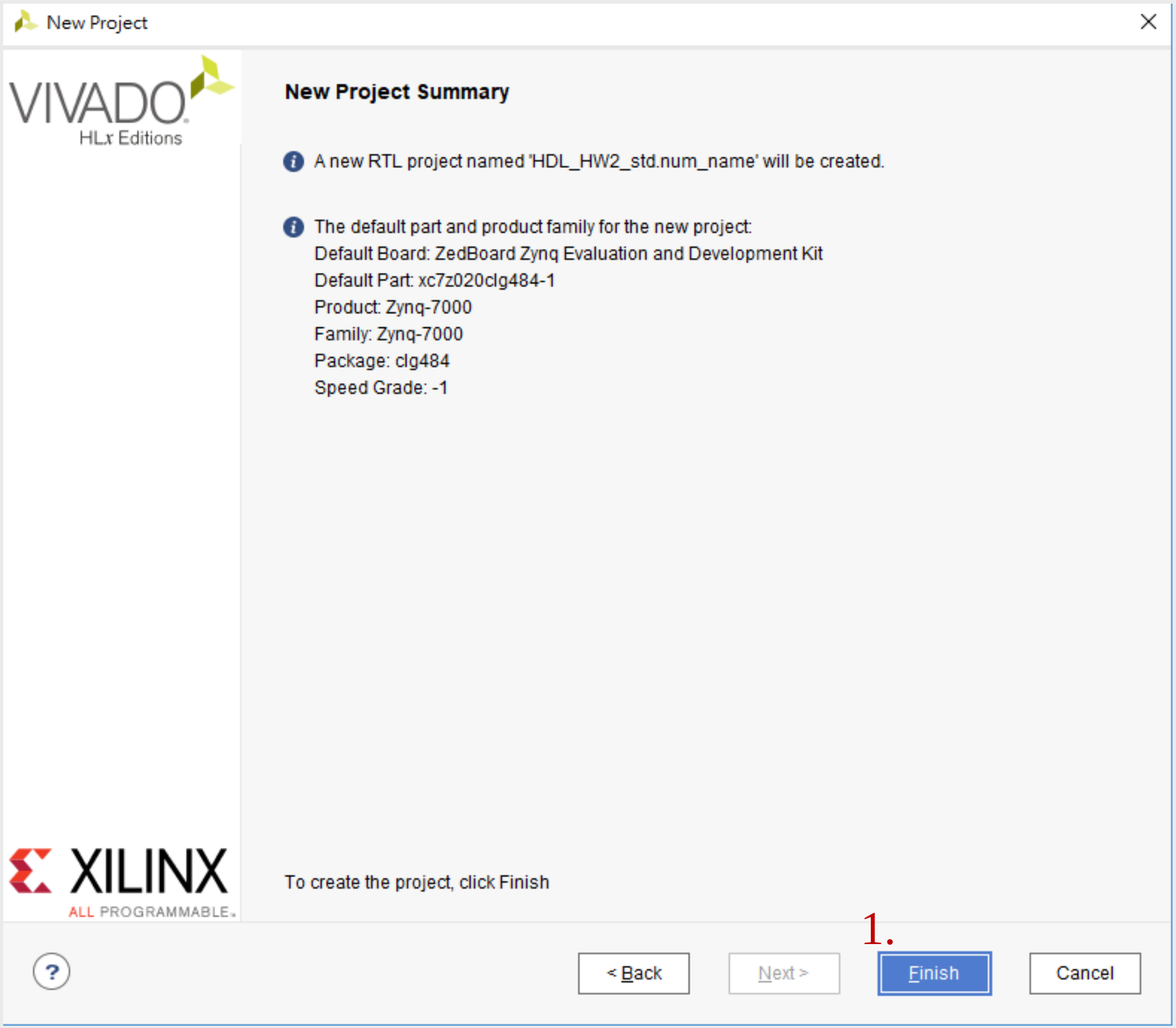
Create Project (3/8)



Create Project (4/8)



Create Project (5/8)



Create Project (6/8)

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator

PROJECT MANAGER
- Settings
- 1. Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - tutorial

Sources

- Design Sources
- Constraints
- Simulation Sources
  - sim_1

Hierarchy | Libraries | Compile Order

Properties

Select an object to see properties

Project Summary

Settings Edit

Project name:	tutorial
Project location:	C:/Users/Msi5015/Desktop/program/vivado/tutorial
Product family:	Zynq-7000
Project part:	ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)
Top module name:	Not defined
Target language:	Verilog
Simulator language:	Mixed

Board Part

Display name:	ZedBoard Zynq Evaluation and Development Kit
Board part name:	em.avnet.com:zed:part0:1.3
Connectors:	
Repository path:	C:/Xilinx/Vivado/2017.4/data/boards/board_files
URL:	http://www.zedboard.org
Board overview:	ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status:	Not started
Messages:	No errors or warnings

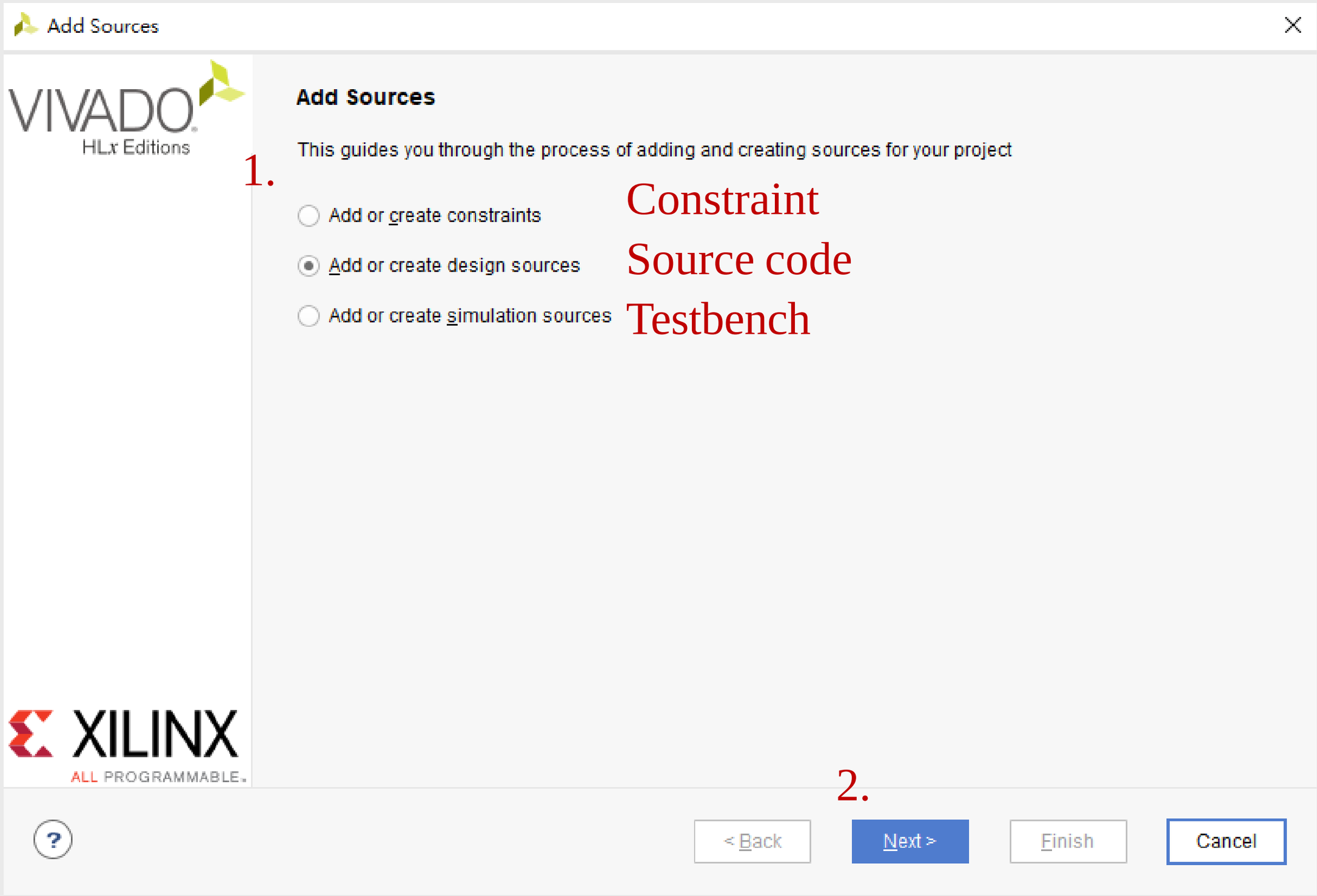
Implementation

Status:	
Messages:	

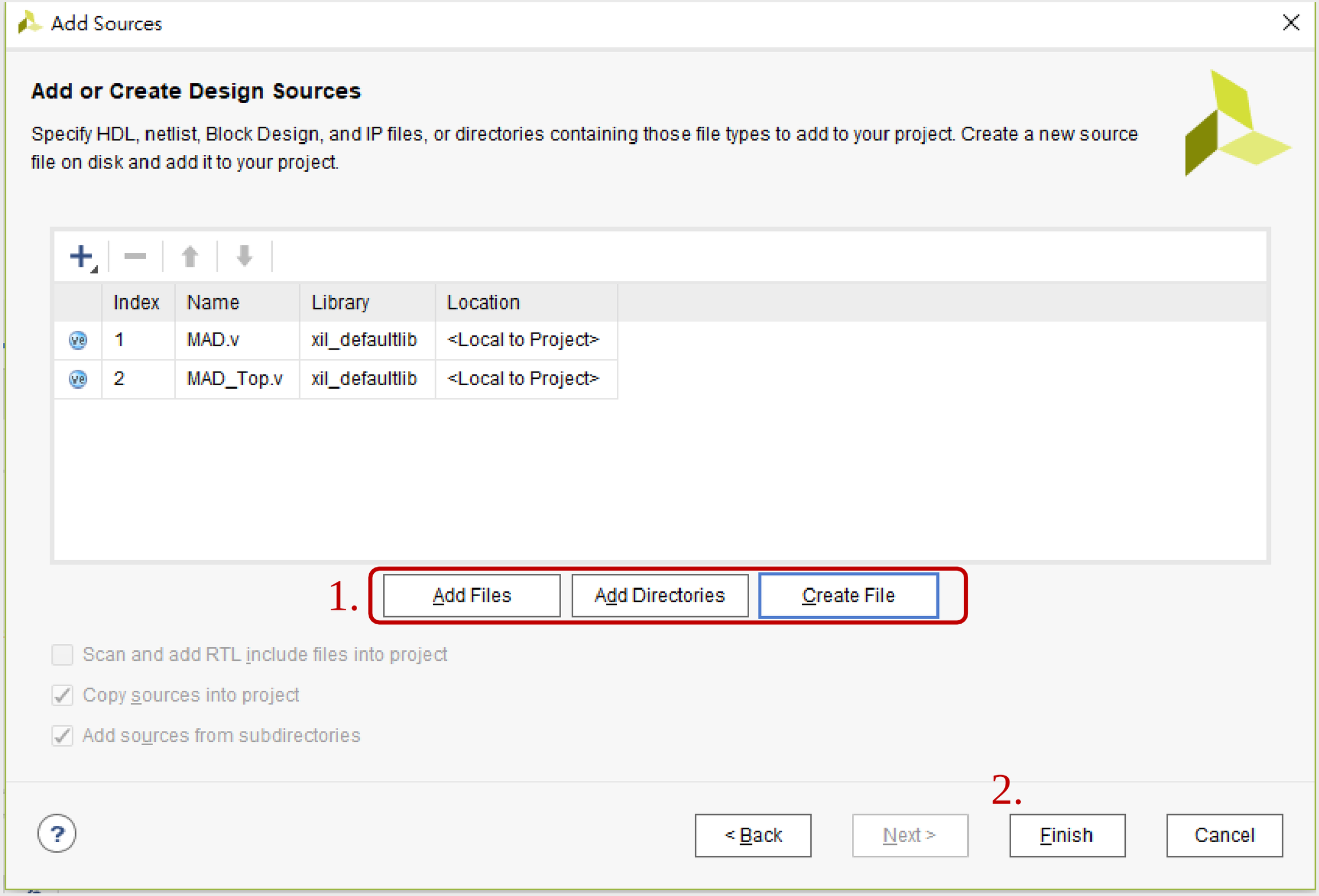
Tcl Console | Messages | Log | Reports | Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synth
impl_1	constrs_1	Not started															Vivado Imple

Create Project (7/8)



Create Project (8/8)



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Setting Constraint (1/5)

1. All you have to do is setting clock frequency, because the homework only asks you complete running implementation

2. There are two ways to set timing constraint

   A. Create .xdc file and write constraint.

   B. Use GUI

Setting Constraint (2/5) (.xdc)

1. Create xdc file.

2. Write the below constraint to .xdc file.

   create_clock -period 10.000 -name clk -waveform {0.000 5.000}

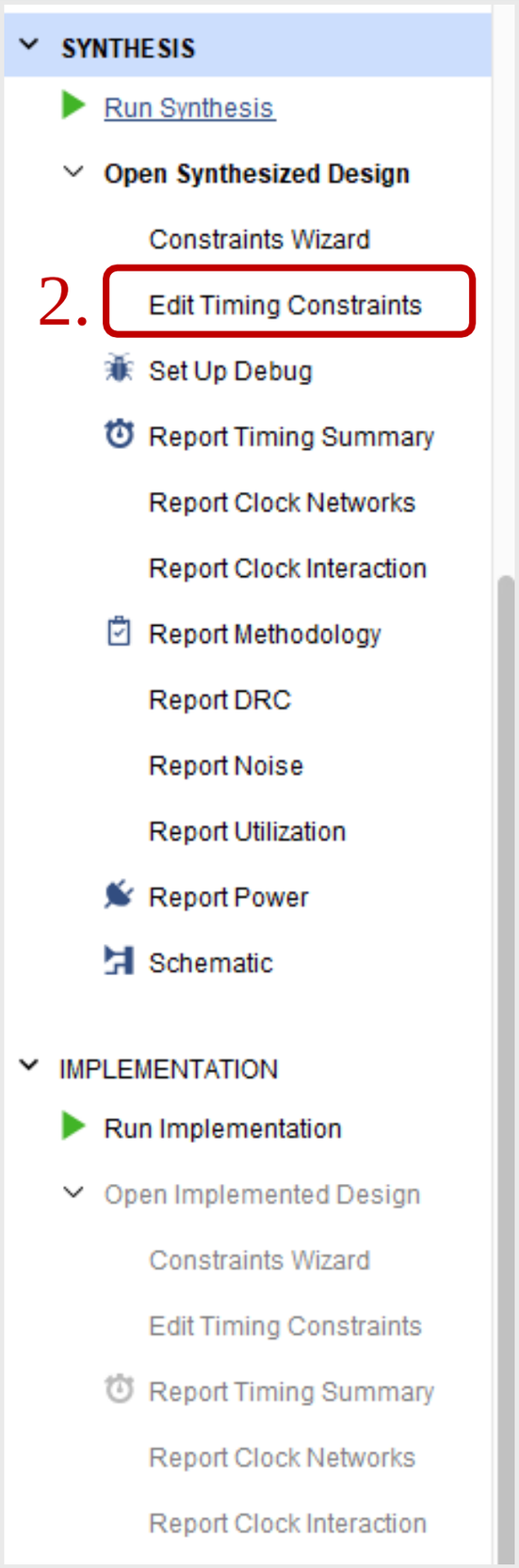
   [get_ports clk]

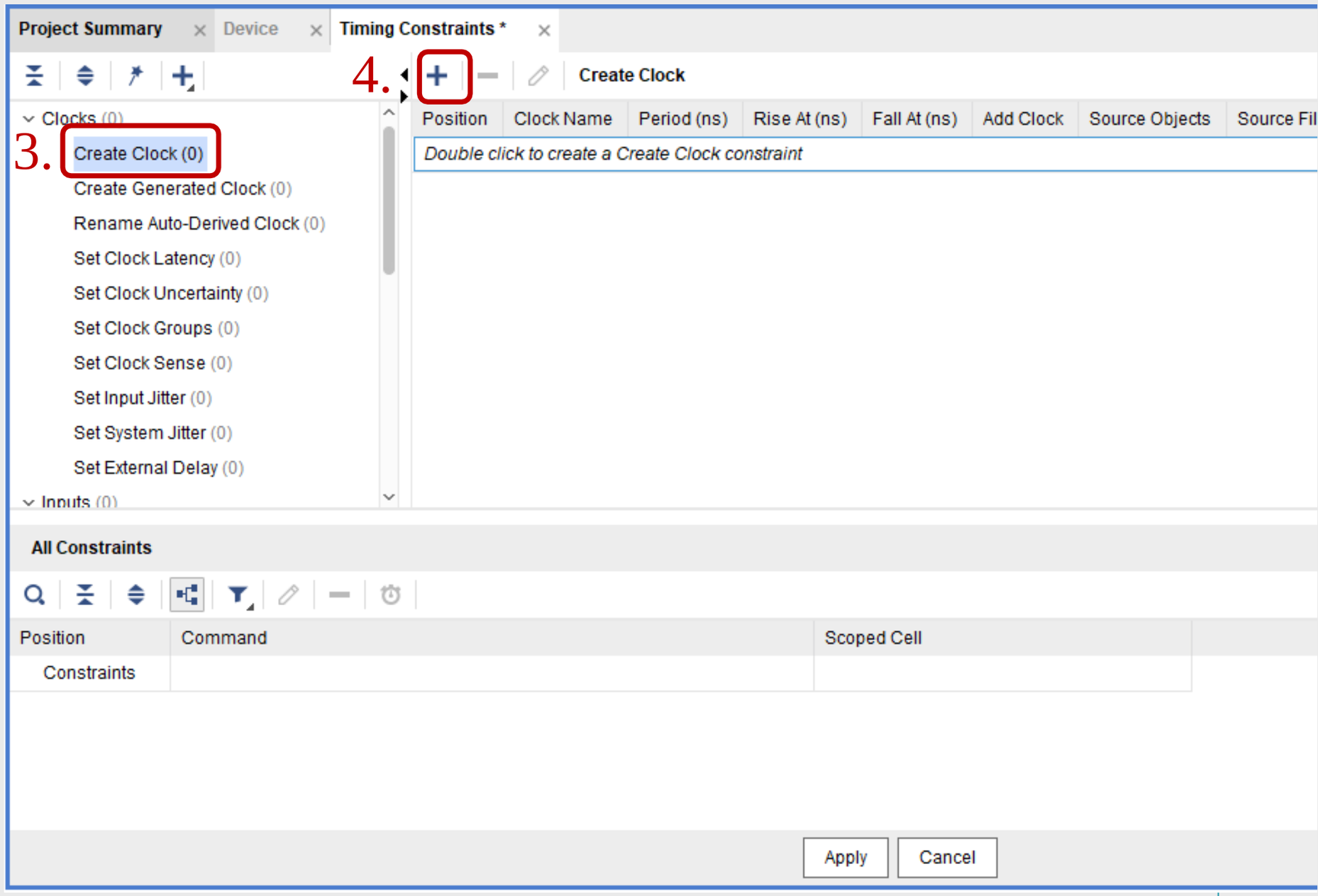
3. Explain：

   1. Create_clock : Create an independent clock source signal
   2. {0.000 5.000} : posedge at 0.0ns, negedge at 5.0ns
   3. [get_ports clk] : Send clock signal to clk of Verilog’s input port

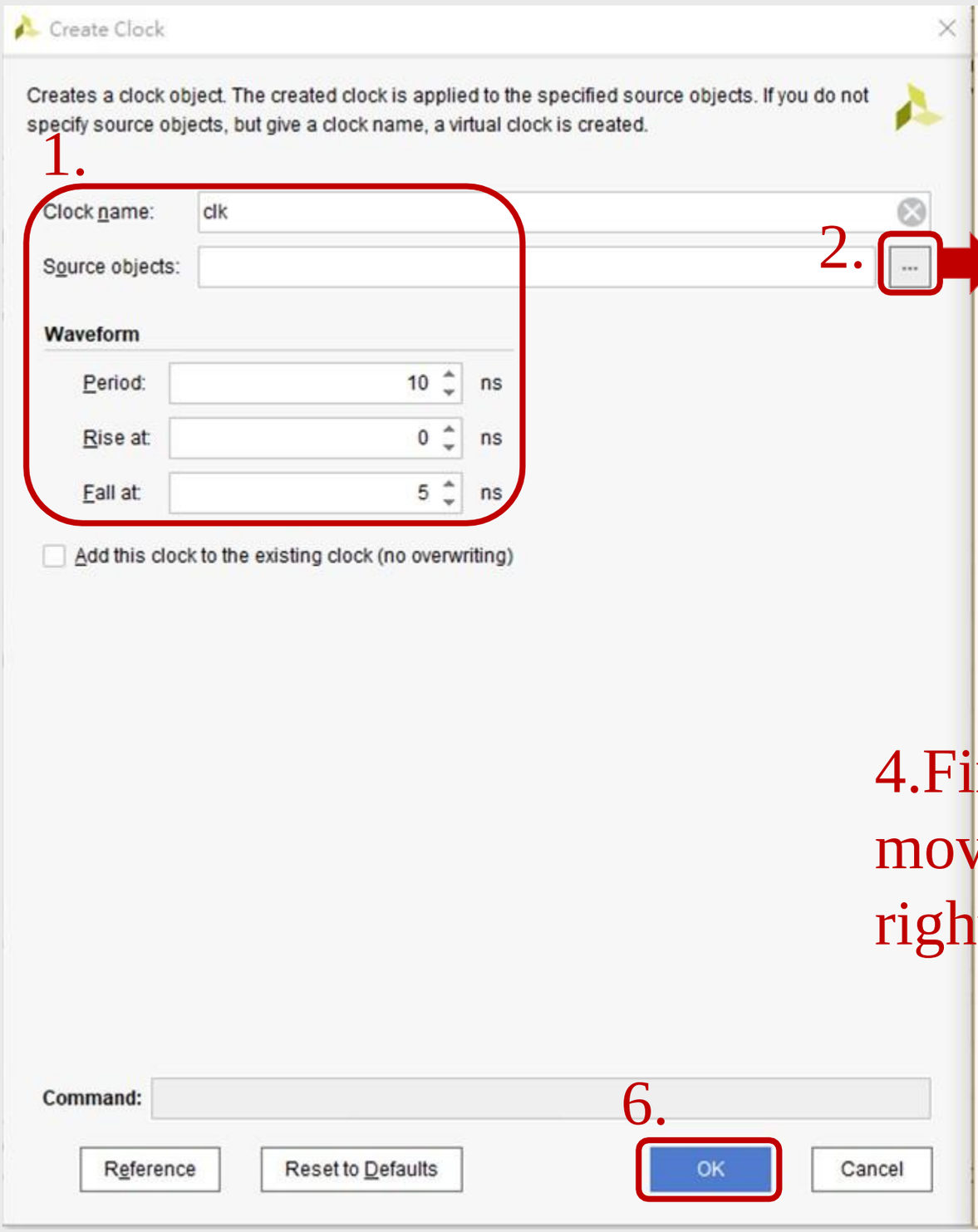
Setting Constraint (3/5) (GUI)

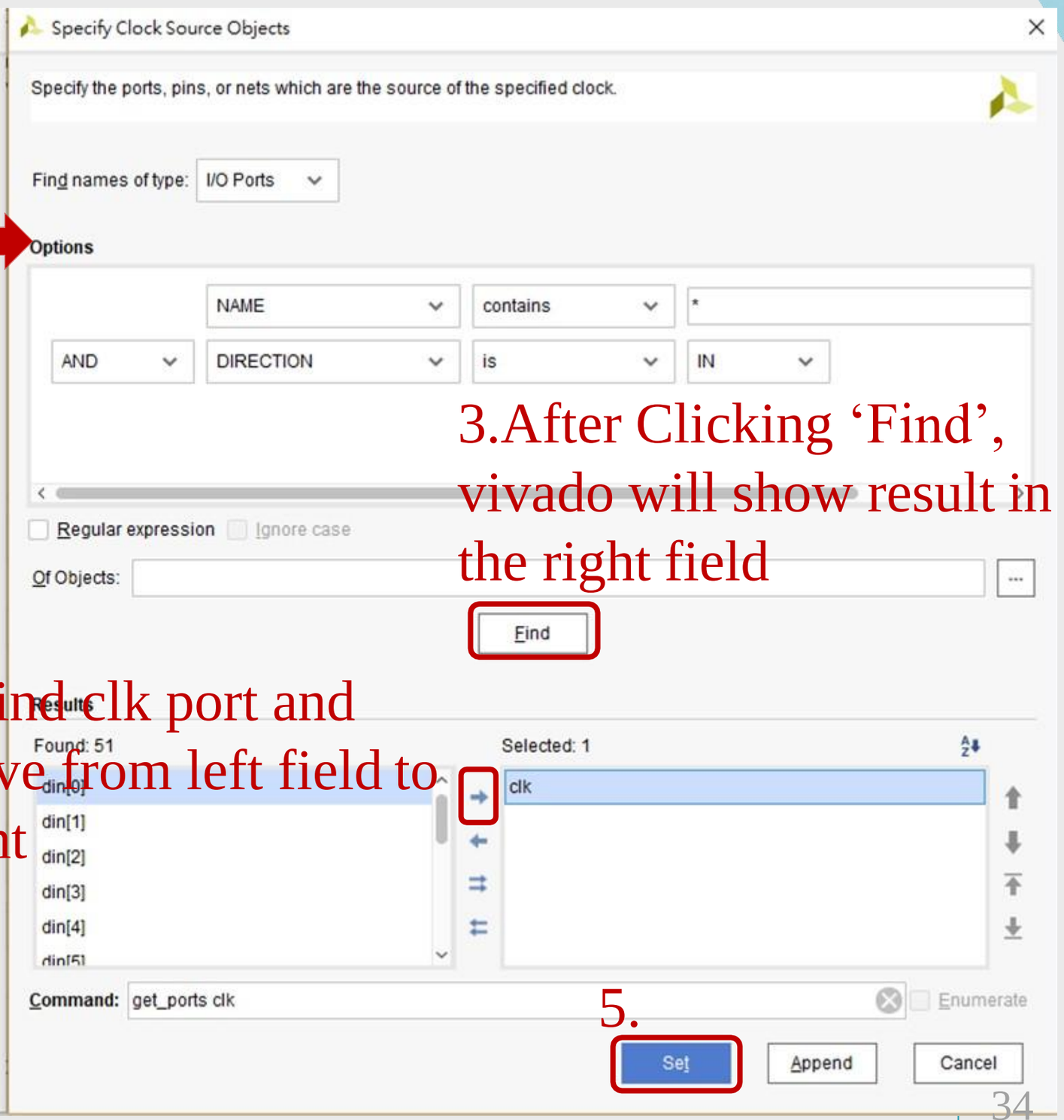
1. You must run synthesis once after creating project.





Setting Constraint (4/5) (GUI)





2.

3.After Clicking ‘Find’, vivado will show result in the right field

4.Find clk port and move from left field to right

Setting Constraint (5/5) (GUI)

Project Summary | Device | Timing Constraints *

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File
2	clk	10.000	0.000	5.000	☐	[get_ports clk]	<unsaved co...

Double click to create a Create Clock constraint

- Clocks (1)
  - Create Clock (1)
  - Create Generated Clock (0)
  - Rename Auto-Derived Clock (0)
  - Set Clock Latency (0)
  - Set Clock Uncertainty (0)
  - Set Clock Groups (0)
  - Set Clock Sense (0)
  - Set Input Jitter (0)
  - Set System Jitter (0)
  - Set External Delay (0)
- Inputs (0)

All Constraints

Position	Command	Scoped Cell
Constraints	1.	
<unsaved constraints>		
2	create_clock -period 10.000 -name clk -waveform {0.000 5.000} [get_ports clk]	

2.

Apply | Cancel

3. Finally, you have to check the timing constraint written correctly in the .xdc file.

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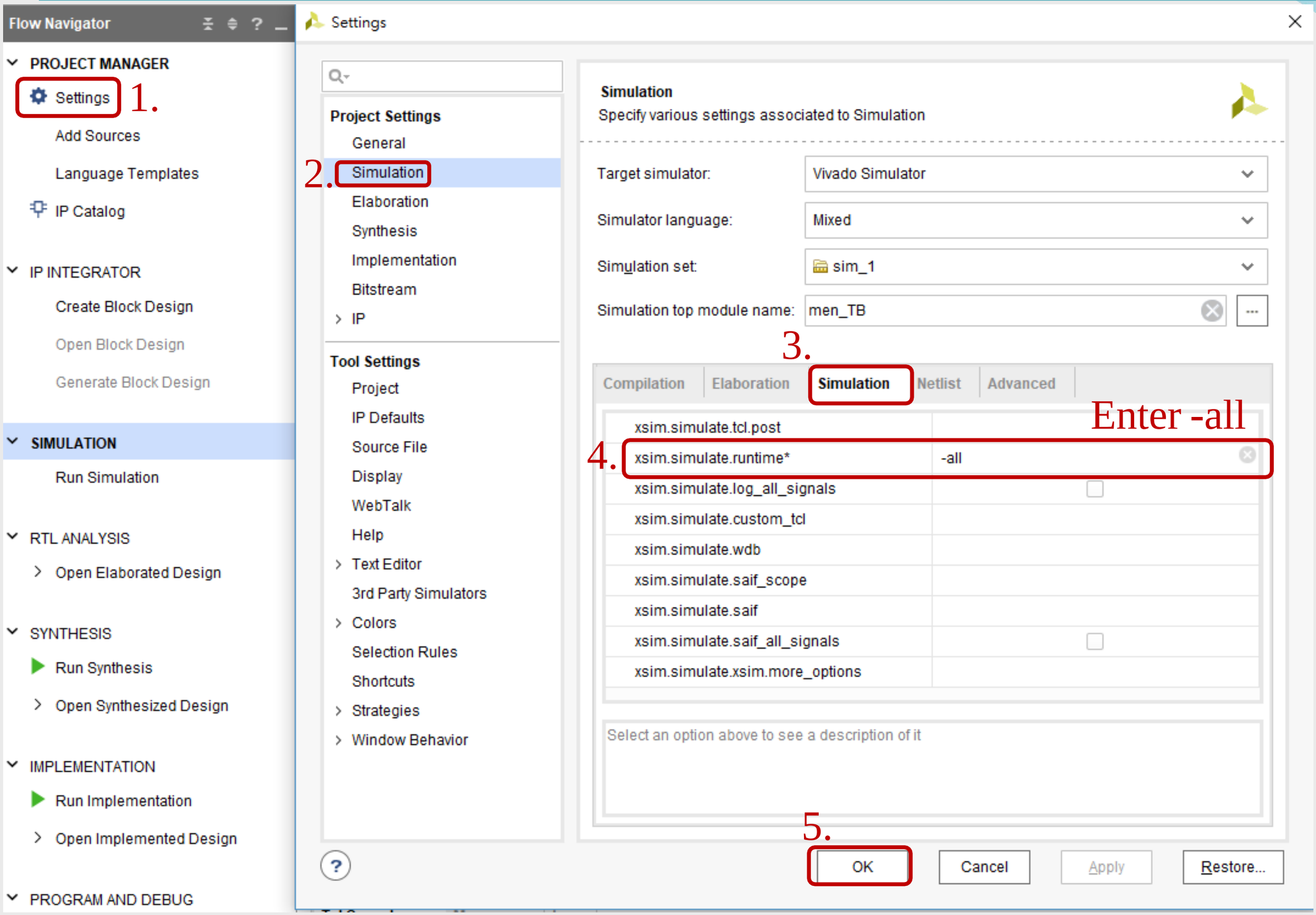
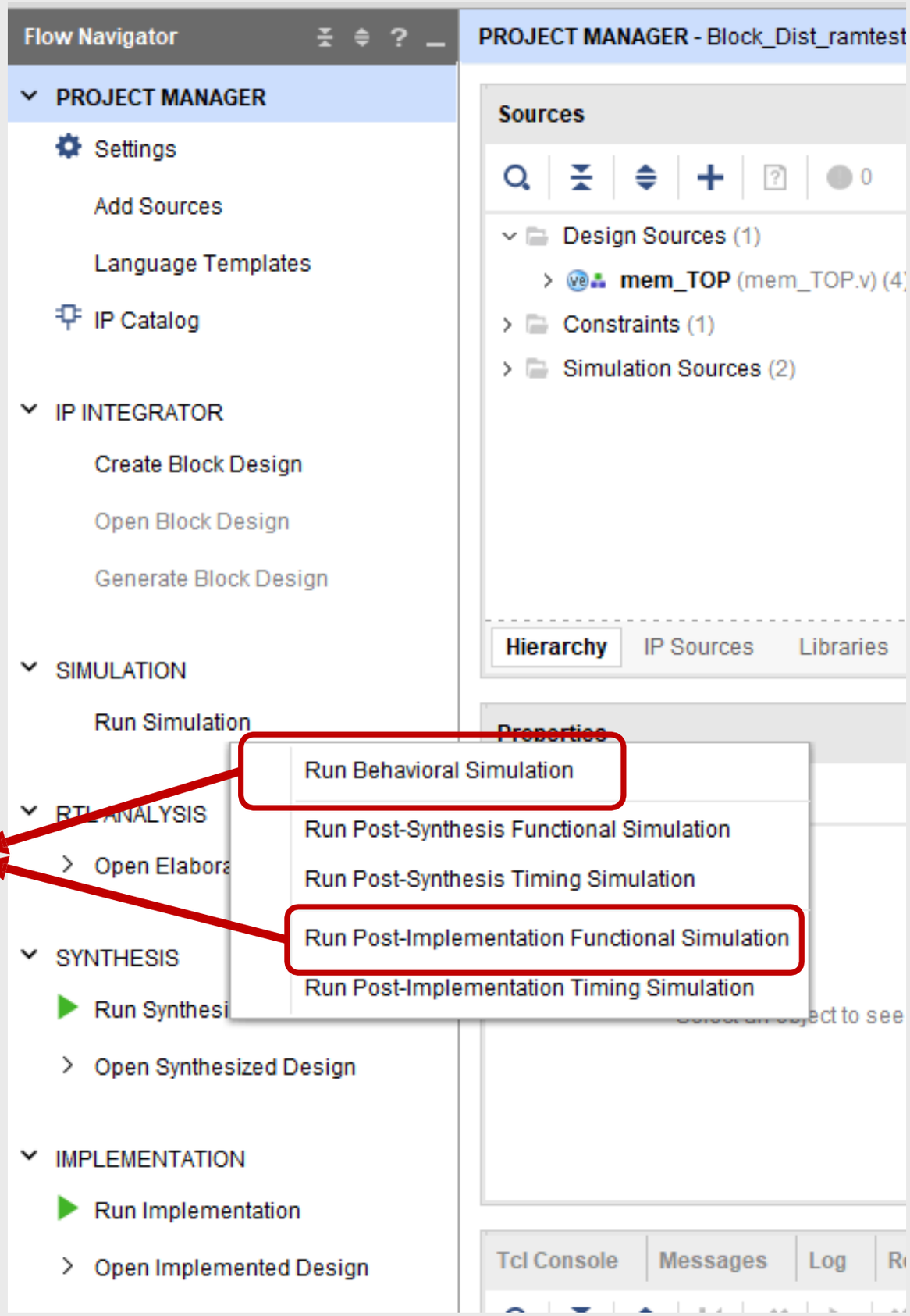
Xsim (1/7)

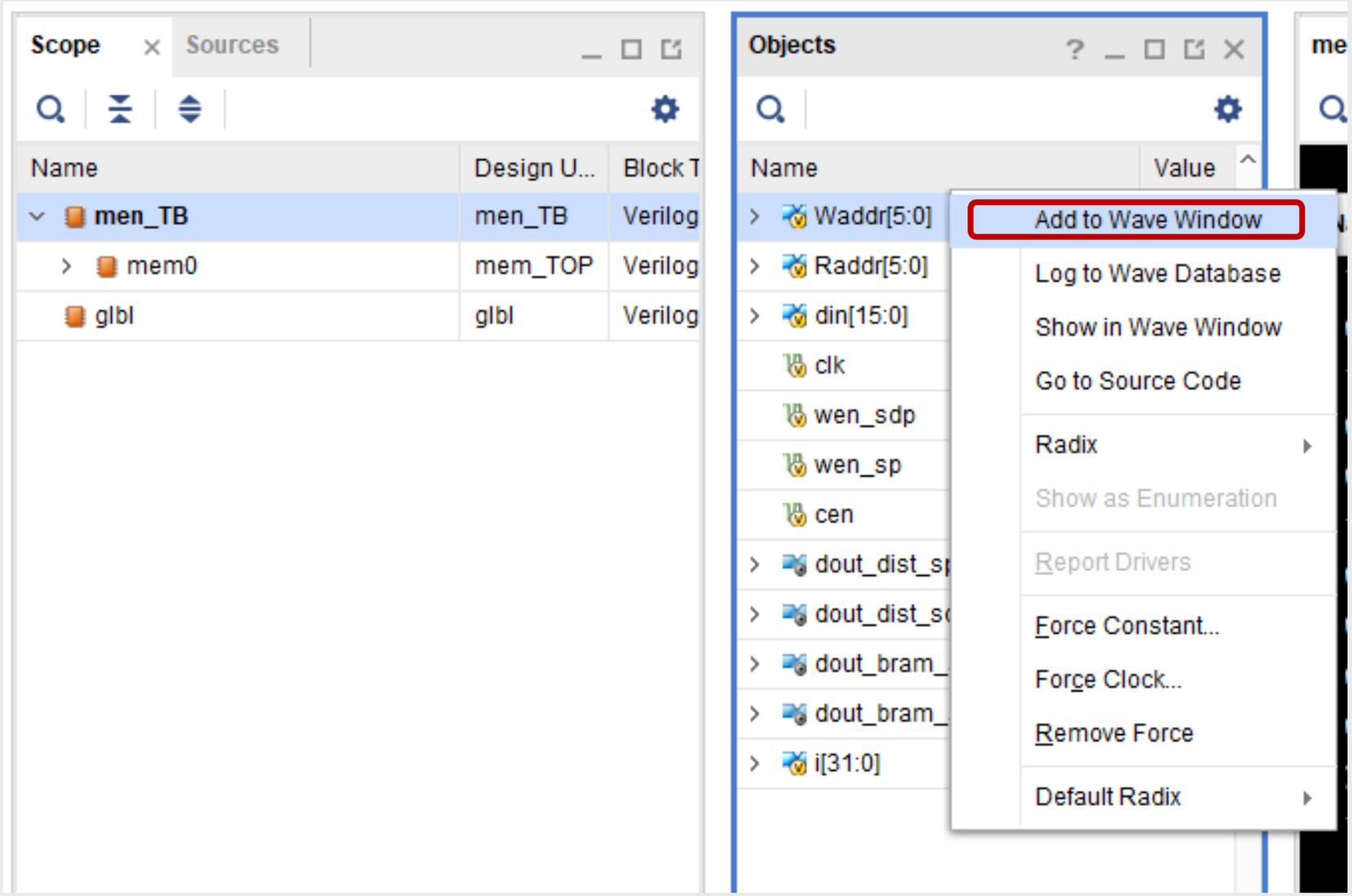

Flow Navigator
PROJECT MANAGER
Settings
1.
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Settings
Project Settings
General
2.
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Window Behavior
Simulation
Specify various settings associated to Simulation
Target simulator:
Vivado Simulator
Simulator language:
Mixed
Simulation set:
sim_1
Simulation top module name:
men_TB
3.
Compilation
Elaboration
Simulation
Netlist
Advanced
Enter -all
xsim.simulate.tcl.post
4.
xsim.simulate.runtime*
-all
xsim.simulate.log_all_signals
xsim.simulate.custom_tcl
xsim.simulate.wdb
xsim.simulate.saif_scope
xsim.simulate.saif
xsim.simulate.saif_all_signals
xsim.simulate.xsim.more_options
Select an option above to see a description of it
5.
OK
Cancel
Apply
Restore...

Xsim (2/7)



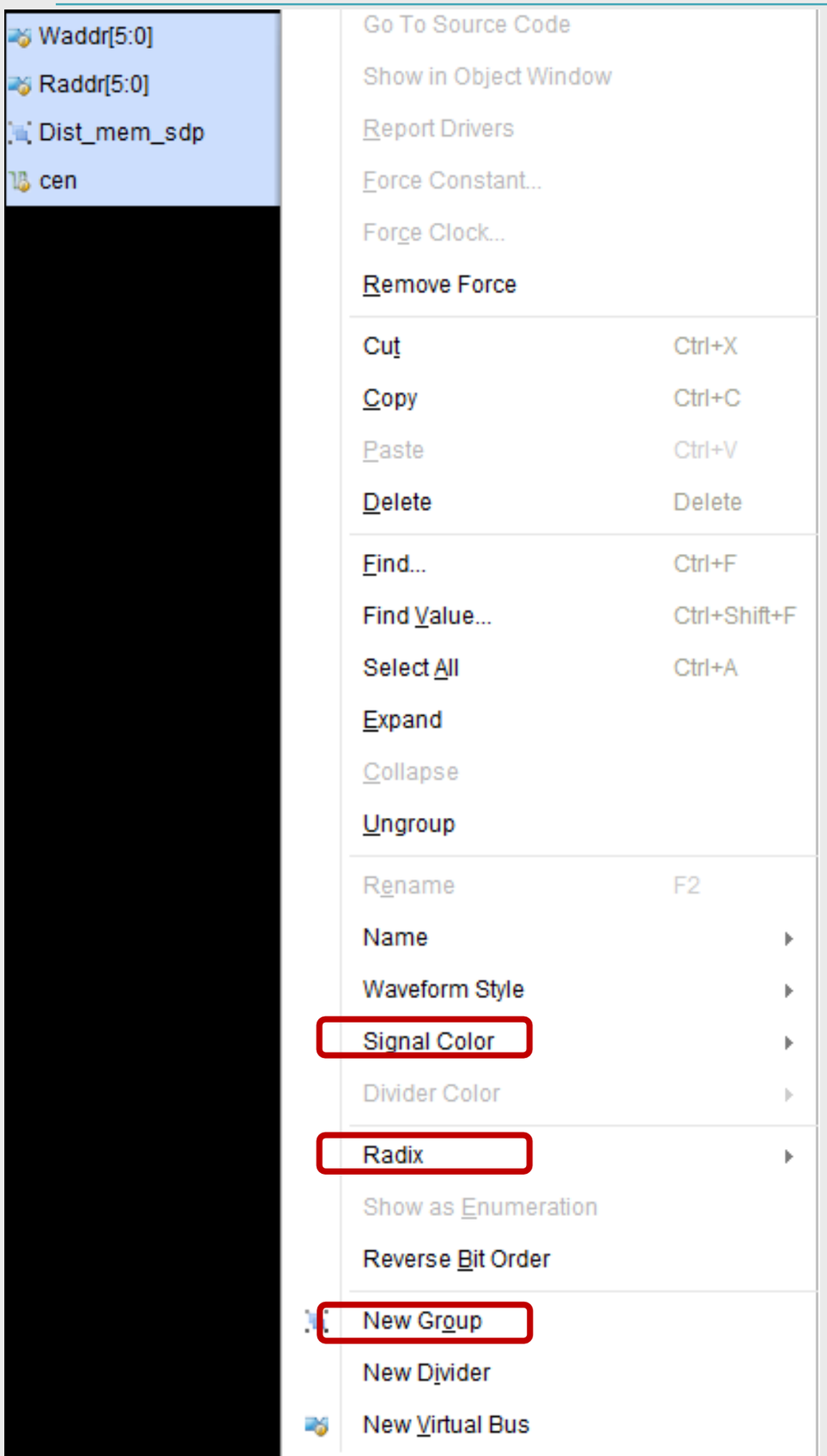
We mainly use these two Simulation

Xsim (3/7)



- You can add some signals which you want to observe.

Xsim (4/7)



- There are three ways to help you observe waveform efficiently.

1. New Group：

   Fold serveral signals into one row.

2. Signal Color

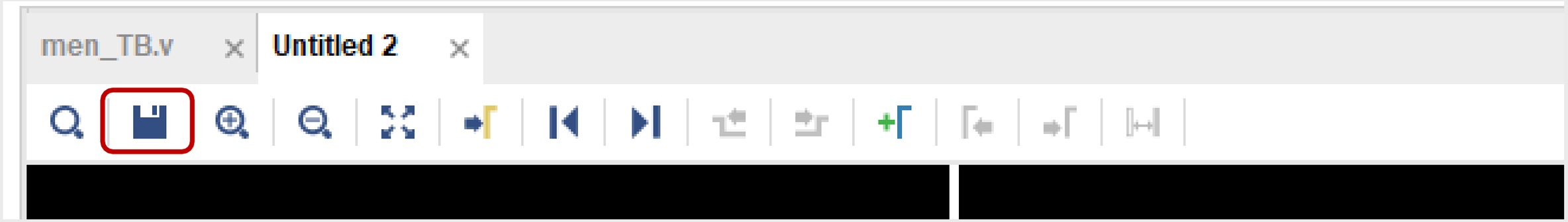
   ： Change color

3. Radix：

   1. Dec, Hex, etc.

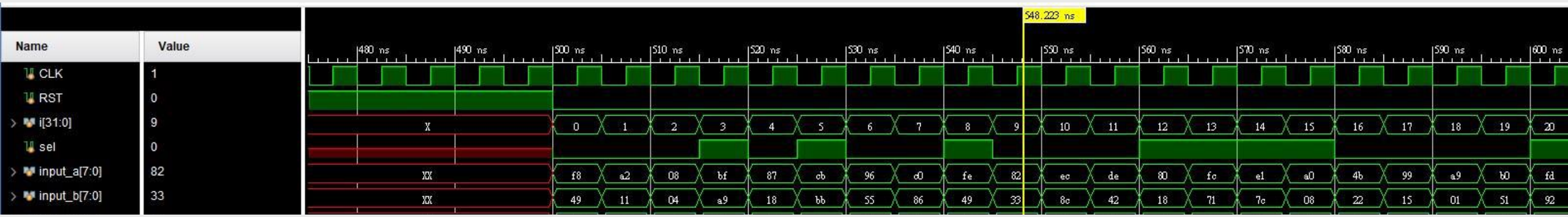
Xsim (5/5)

•After you arranged the signals in waveform, you can ‘Save Waveform Configuration’(.wcfg)



Xsim (5/5)

- 截圖pre/post sim波型(共兩張



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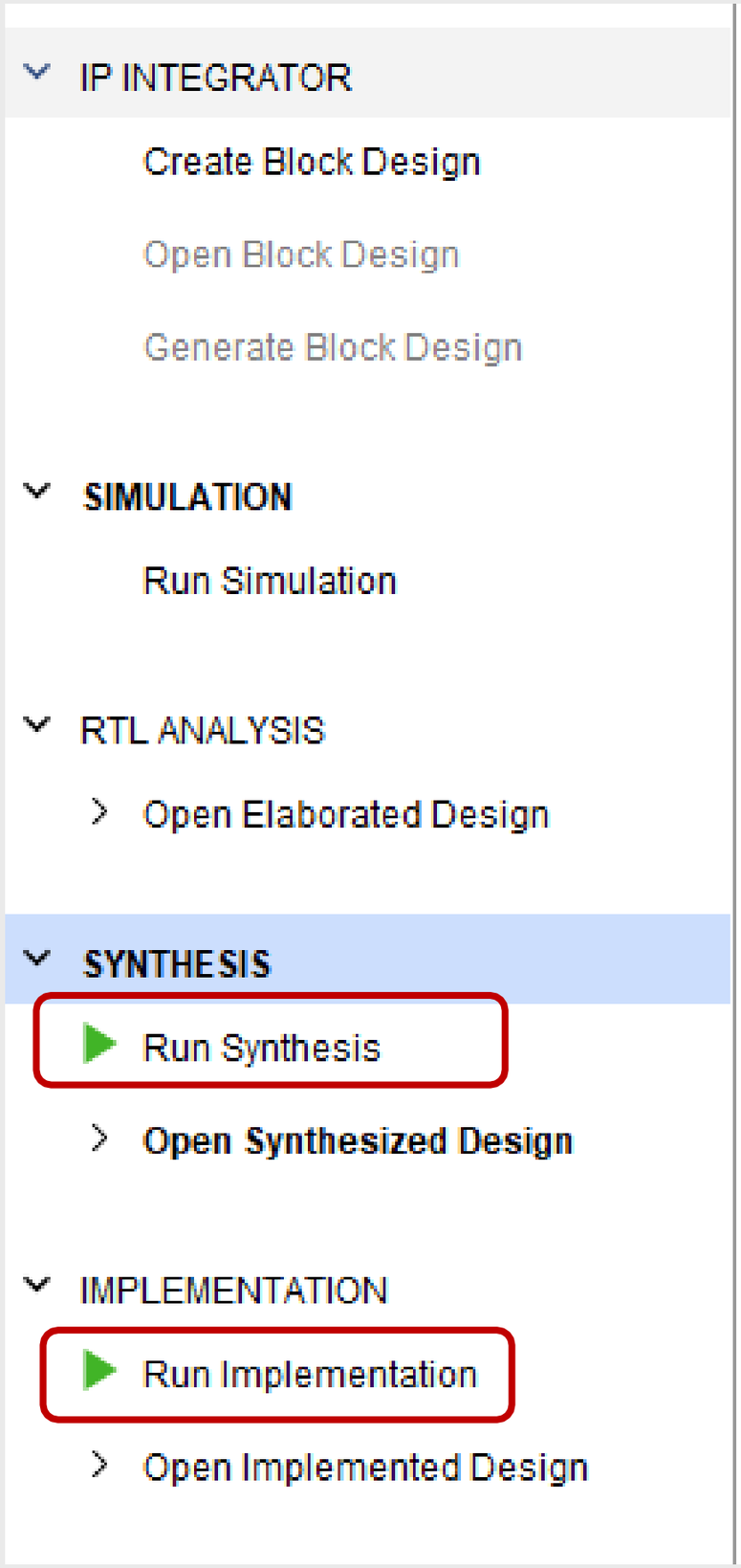
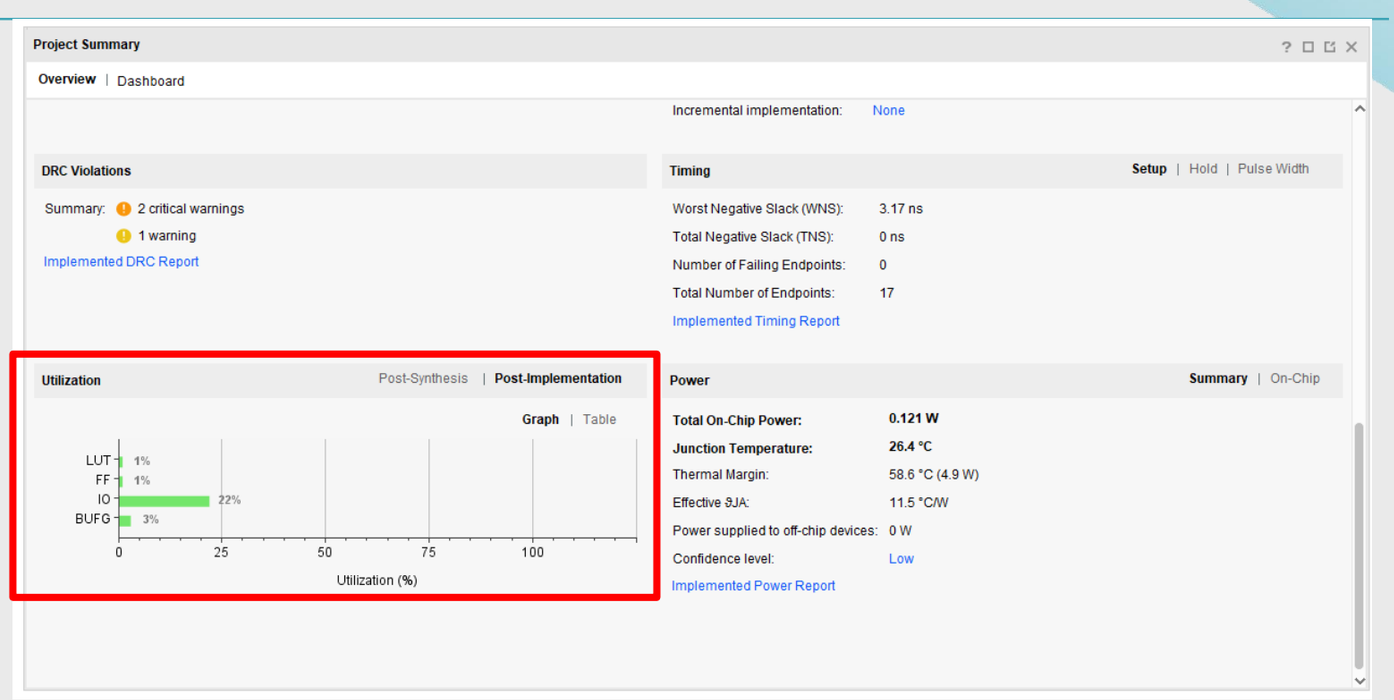
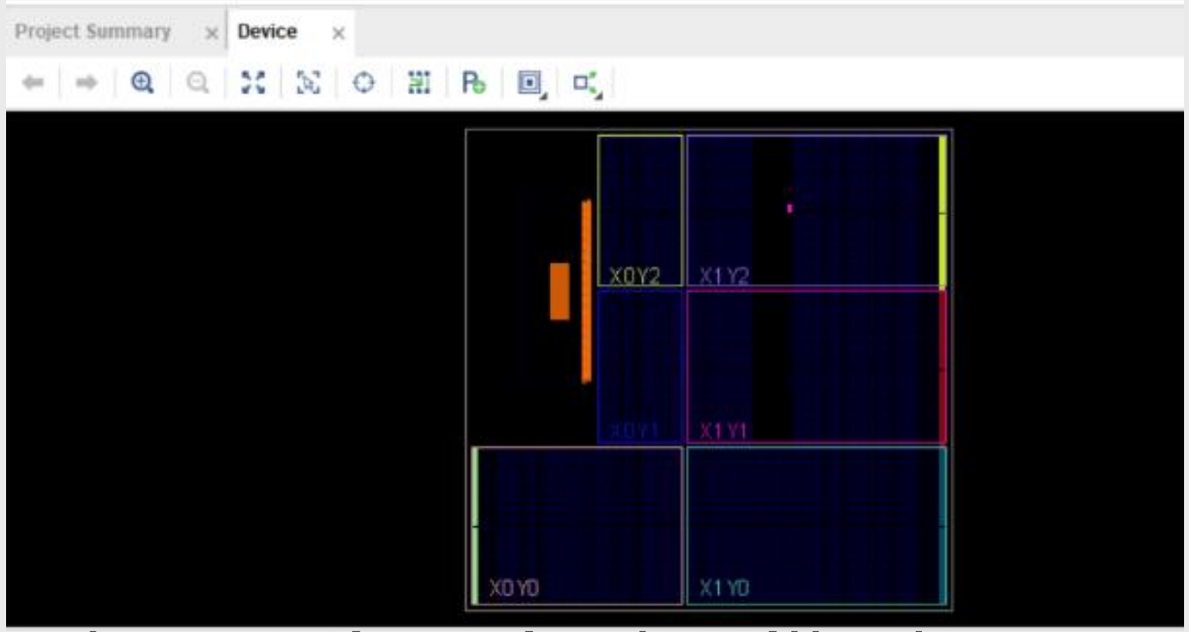
Synthesis & Implementation (1/3)







If you run implementation, vivado will ask you run synthesis first.

Synthesis & Implementation (2/3)

- If all of the value is black font, this means the implementation is successful.

Tcl Console | Messages | Log | Reports | **Design Runs** | Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1 (active)	**constrs_1**	**Synthesis Out-of-date**								**0**	**0**	**0.00**	**0**	**0**
impl_1	constrs_1	Implementation Out-of-date	6.902	0.0...	0.037	0.0...	0.000	0.665	0	40	0	1.00	0	0

1. If implementation didn’t success, it will show error part in red font
2. Please check if timing violation or area is exceeding the limit.

Synthesis & Implementation (3/3)

- Resource：

1. LUT ：Look-up table

   Combinational circuit

2. FF ：Flip-Flop

   Register of sequential circuit

3. BRAM/LUTRAM

   ： Memory

4. DSP：Digital signal processor

   Special arithmetic (multiplication, division, etc.)

5. IO：

   Bit number of IO port.

6. BUFG：

   Usually is used by clock source.

Outline

1. **Download & Install**
2. **Setup License**
3. **Create Project**
4. **Setting Constraint**
5. **Xsim**
6. **Synthesis & Implementation**
7. **Summary**

Summary (1/3)

- FPGA Design Flow：
    1. Write Verilog
    2. Behavior Simulation
    3. Setting Constraint
    4. Synthesis
    5. Implementation
    6. Post-Implementation Functional simulation

Summary (2/3)

2. **Design requirement：**
   - **Clock frequency at 100MHz(Clock=10ns).**
   - **<u>No error and critical warning</u> after running implementation.**
   - **You have to check the warnings will not cause your design incorrect.**

Summary (3/3)

Implementation Complete

Default Layout

Project Summary | Device | MAD.v | MAD_tb.v

Overview | Dashboard

Synthesis

Status:	Complete
Messages:	1 warning
Part:	xc7z020clg484-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports

Implementation — Summary | Route Status

Status:	Complete
Messages:	No errors or warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: 2 critical warnings

1 warning

Implemented DRC Report

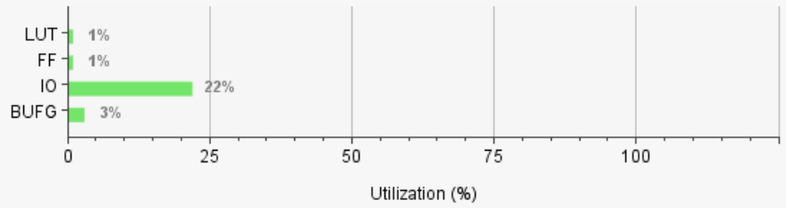
Timing — Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	3.17 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	17

Implemented Timing Report

Utilization — Post-Synthesis | Post-Implementation

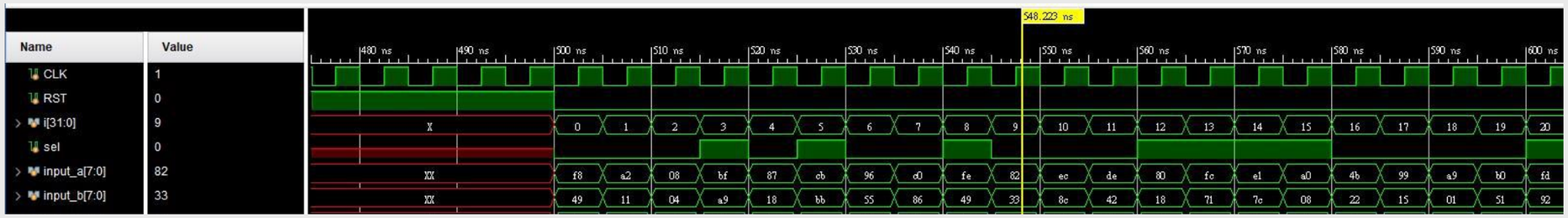
Graph | Table



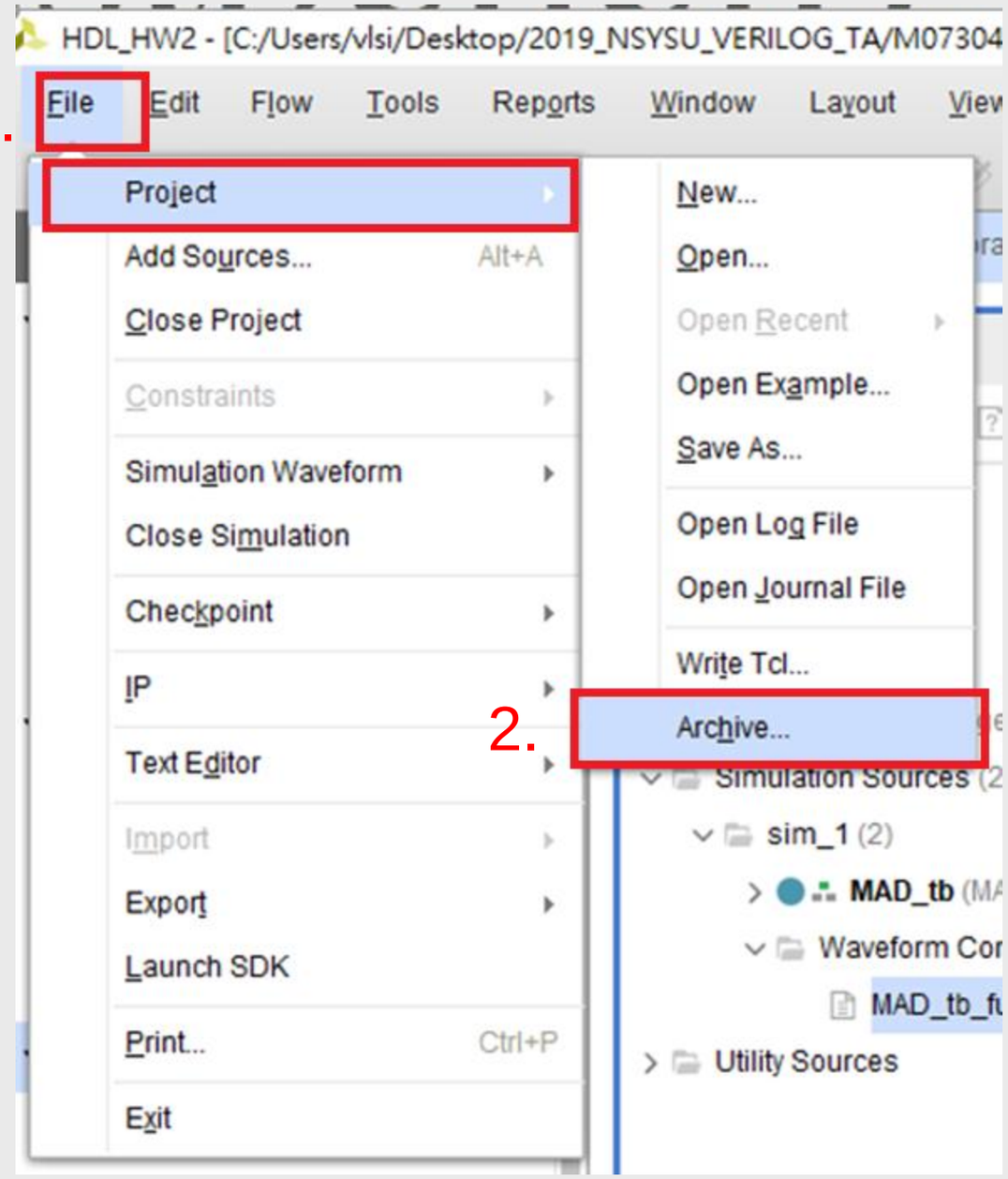
Power — Summary | On-Chip

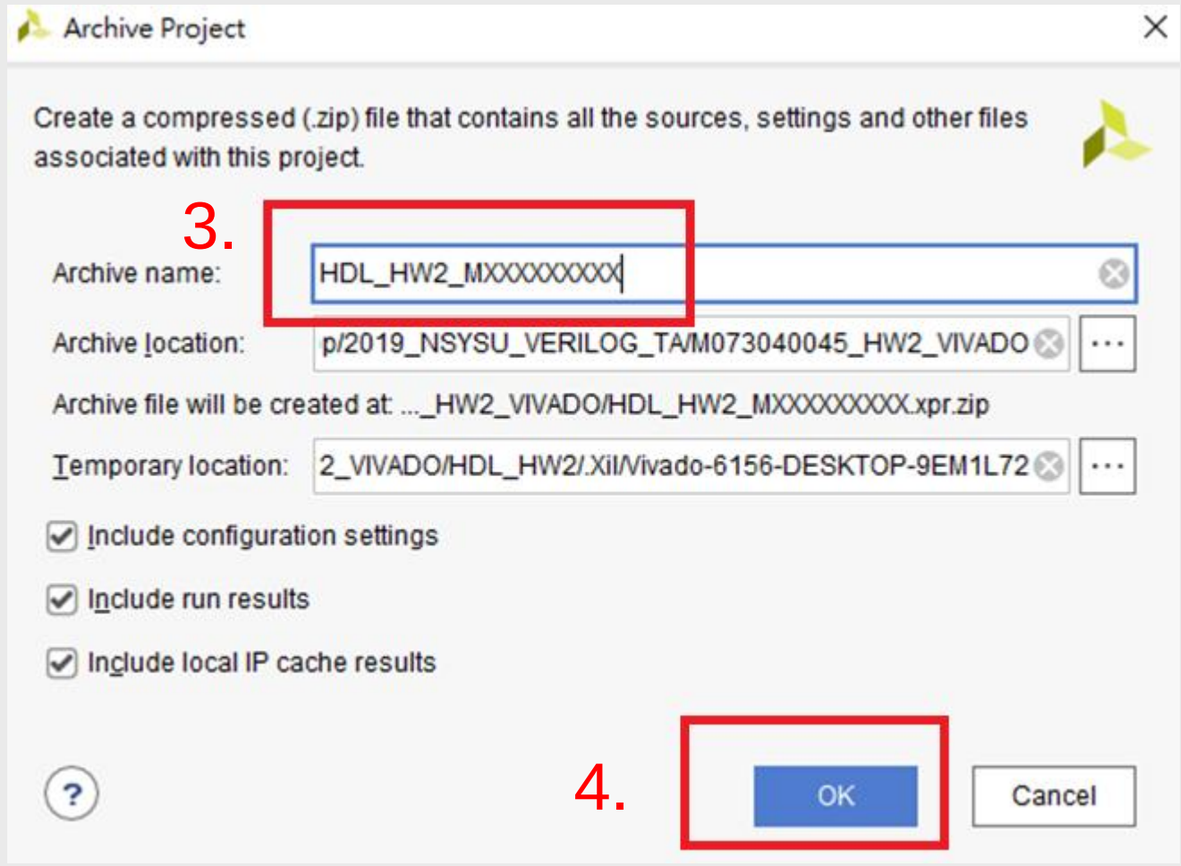
Total On-Chip Power:	**0.121 W**
Junction Temperature:	**26.4 °C**
Thermal Margin:	58.6 °C (4.9 W)
Effective ϑJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report



匯出壓縮檔(.xpr.zip)





Project完成後，可如左圖流程直接產生壓縮檔。

在繳交vivado檔案時，請將vivado壓縮檔路徑裡的檔名.wdb 刪除，以免檔案過大，其他同學無法上傳。
該路徑為 project名稱 (HDL_HWx_MXXXXXX).sim/sim_1/behav/xsim 以及 (HDL_HWx_MXXXXXX).sim/sim_1/impl/func /xsim
請確保壓縮檔裡的這兩個資料夾裡沒有.wdb檔。

整理檔案

整理成一包Vivado資料夾
放進Server HW2裡面一起繳交

Pipeline.xdc
Behavior.wcfg
post-imp.wcfg
.xpr.zip