

# Xilinx Vivado Tutorial

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2025/11/17  
EC5015-VLSILab

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# Outline

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- 1. Download & Install**
- 2. Setup License**
- 3. Create Project**
- 4. Setting Constraint**
- 5. Xsim**
- 6. Synthesis & Implementation**
- 7. Summary**

# Download & Install (1/1)

1. 連結至Xilinx官網 Website:

<https://www.xilinx.com/products/design-tools/vivado.html>

2. Resources & Support->Downloads-> Vivado ML Developer Tools

The screenshot shows the AMD Xilinx website's navigation bar at the top, featuring the AMD and XILINX logos, followed by links for Products, Solutions, and Resources & Support (which is underlined). A vertical sidebar on the left contains links for Downloads, Developer Resources, Partner Resources, and Support. The main content area displays several categories under 'Resources & Support': EPYC Processors, Radeon Graphics & AMD Chipsets, Adaptive SoCs & FPGAs, Vivado ML Developer Tools, Vitis Software Platform, Vitis Accelerated Libraries, Vitis Embedded Platforms, and PetaLinux Tools. Below these are sections for Ryzen Processors (Ryzen Master Overclocking Utility, StoreMI, PRO Manageability Tools for IT Administrators) and Ethernet Adapters (NIC Software & Downloads). At the bottom of the page is a red 'Download Now' button.

Resources & Support			
EPYC Processors	Radeon Graphics & AMD Chipsets	Adaptive SoCs & FPGAs	Vivado ML Developer Tools
Client & Data Center Tech Docs	Drivers	Vitis Software Platform	Vitis Accelerated Libraries
EPYC White Papers & Briefs	Radeon ProRender Plug-ins	Vitis Embedded Platforms	PetaLinux Tools
EPYC Tuning Guides	PRO Certified ISV Applications		
Ryzen Processors	Ethernet Adapters		
Ryzen Master Overclocking Utility	NIC Software & Downloads		
StoreMI			
PRO Manageability Tools for IT Administrators			

# Download & Install (2/11)

3. 選擇Vivado Archive
4. 選擇2018.3並下載Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation裡的All OS installer Single-File Download

Version

- [2023.1](#)
- [2022.2](#)
- [2022.1](#)
- [Vivado Archive](#)
- [ISE Archive](#)
- [CAE Vendor Libraries Archive](#)

Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation

**Important**

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Note: Download verification is only supported with Google Chrome and Microsoft Edge web browsers.

[!\[\]\(5bd3139e49b8ec618dddaa46174de8b0\_img.jpg\) Vivado HLx 2018.3: All OS installer Single-File Download \(TAR/GZIP - 18.97 GB\)](#)

MD5 SUM Value : 8a3a75f26d0e20de21fc673ad9d40d0f

Download Verification [i](#)

[Digests](#) [Signature](#) [Public Key](#)

Download Includes	Vivado Design Suite HLx Editions (All Editions)
Download Type	Full Product Installation
Last Updated	Dec 10, 2018
Answers	<a href="#">2018.x - Vivado Known Issues</a>
Documentation	<a href="#">Release Notes</a>
Support Forums	<a href="#">Installation and Licensing</a>

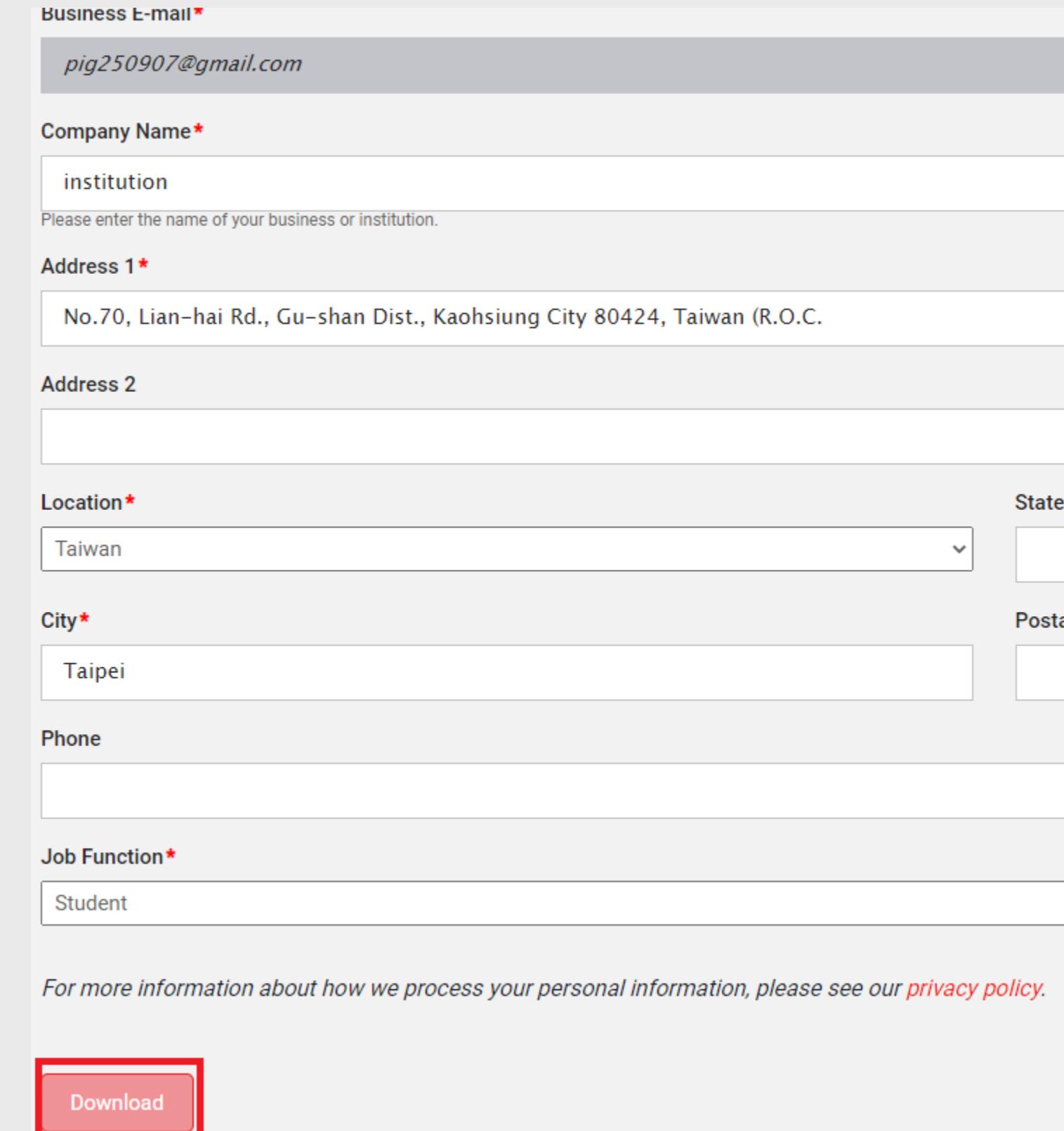
點這個

# Download & Install (2/11)

5. 註冊一個帳號，此帳號然後之後安裝會用到
6. 辦好後就能下載



The AMD login page features the AMD logo at the top. Below it is a large "登入" button. The form fields include "電子郵件地址" (Email Address) and "密碼" (Password), both with placeholder text. A "登入" (Login) button is located below the password field. A horizontal line with the word "或" (Or) separates this from a "創建密碼" (Create Password) button. At the bottom, there are links for "忘記/重設密碼？" (Forgot/Reset Password?) and "幫助" (Help), "使用條款" (Terms of Use), and "隱私權" (Privacy Policy).



The AMD registration form consists of several input fields:

- Business E-mail\***: pig250907@gmail.com
- Company Name\***: institution  
Please enter the name of your business or institution.
- Address 1\***: No.70, Lian-hai Rd., Gu-shan Dist., Kaohsiung City 80424, Taiwan (R.O.C.)
- Address 2**: (empty field)
- Location\***: Taiwan
- City\***: Taipei
- Phone**: (empty field)
- Job Function\***: Student

At the bottom, a note states: "For more information about how we process your personal information, please see our [privacy policy](#)". A prominent red "Download" button is located at the bottom center.

# Download & Install (3/11)

---

1. Exunzip vivado.
2. execute installer
  - Windows :
    - A. Go to folder of vivado
    - B. Double-Click xsetup.exe
  - Linux :
    - A. Open terminal
    - B. cd <path to folder of vivado>
    - C. sudo ./xsetup

# Download & Install (4/11)

Vivado 2017.4 Installer - Welcome

Welcome

We are glad you've chosen Xilinx as your platform development partner. This program can install the Vivado Design Environment, Software Development Kit and Documentation Navigator.

Supported operating systems for Vivado 2017.4 are:

- Windows 7.1: 64-bit
- Windows 10.0 Creators Update: 64-bit
- Red Hat Enterprise Linux 6.6-6.9: 64-bit
- Red Hat Enterprise Linux 7.2-7.3: 64-bit
- CentOS Linux 6.6-6.9: 64-bit
- CentOS Linux 7.2-7.3: 64-bit
- SUSE Enterprise Linux 11.4: 64-bit
- SUSE Enterprise Linux 12.2: 64-bit
- Ubuntu Linux 16.04.2 LTS: 64-bit - Additional library installation required

Note: This release requires upgrading your license server tools to the Flex 11.14.1 versions. Please confirm with your license admin that the correct version of the license server tools are installed and available, before running the tools.

Note: 32-bit machine support is now only available through HW Server standalone product installers

Note: This installation program will not install cable drivers on Linux. This item will need to be installed separately, with administrative privileges.

To reduce installation time, we recommend that you disable any anti-virus software before continuing.

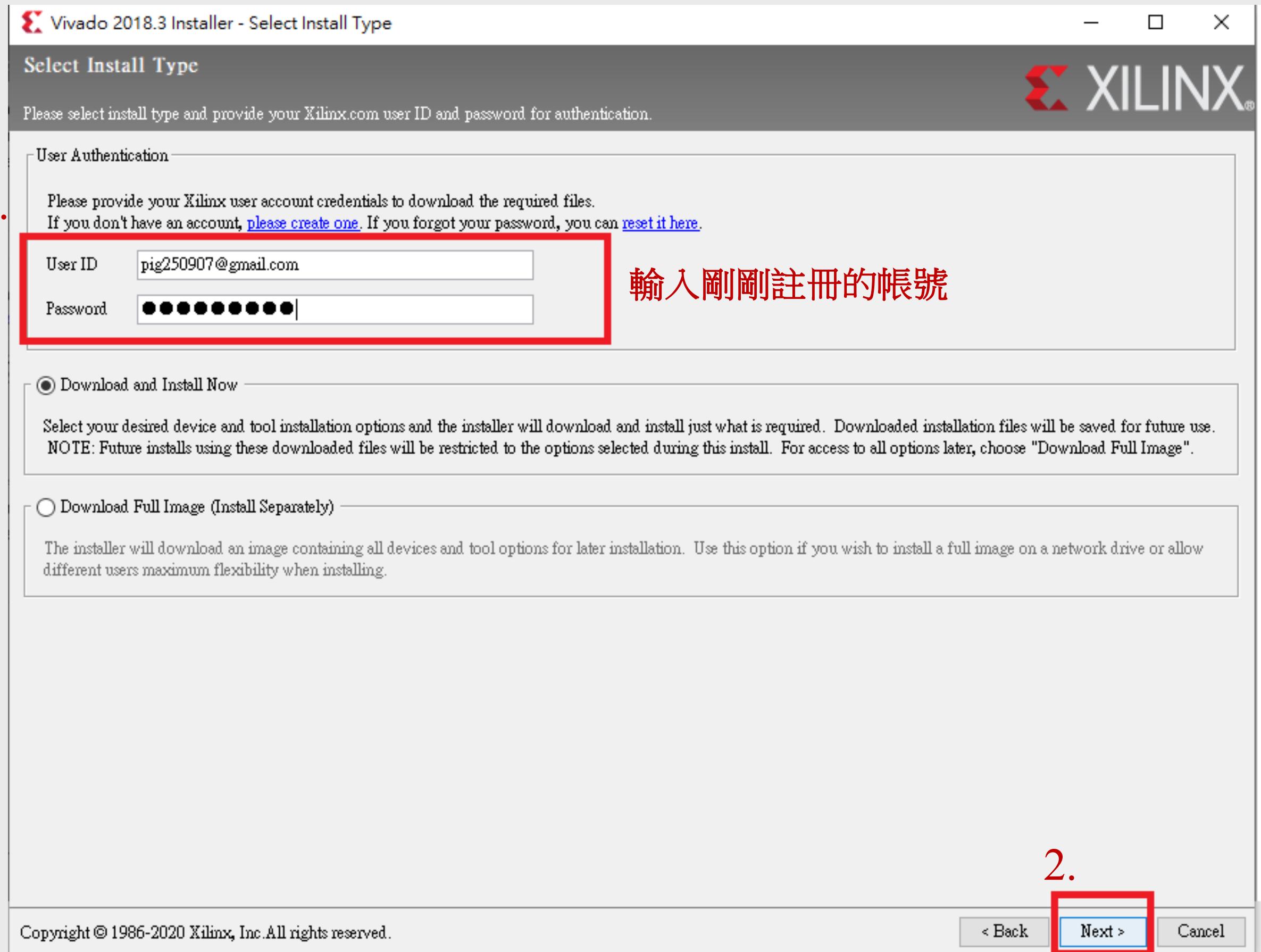
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1.

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Preferences < Back Next > Cancel

# Download & Install (5/11)



# Download & Install (5/11)

Vivado 2017.4 Installer - Accept License Agreements

## Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

**Xilinx Inc. End User License Agreement**

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

1.  I Agree

**WebTalk Terms And Conditions**

By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(a) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

I Agree

**Third Party Software End User License Agreement**

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

2.

< Back   

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# Download & Install (6/11)

 Vivado 2017.4 Installer - Select Edition to Install

Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

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Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

Vivado HL Design Edition

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

Vivado HL System Edition

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

Documentation Navigator (Standalone)

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

1.

2.

< Back  Next > Cancel

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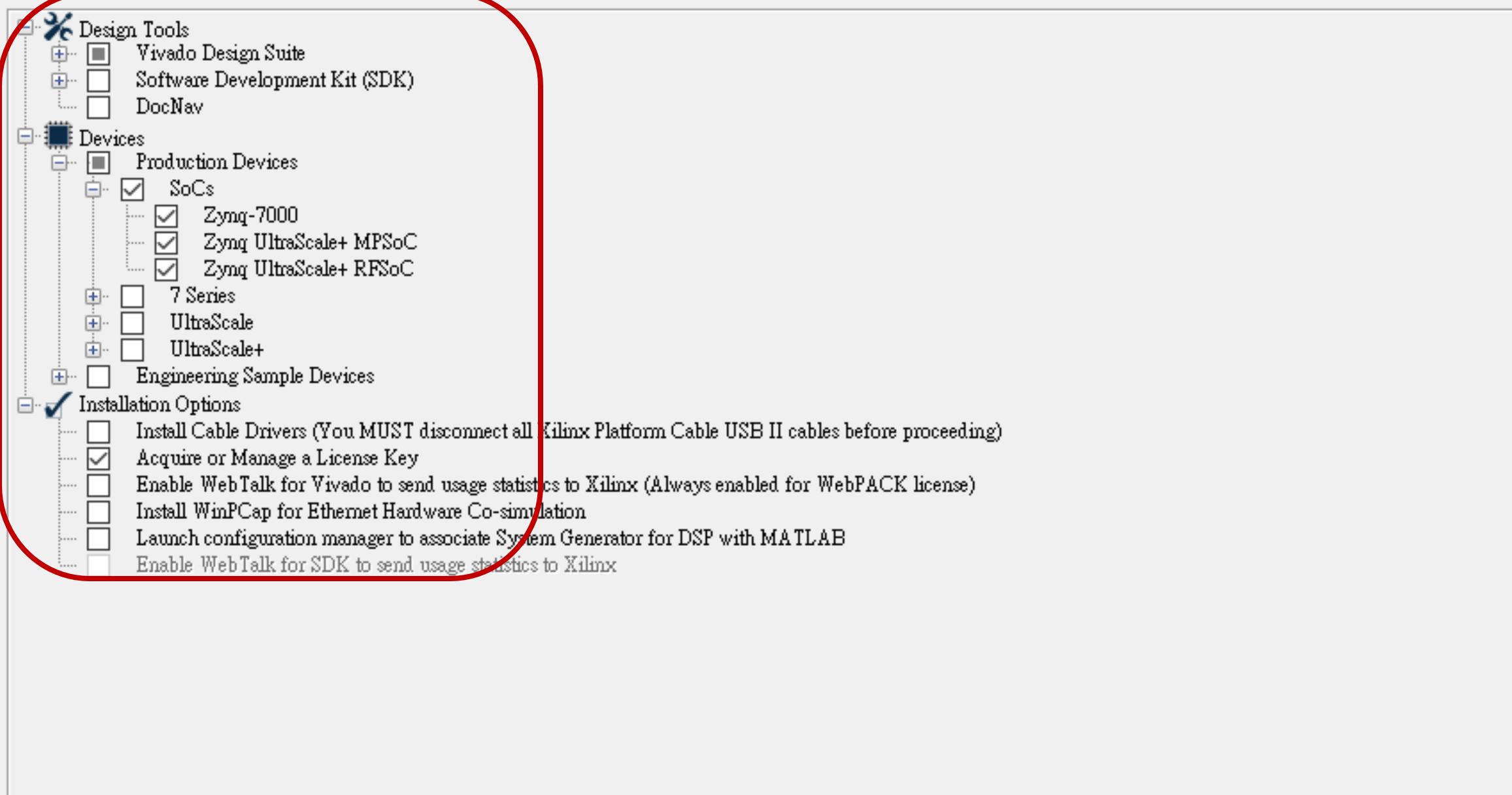
# Download & Install (7/11)

Vivado 2018.3 Installer - Vivado HL System Edition

Vivado HL System Edition

Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.

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1. 

2. 

Design Tools

- + Vivado Design Suite
- + Software Development Kit (SDK)
- DocNav

Devices

- + Production Devices
  - + SoCs
    - Zynq-7000
    - Zynq UltraScale+ MPSoC
    - Zynq UltraScale+ RFSoC
  - + 7 Series
  - + UltraScale
  - + UltraScale+
- + Engineering Sample Devices

Installation Options

- Install Cable Drivers (You MUST disconnect all Xilinx Platform Cable USB II cables before proceeding)
- Acquire or Manage a License Key
- Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)
- Install WinPcap for Ethernet Hardware Co-simulation
- Launch configuration manager to associate System Generator for DSP with MATLAB
- Enable WebTalk for SDK to send usage statistics to Xilinx

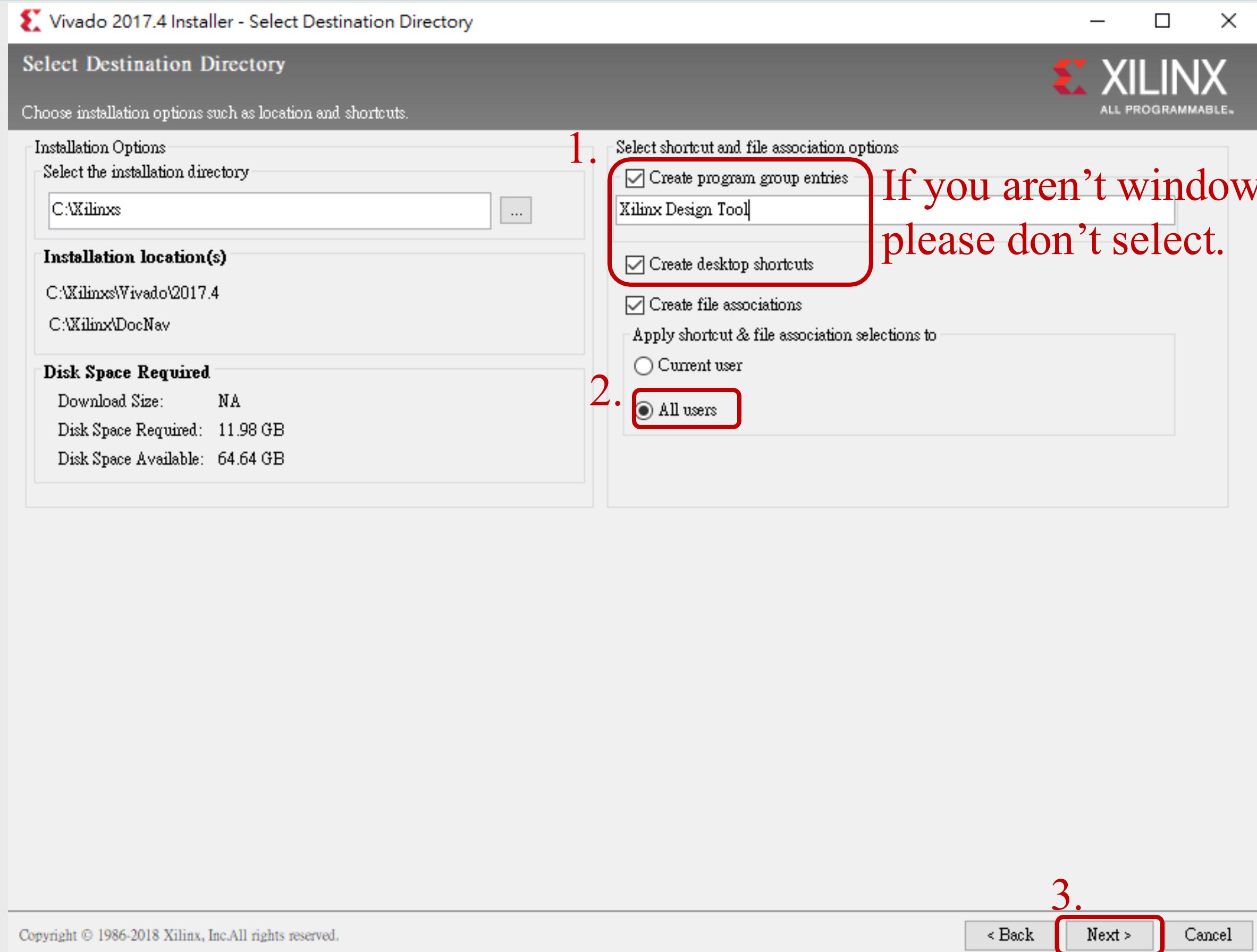
Download Size: 6.8 GB

Disk Space Required: 24.68 GB

Reset to Defaults

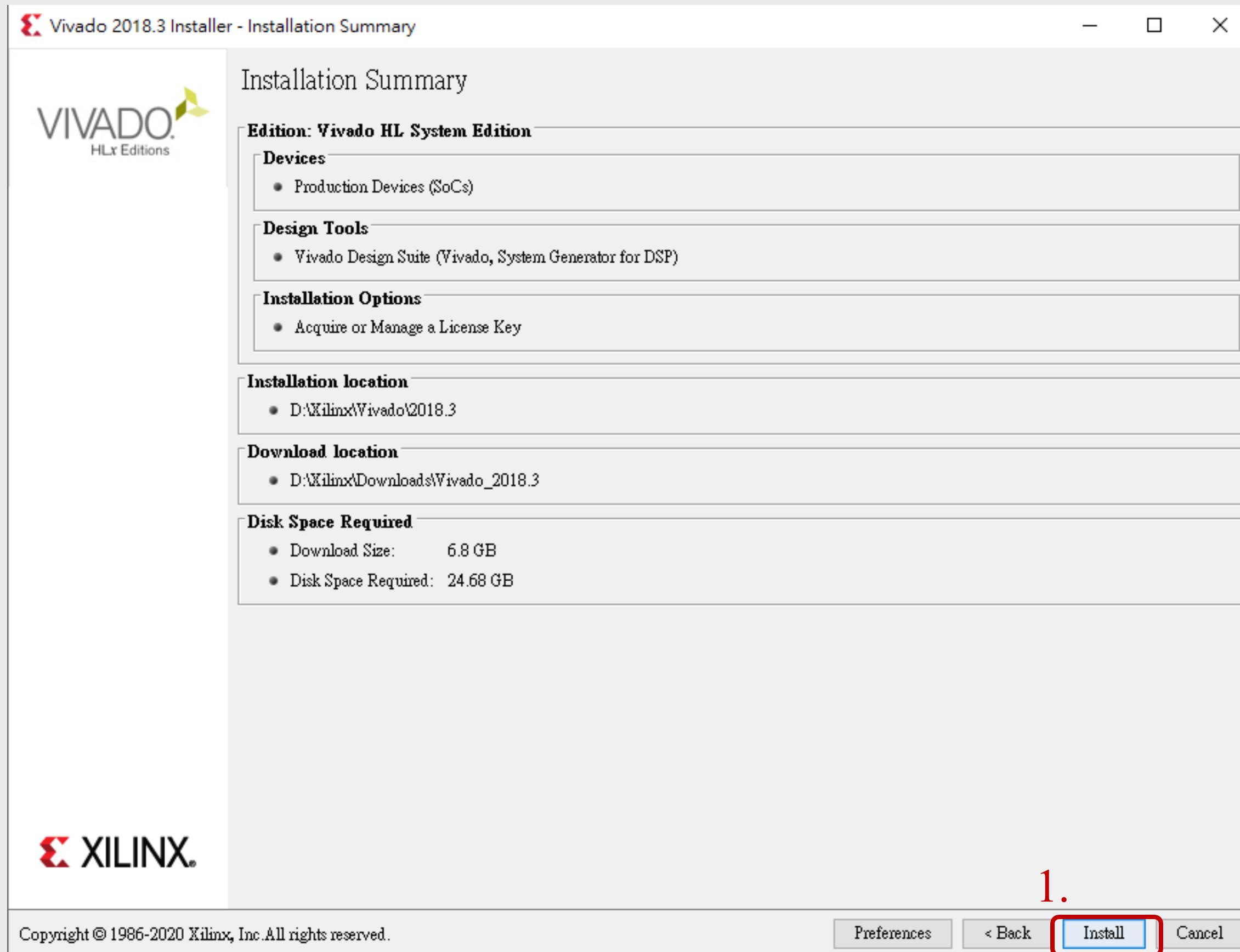
< Back Next > Cancel

# Download & Install (8/11)



# Download & Install (9/11)

- 如安裝完成後遇到License，可先至18頁設定。



# Download & Install (11/11)

After installing vivado, you can open vivado by following :

1. Window :

- ◆ Double-Click the icon

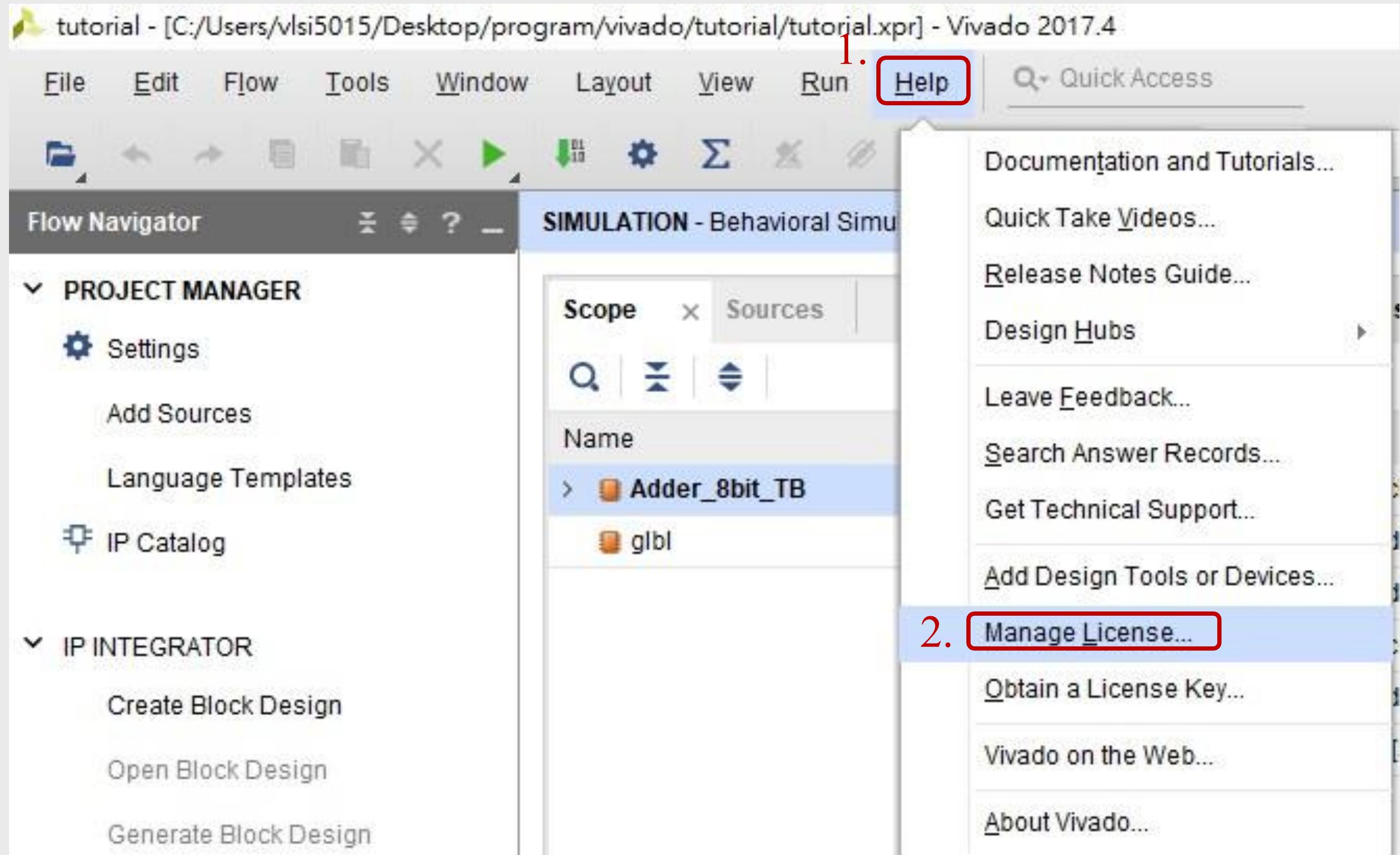


# Outline

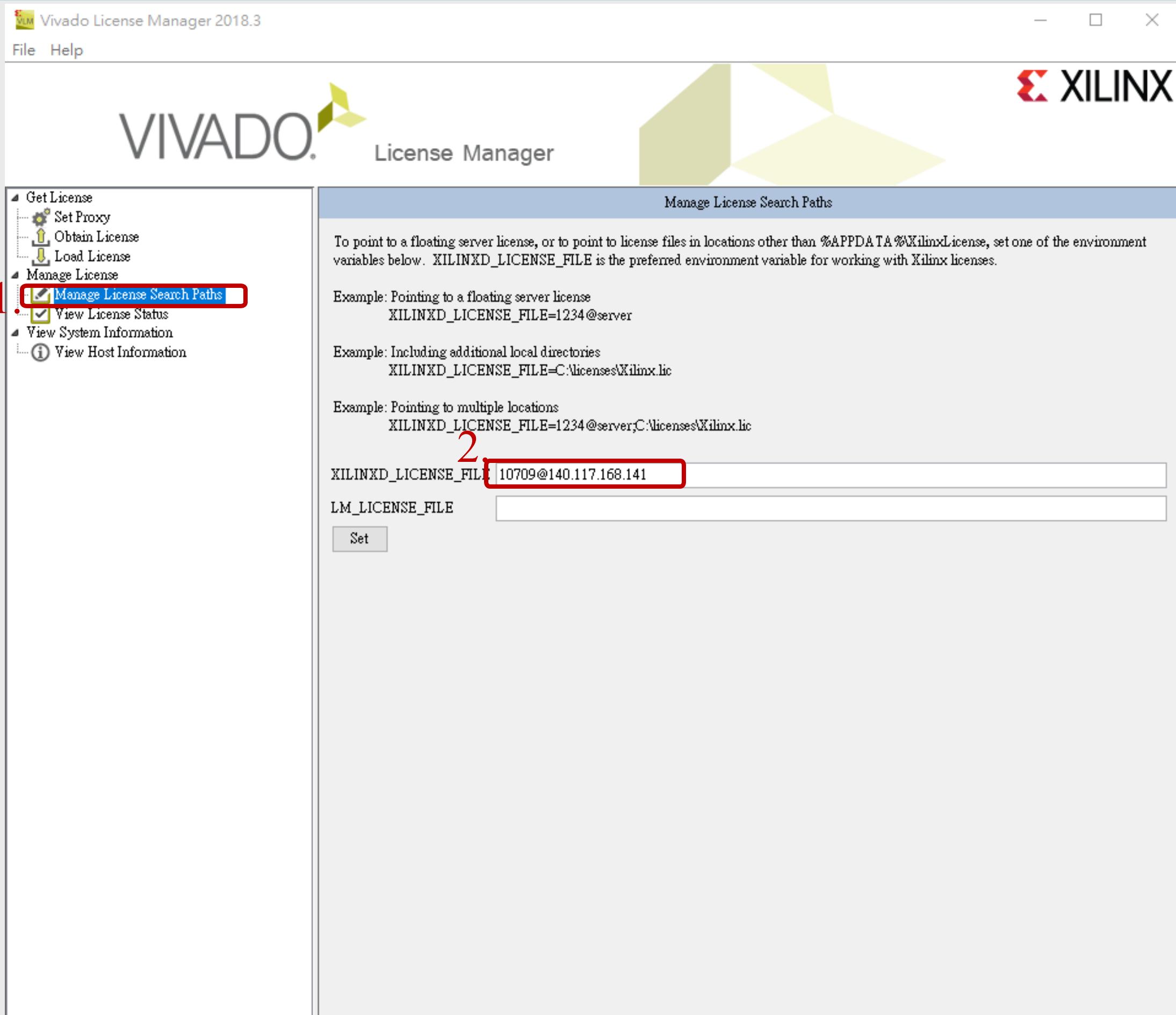
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1. Download & Install
- 2. Setup License**
3. Create Project
4. Setting Constraint
5. Xsim
6. Synthesis & Implementation
7. Summary

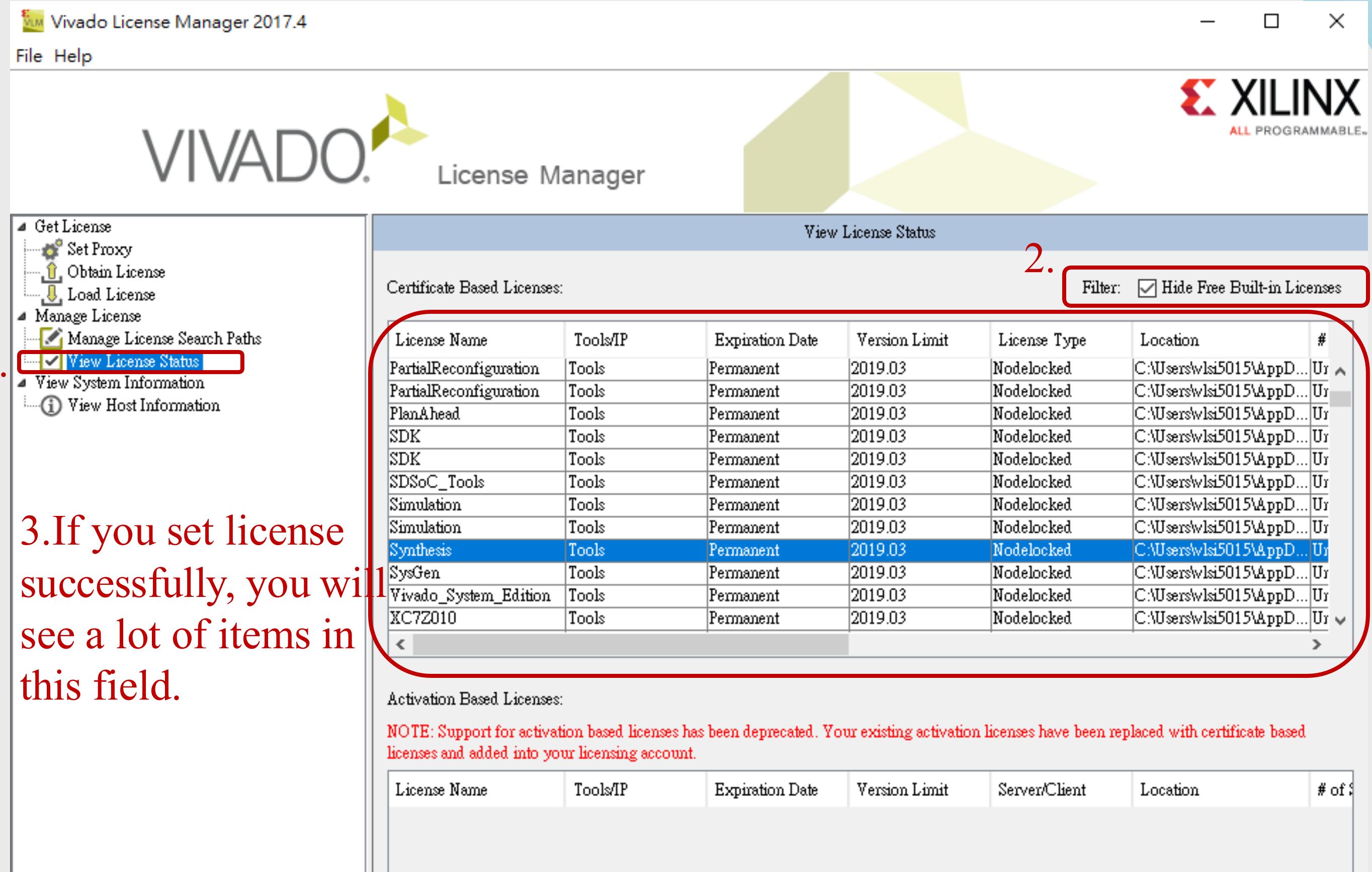
# Setup License (1/3)



# Setup License (2/3)



# Setup License (3/3)

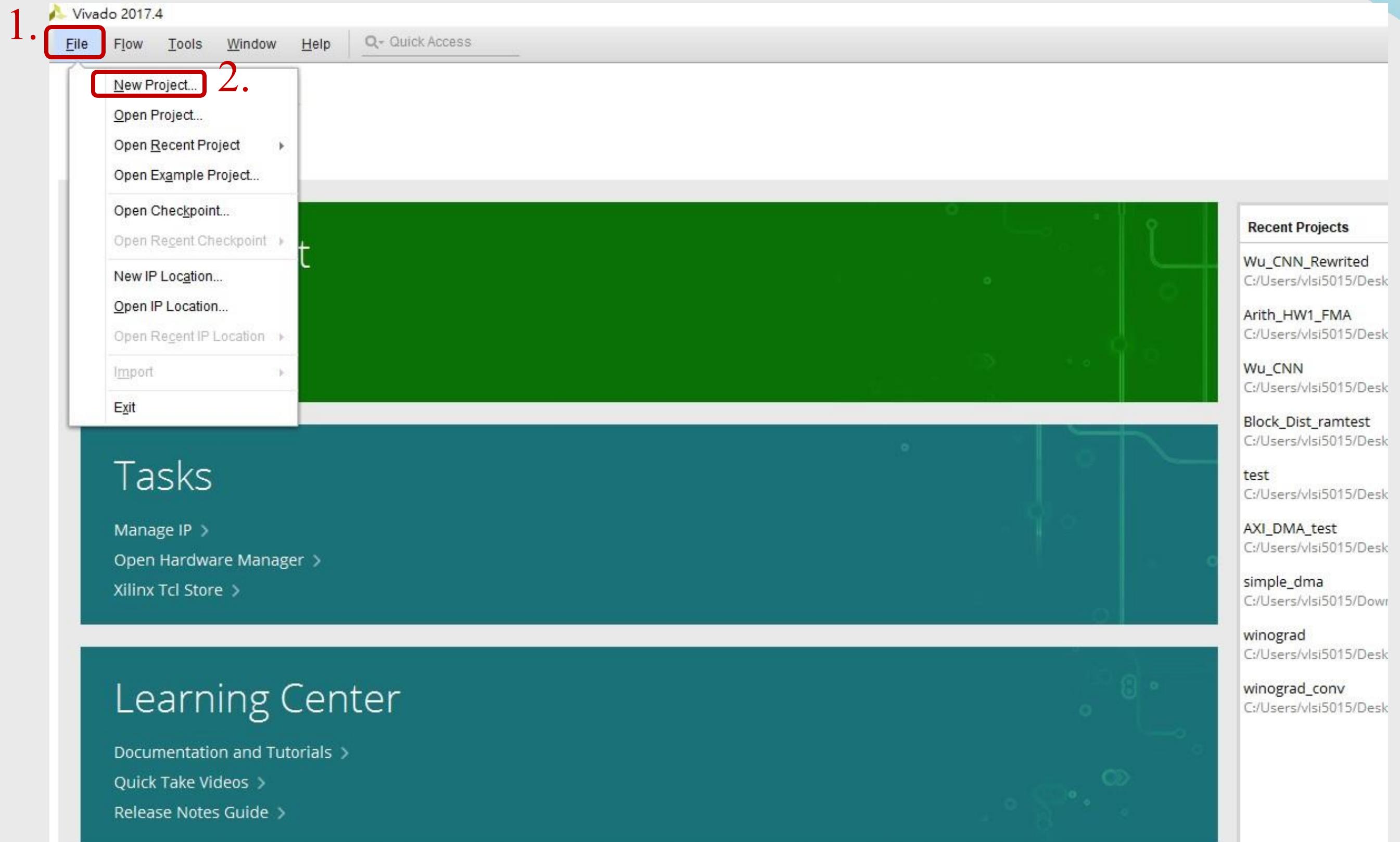


# Outline

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# Create Project (1/8)



# Create Project (2/8)

New Project

**Project Name**

Enter a name for your project and specify a directory where the project data files will be stored.

1. Project name: HDL\_HW2\_std.num\_name

2. Project location: C:/Users/Msi5015/Desktop/program/vivado

Create project subdirectory

Project will be created at: C:/Users/Msi5015/Desktop/program/vivado/HDL\_HW2\_std.num\_name

3.

< Back      Next >      Finish      Cancel

# Create Project (3/8)

New Project X

**Project Type**  
Specify the type of project to create.



1.  RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

2.  Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

We add source codes later  
or you can add now by unselecting this option.

3. Next > Back < Finish Cancel

# Create Project (4/8)

New Project

**Default Part**

Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards 1.

Filter/ Preview

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

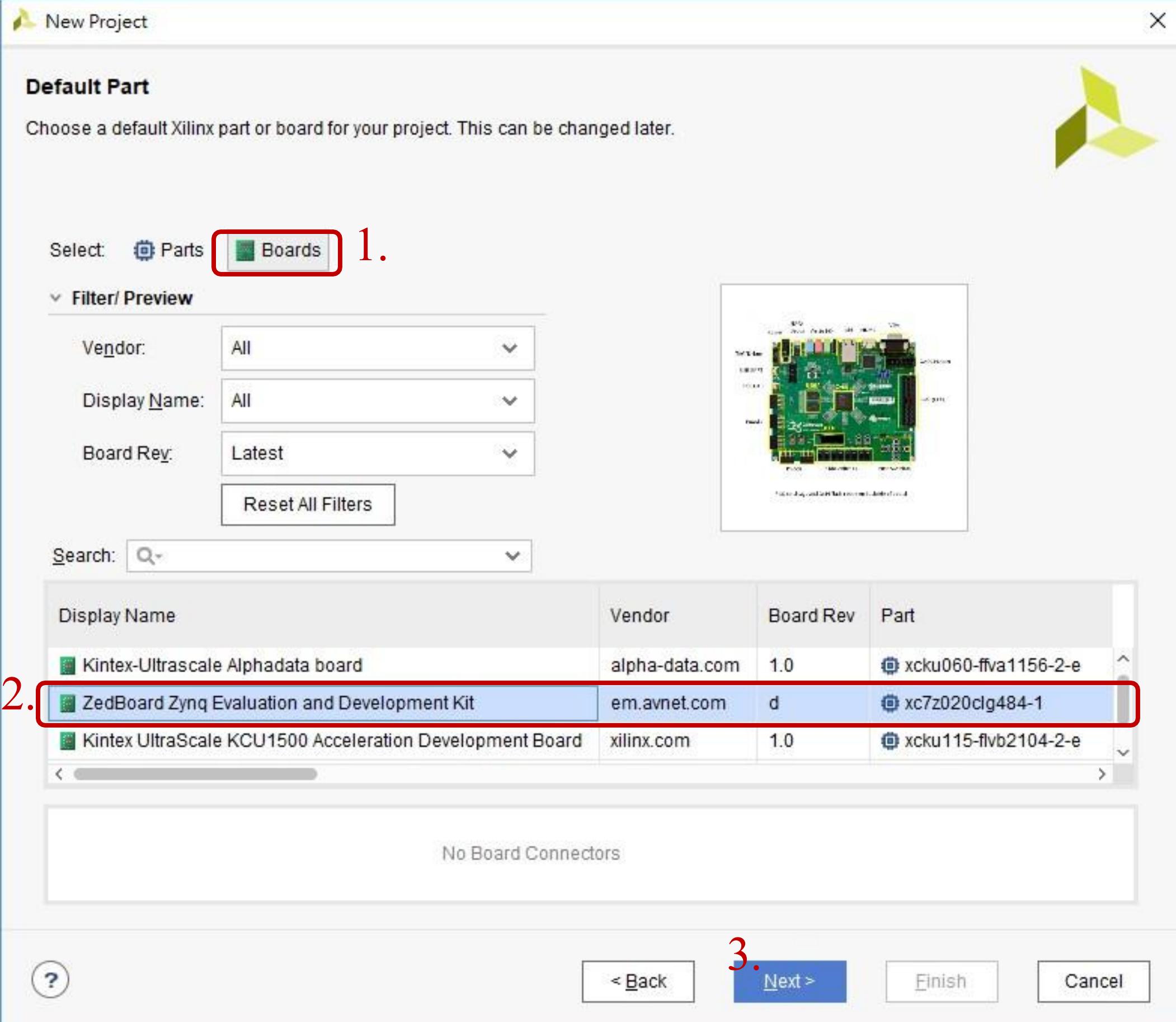
Search:

Display Name	Vendor	Board Rev	Part
Kintex-Ultrascale Alphadata board	alpha-data.com	1.0	xcku060-ffva1156-2-e
2. ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1
Kintex UltraScale KCU1500 Acceleration Development Board	xilinx.com	1.0	xcku115-flvb2104-2-e

No Board Connectors

?

< Back 3. Next > Finish Cancel



Display Name	Vendor	Board Rev	Part
Kintex-Ultrascale Alphadata board	alpha-data.com	1.0	xcku060-ffva1156-2-e
2. ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1
Kintex UltraScale KCU1500 Acceleration Development Board	xilinx.com	1.0	xcku115-flvb2104-2-e

# Create Project (5/8)

New Project

**VIVADO**  
HLx Editions

**New Project Summary**

- i** A new RTL project named 'HDL\_HW2\_std.num\_name' will be created.
- i** The default part and product family for the new project:  
Default Board: ZedBoard Zynq Evaluation and Development Kit  
Default Part: xc7z020clg484-1  
Product: Zynq-7000  
Family: Zynq-7000  
Package: clg484  
Speed Grade: -1

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To create the project, click Finish

1.

< Back    Next >    **Finish**    Cancel

# Create Project (6/8)

The screenshot shows the Vivado Project Manager interface with a project named "tutorial".

**Project Summary:**

- Project name: tutorial
- Project location: C:/Users/Msi5015/Desktop/program/vivado/tutorial
- Product family: Zynq-7000
- Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)
- Top module name: Not defined
- Target language: Verilog
- Simulator language: Mixed

**Board Part:**

- Display name: ZedBoard Zynq Evaluation and Development Kit
- Board part name: em.avnet.com:zed:part0:1.3
- Connectors:
- Repository path: C:/Xilinx/Vivado/2017.4/data/boards/board\_files
- URL: <http://www.zedboard.org>
- Board overview: ZedBoard Zynq Evaluation and Development Kit

**Synthesis:**

- Status: Not started
- Messages: No errors or warnings

**Implementation:**

- Status: Not started
- Messages: No errors or warnings

**Design Runs:**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synth
impl_1	constrs_1	Not started															Vivado Implement

**Left Sidebar (PROJECT MANAGER):**

1. Add Sources (highlighted with a red box)
- Language Templates
- IP Catalog

**Bottom Navigation:**

- Tcl Console
- Messages
- Log
- Reports
- Design Runs

# Create Project (7/8)

Add Sources X

**VIVADO**  
HLx Editions

**Add Sources**  
This guides you through the process of adding and creating sources for your project

**1.**

- Add or create constraints
- Add or create design sources
- Add or create simulation sources

**Constraint**  
**Source code**  
**Testbench**

**2.**

[? Help](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

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# Create Project (8/8)

Add Sources X

**Add or Create Design Sources**

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.



**1.** Add Files Add Directories Create File

Scan and add RTL include files into project  
 Copy sources into project  
 Add sources from subdirectories

**2.** < Back Next > Finish Cancel

# Outline

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# Setting Constraint (1/5)

---

1. All you have to do is setting clock frequency, because the homework only asks you complete running implementation
  
2. There are two ways to set timing constraint
  - A. Create .xdc file and write constraint.
  - B. Use GUI

# Setting Constraint (2/5) (.xdc)

1. Create xdc file.

2. Write the below constraint to .xdc file.

```
create_clock -period 10.000 -name clk -waveform {0.000 5.000}  
[get_ports clk]
```

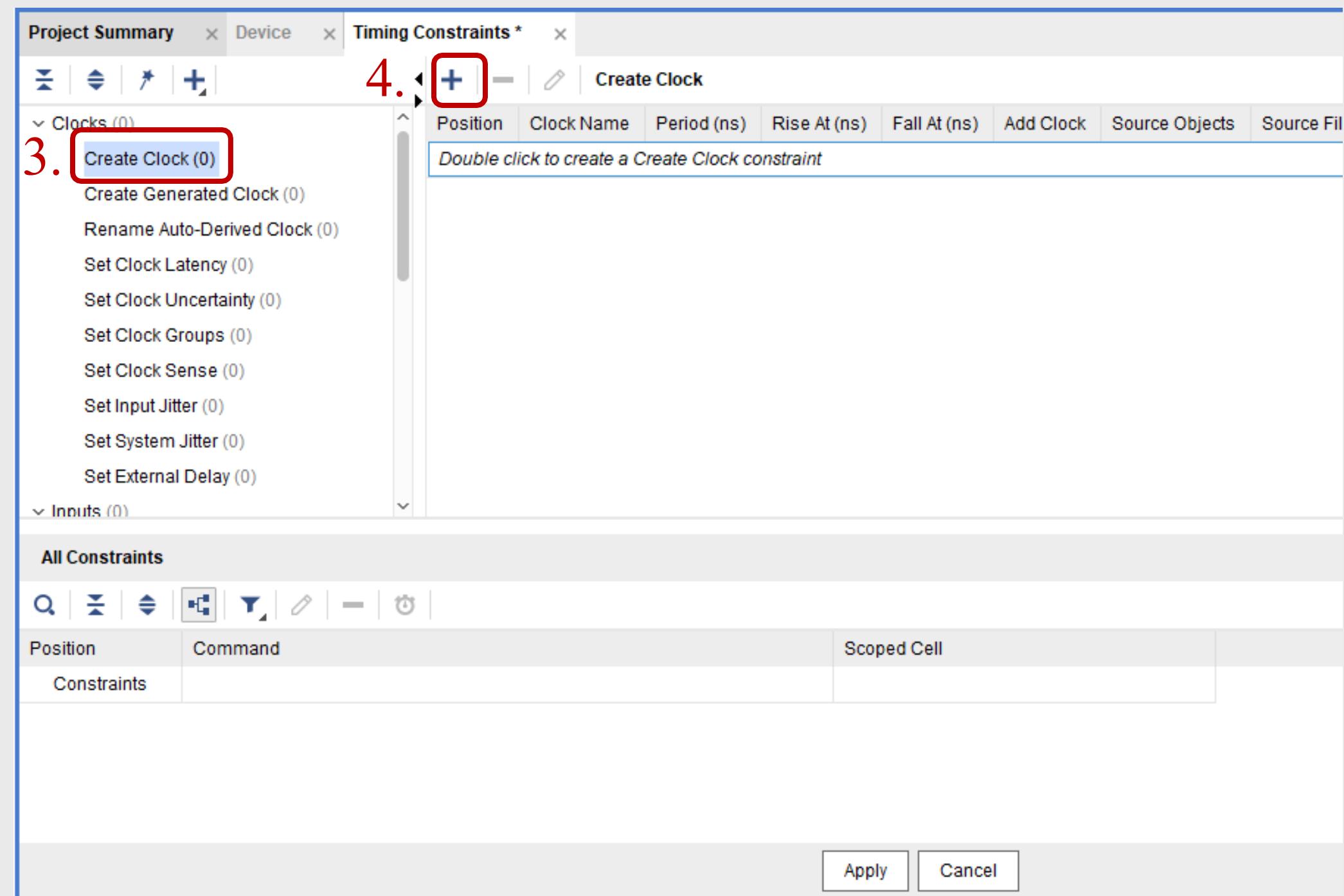
3. Explain :

1. Create\_clock : Create an independent clock source signal
2. {0.000 5.000} : posedge at 0.0ns, negedge at 5.0ns
3. [get\_ports clk] : Send clock signal to clk of Verilog's input port

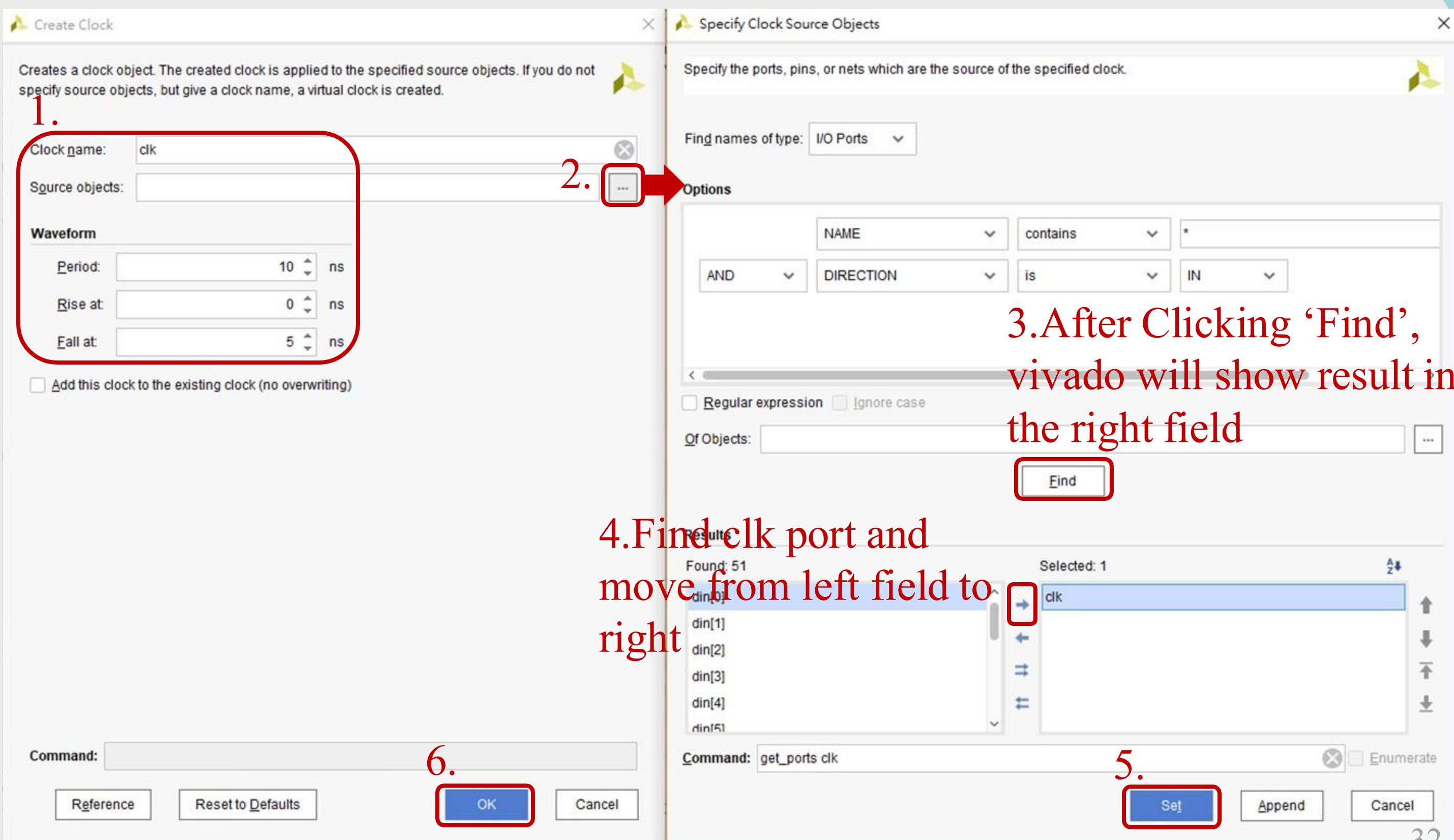
# Setting Constraint (3/5) (GUI)

- ▼ SYNTHESIS
  - ▶ Run Synthesis
  - ▼ Open Synthesized Design
    - Constraints Wizard
  - 2. **Edit Timing Constraints**
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic
- ▼ IMPLEMENTATION
  - ▶ Run Implementation
  - ▼ Open Implemented Design
    - Constraints Wizard
    - Edit Timing Constraints
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction

1. You must run synthesis once after creating project.



# Setting Constraint (4/5) (GUI)



# Setting Constraint (5/5) (GUI)

The screenshot shows the Vivado Timing Constraints interface. The top menu bar includes Project Summary, Device, and Timing Constraints. The main area is titled "Timing Constraints \*".

**Left Panel (Actions):**

- Clocks (1):
  - Create Clock (1)
  - Create Generated Clock (0)
  - Rename Auto-Derived Clock (0)
  - Set Clock Latency (0)
  - Set Clock Uncertainty (0)
  - Set Clock Groups (0)
  - Set Clock Sense (0)
  - Set Input Jitter (0)
  - Set System Jitter (0)
  - Set External Delay (0)
- Inputs (0)

**Top Center (Create Clock):**

Position: 2 | Clock Name: clk | Period (ns): 10.000 | Rise At (ns): 0.000 | Fall At (ns): 5.000 | Add Clock:  | Source Objects: [get\_ports clk] | Source File: <unsaved co...

*Double click to create a Create Clock constraint*

**Bottom Panel (All Constraints):**

Position: 1. | Command: create\_clock -period 10.000 -name clk -waveform {0.000 5.000} [get\_ports clk]

**Buttons:**

Apply | Cancel

**Annotations:**

3. Finally, you have to check the timing constraint written correctly in the .xdc file.
- 2.
- 1.

constraint written correctly in the .xdc file.

# Outline

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# Xsim

(1/7)

The screenshot shows the Xilinx Vivado Flow Navigator interface. The left sidebar lists various project management, IP integration, simulation, RTL analysis, synthesis, implementation, and program/debugging tools. The 'SIMULATION' section is currently selected.

The main window displays the 'Settings' dialog for 'Simulation'. The 'Simulation' tab is active. The configuration includes:

- Target simulator: Vivado Simulator
- Simulator language: Mixed
- Simulation set: sim\_1
- Simulation top module name: men\_TB

Step 1: Click on 'Settings' in the Project Manager.

Step 2: Select 'Simulation' in the Settings dialog.

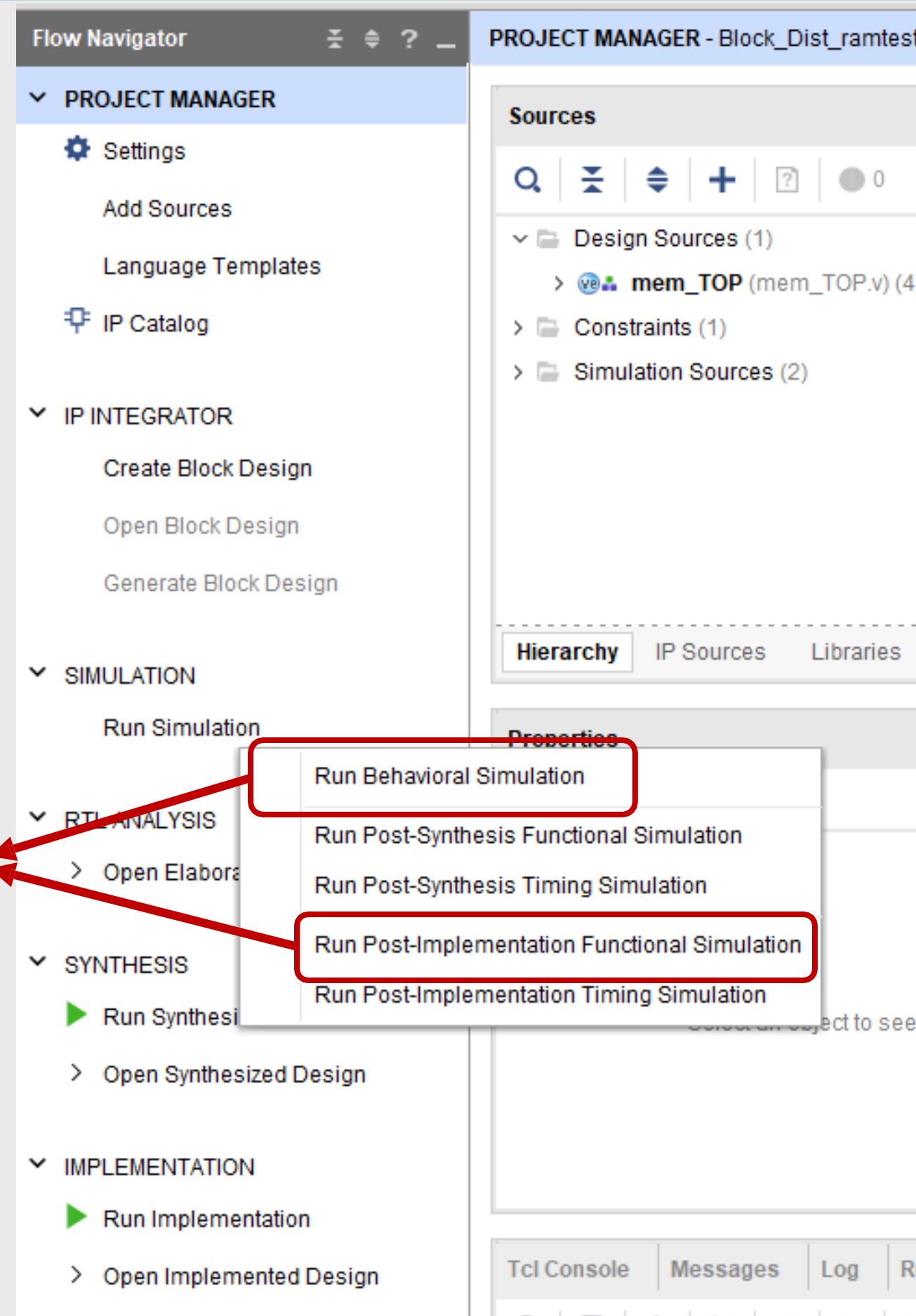
Step 3: Click on the 'Simulation' tab in the Simulation settings.

Step 4: In the 'xsim.simulate.runtime\*' dropdown, enter '-all'.

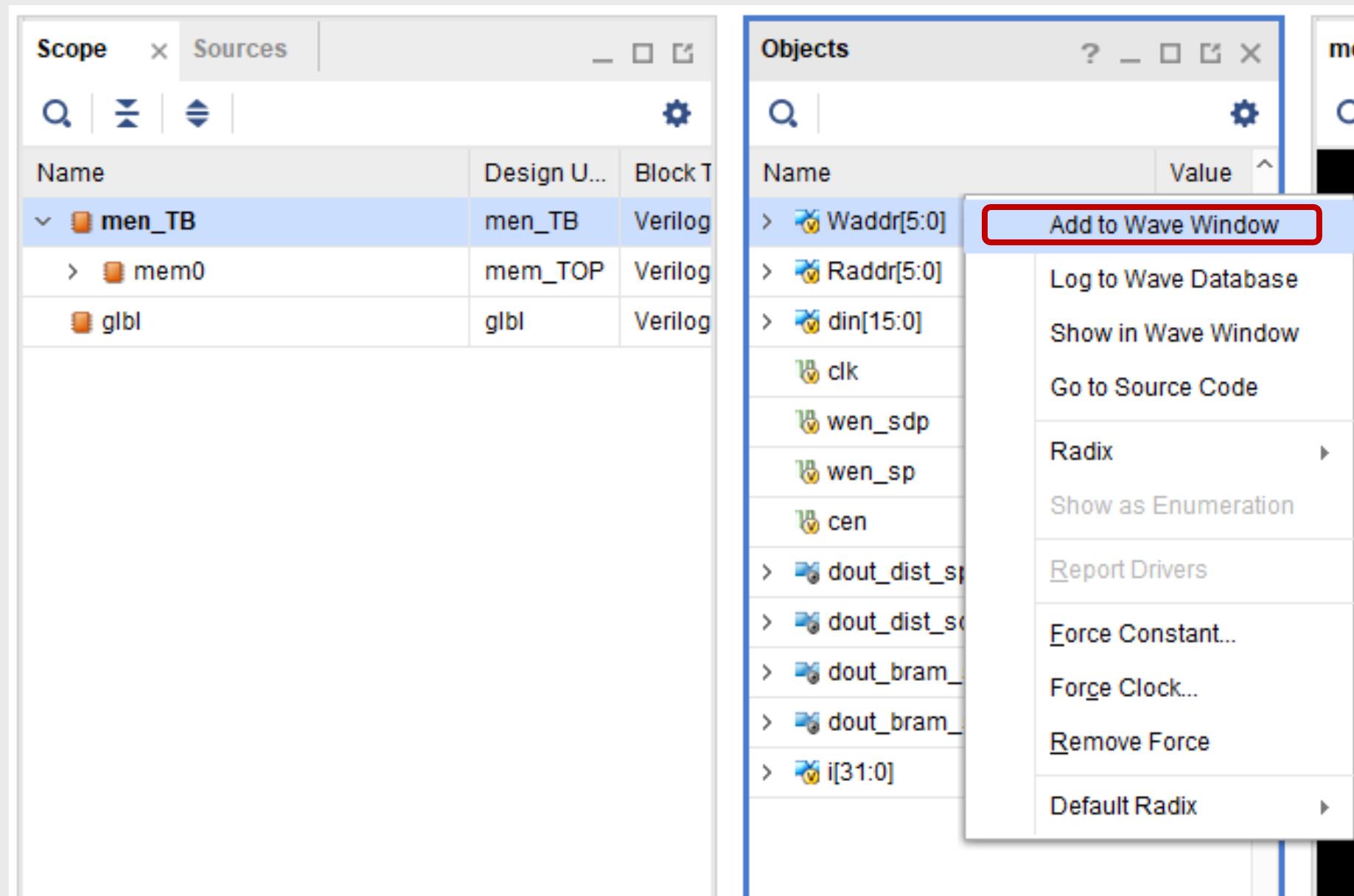
Step 5: Click 'OK' to apply the settings.

Text annotations:

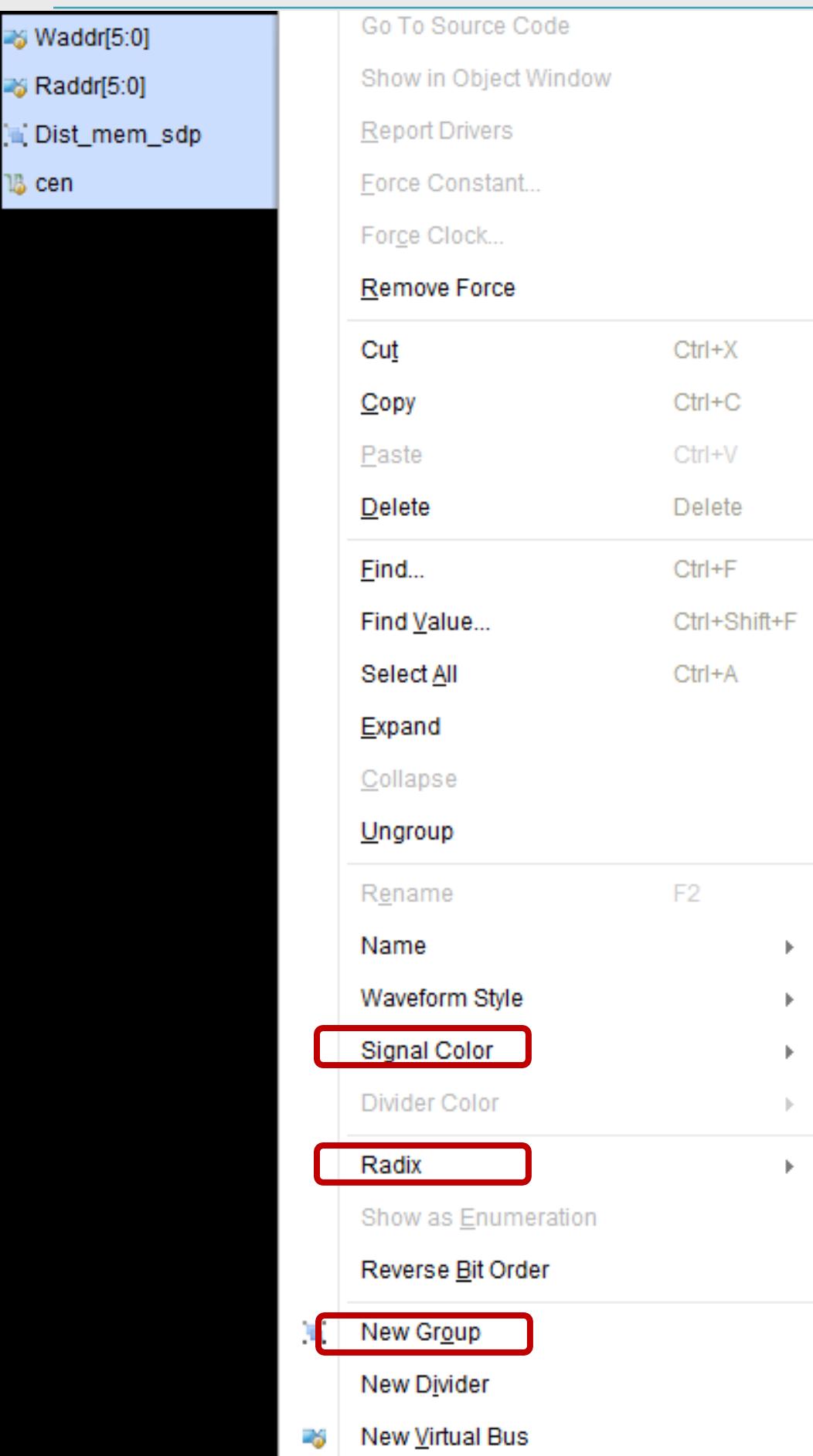
- Step 1: '1.'
- Step 2: '2.'
- Step 3: '3.'
- Step 4: '4.' and 'Enter -all'
- Step 5: '5.'



We mainly use  
these two  
Simulation



- You can add some signals which you want to observe.



- There are three ways to help you observe waveform efficiently.

### 1. New Group :

Fold several signals into one row.

### 2. Signal Color

: Change

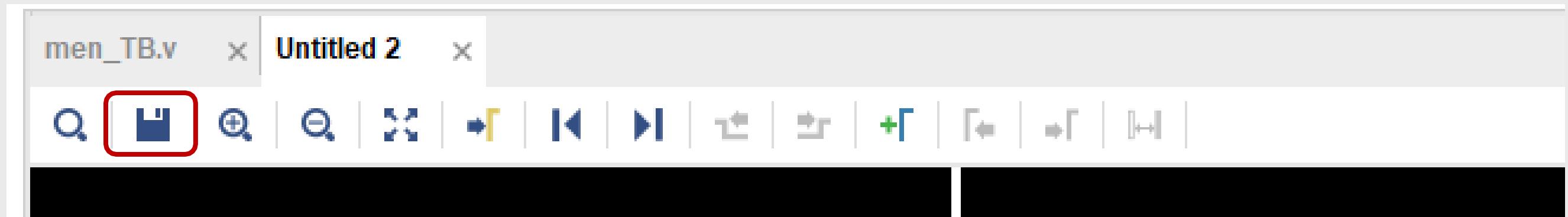
color

### 3. Radix :

1. Dec, Hex, etc.

# Xsim (5/5)

- After you arranged the signals in waveform, you can ‘Save Waveform Configuration’ (.wcfg)



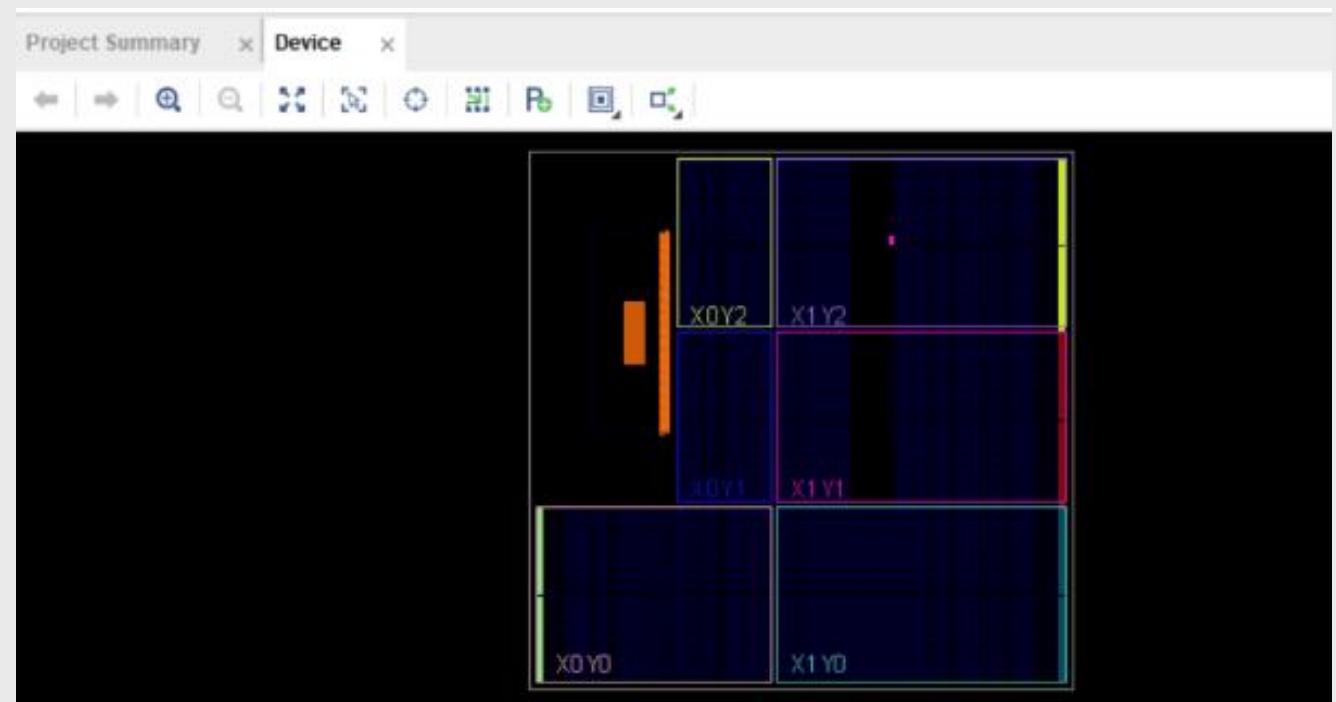
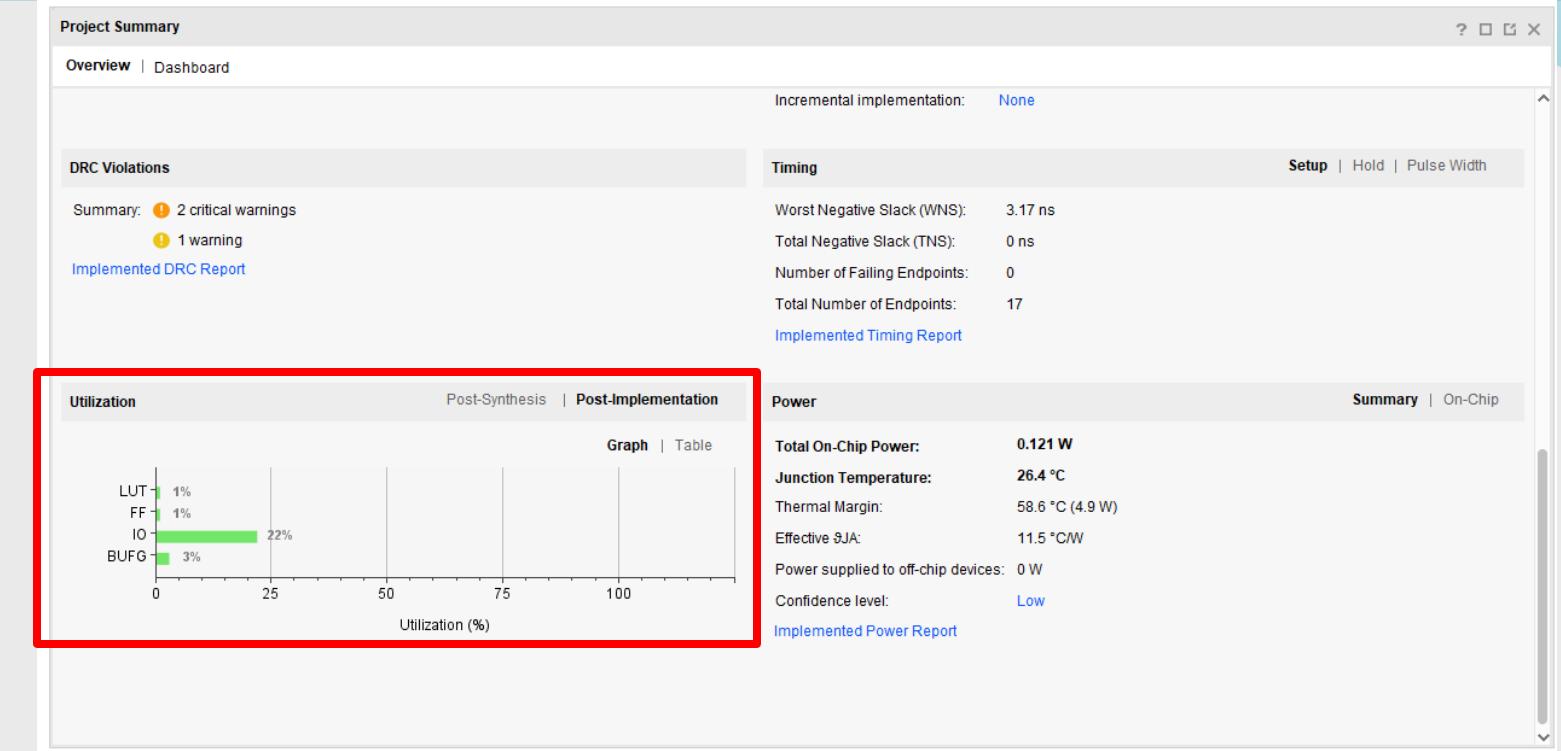
# Outline

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# Synthesis & Implementation (1/3)

- ▼ IP INTEGRATOR
  - [Create Block Design](#)
  - [Open Block Design](#)
  - [Generate Block Design](#)
- ▼ SIMULATION
  - [Run Simulation](#)
- ▼ RTL ANALYSIS
  - > [Open Elaborated Design](#)
- ▼ SYNTHESIS
  - ▶ [Run Synthesis](#)
  - > [Open Synthesized Design](#)
- ▼ IMPLEMENTATION
  - ▶ [Run Implementation](#)
  - > [Open Implemented Design](#)



If you run implementation, vivado will ask you run synthesis first.

# Synthesis & Implementation (2/3)

- If all of the value is black font, this means the implementation is successful.

Tcl Console	Messages	Log	Reports	Design Runs	x	Timing													
Name		Constraints		Status			WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	
✓ synth_1 (active)		constrs_1		Synthesis Out-of-date										0	0	0.00	0	0	
✓ impl_1		constrs_1		Implementation Out-of-date			6.902	0.0...	0.037	0.0...	0.000	0.665	0	40	0	1.00	0	0	

- If implementation didn't success, it will show error part in red font
- Please check if timing violation or area is exceeding the limit.

# Synthesis & Implementation (3/3)

- Resource :
  1. LUT : Look-up table  
Combinational circuit
  2. FF : Flip-Flop  
Register of sequential circuit
  3. BRAM/LUTRAM : Memory
  4. DSP : Digital signal processor  
Special arithmetic (multiplication, division, etc.)
  5. IO :  
Bit number of IO port.
  6. BUFG :  
Usually is used by clock source.

# Outline

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1. Download & Install
2. Setup License
3. Create Project
4. Setting Constraint
5. Xsim
6. Synthesis & Implementation
7. Summary

# Summary (1/3)

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- FPGA Design Flow :
  1. Write Verilog
  2. Behavior Simulation
  3. Setting Constraint
  4. Synthesis
  5. Implementation
  6. Post-Implementation Functional simulation

# Summary (2/3)

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## 2. Design requirement :

- Clock frequency at 100MHz.
- No error and critical warning after running implementation.
- You have to check the warnings will not cause your design incorrect.

# Summary (3/3)

Implementation Complete ✓

Default Layout

Project Summary x Device x MAD.v x MAD\_tb.v x Overview | Dashboard

Synthesis

Status: ✓ Complete

Messages: ! 1 warning

Part: xc7z020clg484-1

Strategy: Vivado Synthesis Defaults

Report Strategy: Vivado Synthesis Default Reports

Implementation

Status: ✓ Complete

Messages: No errors or warnings

Part: xc7z020clg484-1

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Implementation Default Reports

Incremental implementation: None

Summary | Route Status

DRC Violations

Summary: ! 2 critical warnings

! 1 warning

Implemented DRC Report

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS): 3.17 ns

Total Negative Slack (TNS): 0 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 17

Implemented Timing Report

Utilization

Post-Synthesis | Post-Implementation

Graph | Table

LUT 1%  
FF 1%  
IO 22%  
BUFG 3%

Utilization (%)

Power

Summary | On-Chip

Total On-Chip Power: 0.121 W

Junction Temperature: 26.4 °C

Thermal Margin: 58.6 °C (4.9 W)

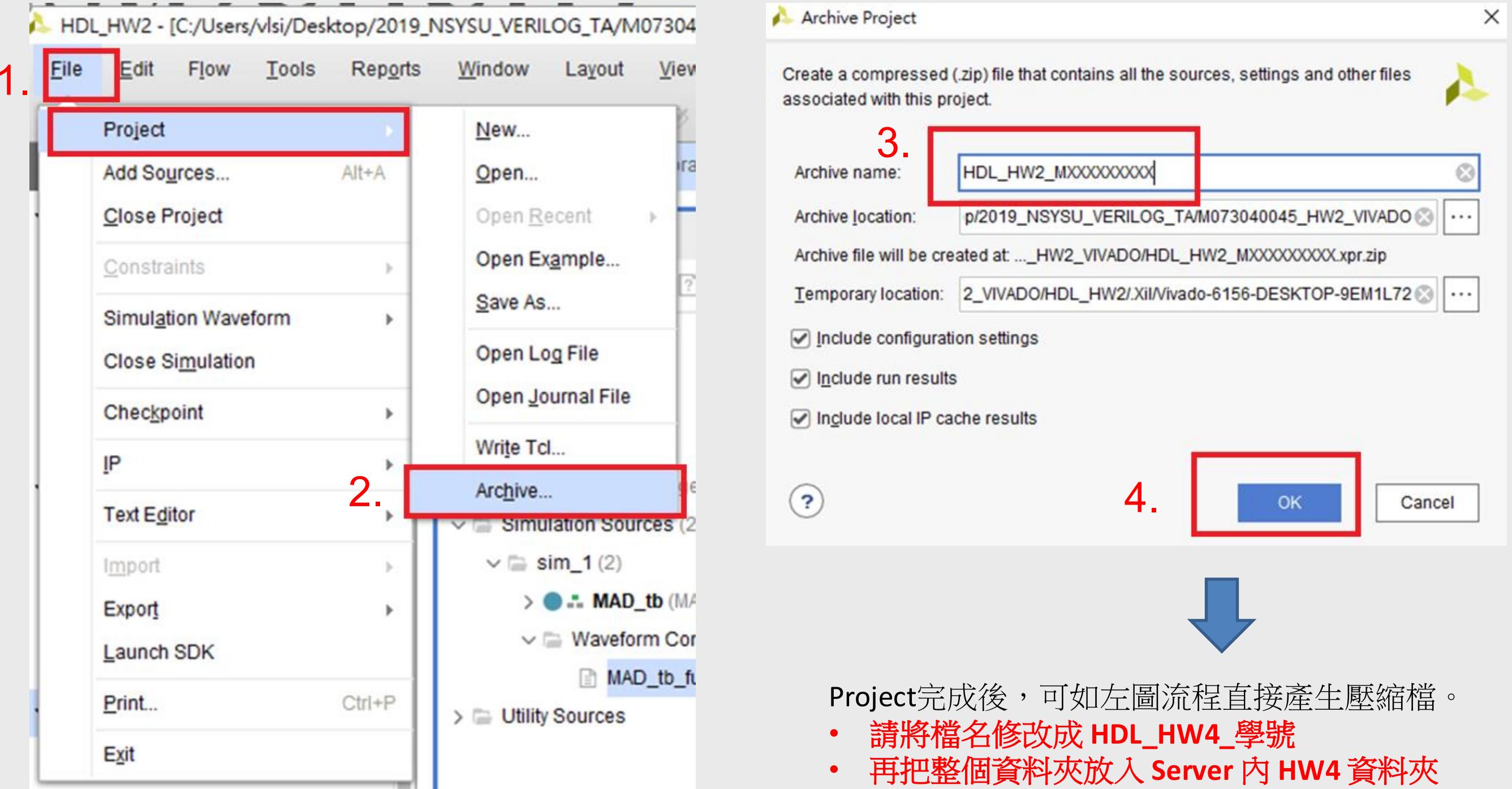
Effective θJA: 11.5 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

Implemented Power Report

# 匯出壓縮檔(.xpr.zip)



Project完成後，可如左圖流程直接產生壓縮檔。

- 請將檔名修改成 **HDL\_HW4\_學號**
- 再把整個資料夾放入 **Server** 內 **HW4** 資料夾
- 繳交整個 **HW4** 資料夾到 **Homework-Submit**