

114 學年度
國立中山大學
硬體描述語言

Homework 3

Pipelined THUMB CPU and Placement and Routing (P&R)

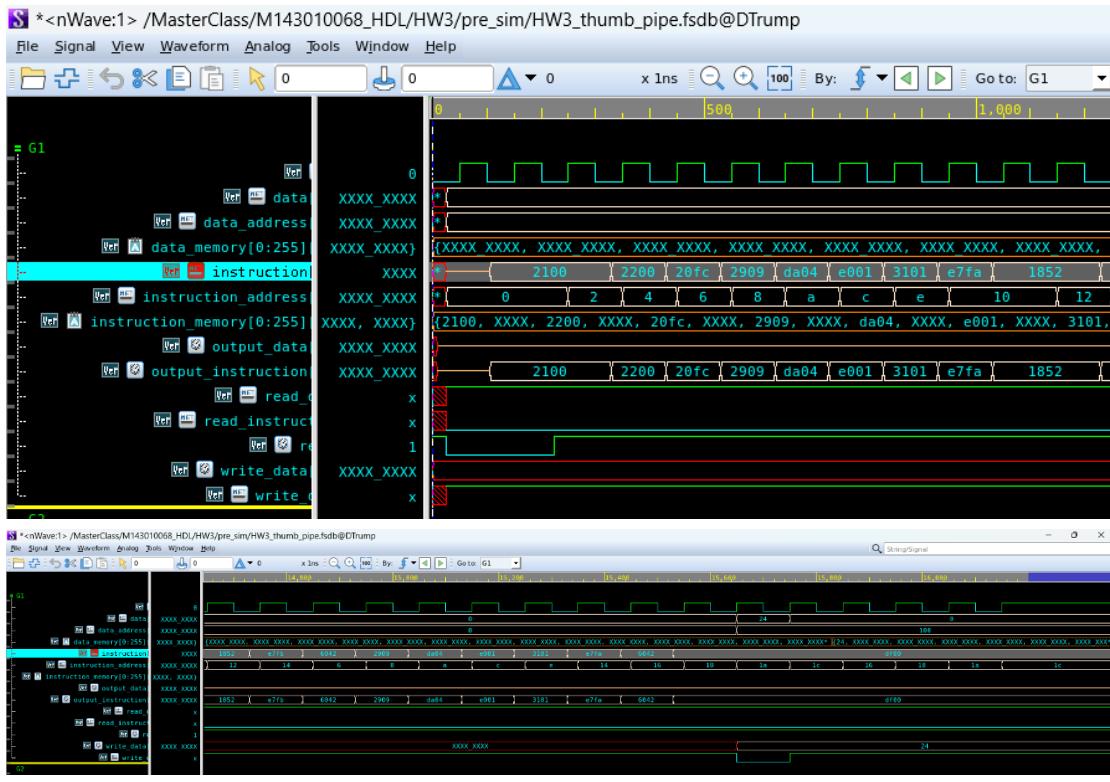
作業

授課教師：蕭勝夫

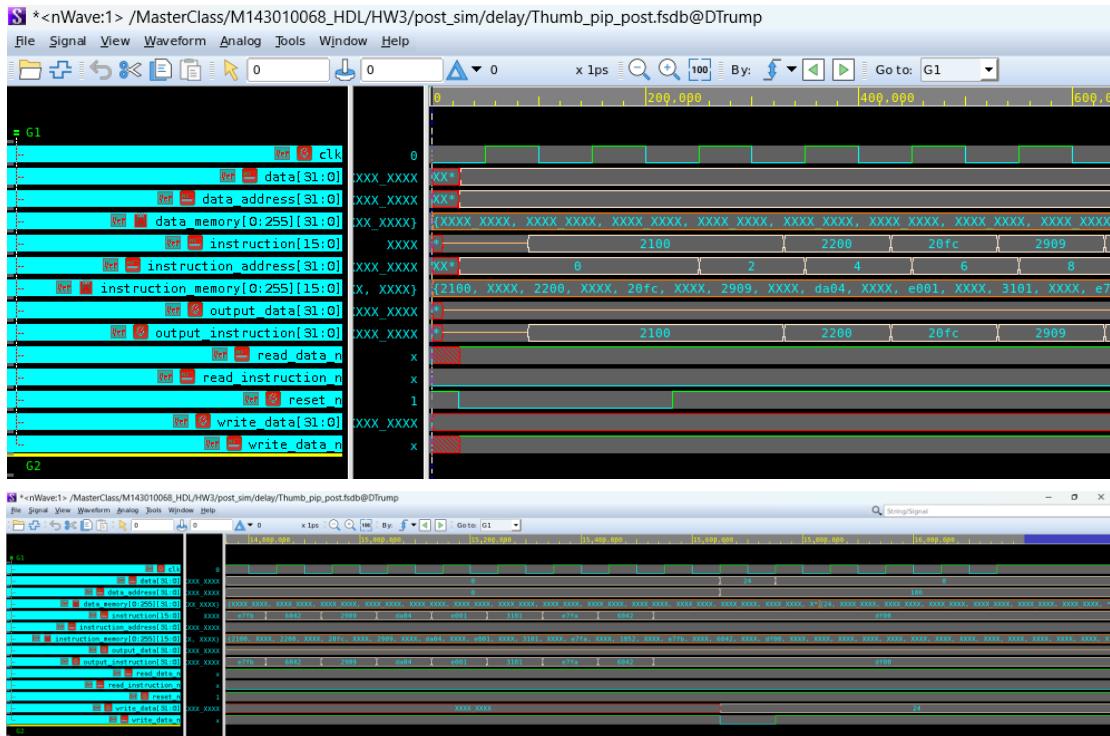
學生學號/班級/姓名：M143010068/電機工程學系碩士班/王嘉良

第一部分：功能驗證模擬

1.1 RTL Level 模擬波形



1.2 Gate Level 模擬波形 (Delay Optimized)



1.3 波形解釋

根據波形圖，可以觀察到因為 thumb 是 16bits 的 instruction，所以是 PC+2，老師給的講義也有說明到這一點，所以在 PC+2 這邊波形圖的顯示皆為正確的

在 16 bits 的 instruction 中，也有發現指令是先 2100, 2200, 20fc, 2909...，表示我們在 testbench 裡面的 instruction memory 有被正確的設定，所以可以做到各個組合語言指令。在 instruction memory 裡面，可以看到各指令間，都有間隔 xxxx，我想是因為 CPU 只會從偶數位址抓取 16 bits 指令，因此奇數位址都沒有被寫入資料，所以模擬器顯示 xxxx。

第二部分：合成數據比較與分析

2.1 數據比較總表

constraint	Area	Delay					Power	
		1 st	2 nd	3 rd	4 th	critical	DC(mW)	PT(mW)
Delay	4849.83	0.86	1.18	1.18	0.55	1.18	2.80	0.0395
Area	4469.74	1.03	1.77	1.77	0.57	1.77	0.5816	0.0373
Mid	4630.24	0.73	1.76	1.76	0.55	1.76	1.0073	0.0389

觀察與發現

在追求 delay 最小的時候，為何達到最快的 critical 速度，付出了 area 跟 power，所以可以看到 area 跟 power 都是最大的，但是在追求 area 的時候，雖然得到最小的 area 跟 power，但是 critical 速度比 delay 還要大，而 mid 正好居中，正好展示了我們的 trade off，

在四個 stage 中，電路的延遲幾乎都是以 ID, EXE 階段決定，大概是因為 ID 要做複雜的 instruction decode，EXE 是算術邏輯單元做運算的地方，所以如果要優化 pipeline 大概從這兩個 stage 下手。

2.2 In-Between (mid) 版本佐證截圖

圖 1：Area Report (DC)

```

1 ****
2
3 Report : area
4 Design : thumb
5 Version: T-2022.03
6 Date   : Thu Nov 13 17:53:00 2025
7 ****
8
9 Library(s) Used:
10
11 N16ADFP_StdCellss0p72vm40c_ccs (File: /cad/CBDK/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell
12
13 Number of ports:          3596
14 Number of nets:           15366
15 Number of cells:          11438
16 Number of combinational cells: 10671
17 Number of sequential cells: 737
18 Number of macros/black boxes: 0
19 Number of buf/inv:         2231
20 Number of references:     11
21
22 Combinational area:      3775.092587
23 Buf/Inv area:            392.739849
24 Noncombinational area:   855.152673
25 Macro/Black Box area:    0.000000
26 Net Interconnect area:  undefined (Wire load has zero net area)
27
28 Total cell area:         4630.245260
29 Total area:              undefined
30
31 Hierarchical area distribution
32 -----
33
34
35
36 Hierarchical cell          Global cell area          Local cell area
37
38 Hierarchical cell           Absolute Total    Percent Total    Combi-national Noncombi-national Black-boxes Design
39
40 thumb                      4630.2453   100.0    29.4970   0.0000   0.0000   thumb
41 step1                     137.3242    3.0     22.0838   91.8605   0.0000   IF
42 step1/r363                 23.3798    0.5     23.3798   0.0000   0.0000   IF_DW01_add_0_DW01_add_15
43 step2                     641.7792   13.9     468.4263  173.3530   0.0000   ID
44 step3                     3332.5863   72.0    1906.0532  271.4342   0.0000   EX
45 step3/add_0_root_add_831_2 32.0371    0.7     32.0371   0.0000   0.0000   EX_DW01_add_4
46 step3/add_1_root_add_779_2 33.1776    0.7     33.1776   0.0000   0.0000   EX_DW01_add_7
47 step3/add_780                25.4016    0.5     25.4016   0.0000   0.0000   EX_DW01_add_6
48 step3/add_781                26.6976    0.6     26.6976   0.0000   0.0000   EX_DW01_add_5
49 step3/add_840_2               32.0371    0.7     32.0371   0.0000   0.0000   EX_DW01_add_3
50 step3/add_849                22.9133    0.5     22.9133   0.0000   0.0000   EX_DW01_add_2
51 step3/add_852                26.9050    0.6     26.9050   0.0000   0.0000   EX_DW01_add_1
52 step3/add_891                22.8614    0.5     22.8614   0.0000   0.0000   EX_DW01_add_0
53 step3/mult_884               492.7911   10.6    492.7911   0.0000   0.0000   EX_DW_mult_0
54 step3/r918                  32.9184    0.7     32.9184   0.0000   0.0000   EX_DW01_add_14
55 step3/r919                  25.1424    0.5     25.1424   0.0000   0.0000   EX_DW01_add_13
56 step3/r920                  25.5571    0.6     25.5571   0.0000   0.0000   EX_DW01_add_12
57 step3/r984                  23.3798    0.5     23.3798   0.0000   0.0000   EX_DW01_add_11
58 step3/r989                  27.8899    0.6     27.8899   0.0000   0.0000   EX_DW01_sub_6
59 step3/r990                  38.0506    0.8     38.0506   0.0000   0.0000   EX_DW01_sub_5
60 step3/r991                  24.7795    0.5     24.7795   0.0000   0.0000   EX_DW01_add_10
61 step3/r992                  25.9200    0.6     25.9200   0.0000   0.0000   EX_DW01_add_9
62 step3/r993                  25.3498    0.5     25.3498   0.0000   0.0000   EX_DW01_add_8
63 step3/sub_0_root_sub_0_root_sub_910_2 38.4134   0.8     38.4134   0.0000   0.0000   EX_DW01_sub_7
64 step3/sub_1_root_sub_0_root_sub_910_2 25.0387   0.5     25.0387   0.0000   0.0000   EX_DW01_sub_8
65 step3/sub_886                29.7562    0.6     29.7562   0.0000   0.0000   EX_DW01_sub_4
66 step3/sub_896                22.8096    0.5     22.8096   0.0000   0.0000   EX_DW01_sub_3
67 step3/sub_918                25.8163    0.6     25.8163   0.0000   0.0000   EX_DW01_sub_2
68 step3/sub_921                26.0755    0.6     26.0755   0.0000   0.0000   EX_DW01_sub_1
69 step3/sub_924                23.3798    0.5     23.3798   0.0000   0.0000   EX_DW01_sub_0
70 step4                      489.0586   10.6    170.5536  318.5050   0.0000   WB
71 Total                       3775.0926   855.1527   0.0000
72
73 1

```

圖 2 : Pipeline Stage Delay - IF (DC)

```

2 ****
3 Report : timing
4     -path full
5     -delay max
6     -max_paths 1
7     -sort_by group
8 Design : thumb
9 Version: T-2022.03
10 Date   : Thu Nov 13 17:53:18 2025
11 ****
12
13 Operating Conditions: ss0p72vm40c Library: N16ADFP_StdCellss0p72vm40c_ccs
14 Wire Load Model Mode: top
15
16 Startpoint: step1/IF_IR_reg_9_
17     (rising edge-triggered flip-flop clocked by clk)
18 Endpoint: step2/ID_Rd_code_reg_2_
19     (rising edge-triggered flip-flop clocked by clk)
20 Path Group: clk
21 Path Type: max
22
23 Des/Clust/Port      Wire Load Model      Library
24 -----
25 thumb              ZeroWireload        N16ADFP_StdCellss0p72vm40c_ccs
26
27 Point                           Incr    Path
28 -----
29 clock clk (rise edge)           0.00    0.00
30 clock network delay (ideal)    0.20    0.20
31 step1/IF_IR_reg_9_/CP (DFCNQND1BWP20P90LVT) 0.00    0.20 r
32 step1/IF_IR_reg_9_/QN (DFCNQND1BWP20P90LVT) 0.08    0.28 r
33 step1/IF_IR[9] (IF) <-
34 step2/IF_IR[9] (ID)            0.00    0.28 r
35 step2/U610/ZN (CKND1BWP16P90LVT) 0.04    0.32 f
36 step2/U375/ZN (ND2D1BWP16P90LVT) 0.02    0.33 r
37 step2/U116/ZN (CKND1BWP16P90LVT) 0.01    0.35 f
38 step2/U114/ZN (ND2D1BWP16P90LVT) 0.01    0.36 r
39 step2/U376/Z (AN3D1BWP16P90LVT) 0.02    0.38 r
40 step2/U368/ZN (IND4D1BWP16P90LVT) 0.02    0.40 f
41 step2/U106/Z (BUFFD1BWP16P90LVT) 0.06    0.46 f
42 step2/U57/ZN (NR2D1BWP16P90LVT) 0.11    0.56 r
43 step2/U56/Z (BUFFD1BWP16P90LVT) 0.03    0.59 r
44 step2/U7/ZN (CKND1BWP16P90LVT) 0.01    0.60 f
45 step2/U652/ZN (OAI2D1BWP16P90LVT) 0.01    0.61 r
46 step2/U649/ZN (ND4D1BWP16P90LVT) 0.02    0.63 f
47 step2/U170/ZN (CKND1BWP16P90LVT) 0.07    0.70 r
48 step2/U162/Z (AO22D1BWP16P90LVT) 0.03    0.73 r
49 step2/ID_Rd_code_reg_2_/D (DFCNQD2BWP16P90LVT) 0.00    0.73 r
50 data arrival time             0.73
51
52 clock clk (rise edge)           2.75    2.75
53 clock network delay (ideal)    0.20    2.95
54 clock uncertainty              -0.02    2.93
55 step2/ID_Rd_code_reg_2_/CP (DFCNQD2BWP16P90LVT) 0.00    2.93 r
56 library setup time             0.00    2.93
57 data required time             2.93
58 -----
59 data required time             2.93
60 data arrival time             -0.73
61 -----
62 slack (MET)                   2.20
63

```

圖 3 : Pipeline Stage Delay - ID (DC)

```

2 ****
3 Report : timing
4   -path full
5   -delay max
6   -max_paths 1
7   -sort_by group
8 Design : thumb
9 Version: T-2022.03
10 Date  : Thu Nov 13 17:53:18 2025
11 ****
12
13 Operating Conditions: ss0p72vm40c Library: N16ADFP_StdCellss0p72vm40c_ccs
14 Wire Load Model Mode: top
15
16 Startpoint: step2/ID_Rm_Rs_reg_2_
17   (rising edge-triggered flip-flop clocked by clk)
18 Endpoint: step3/Z_flag_reg
19   (rising edge-triggered flip-flop clocked by clk)
20 Path Group: clk
21 Path Type: max
22
23 Des/Clust/Port      Wire Load Model      Library
24 -----
25 thumb                ZeroWireload        N16ADFP_StdCellss0p72vm40c_ccs
26
27 Point                      Incr      Path
28 -----
29 clock clk (rise edge)          0.00    0.00
30 clock network delay (ideal)  0.20    0.20
31 step2/ID_Rm_Rs_reg_2/_CP (DFCNQD2BWP16P90LVT) 0.00    0.20 r
32 step2/ID_Rm_Rs_reg_2/_Q (DFCNQD2BWP16P90LVT)  0.10    0.30 f
33 step2/ID_Rm_Rs[2] (ID) <-
34 step3/ID_Rm_Rs[2] (EX)          0.00    0.30 f
35 step3/U3633/Z (BUFD1BWP16P90LVT) 0.19    0.49 f
36 step3/mult_884/b[2] (EX_DW_mult_uns_0) 0.00    0.49 f
37 step3/mult_884/U1059/C0 (FA1D1BWP16P90LVT) 0.06    0.55 f
38 step3/mult_884/U1058/C0 (FA1D1BWP16P90LVT) 0.03    0.58 f
39 step3/mult_884/U1057/C0 (FA1D1BWP16P90LVT) 0.03    0.61 f
40 step3/mult_884/U1056/C0 (FA1D1BWP16P90LVT) 0.03    0.64 f
41 step3/mult_884/U1055/C0 (FA1D1BWP16P90LVT) 0.03    0.67 f
42 step3/mult_884/U1054/C0 (FA1D1BWP16P90LVT) 0.03    0.69 f
43 step3/mult_884/U1053/C0 (FA1D1BWP16P90LVT) 0.03    0.72 f
44 step3/mult_884/U1052/C0 (FA1D1BWP16P90LVT) 0.03    0.75 f
45 step3/mult_884/U1051/C0 (FA1D1BWP16P90LVT) 0.03    0.78 f
46 step3/mult_884/U1050/C0 (FA1D1BWP16P90LVT) 0.03    0.81 f
47 step3/mult_884/U1049/C0 (FA1D1BWP16P90LVT) 0.03    0.84 f
48 step3/mult_884/U1048/S (FA1D1BWP16P90LVT) 0.05    0.88 r
49 step3/mult_884/U1255/ZN (AOI22D1BWP16P90) 0.02    0.90 f
50 step3/mult_884/U1254/ZN (AOI22D1BWP16P90) 0.02    0.92 r
51 step3/mult_884/U1253/ZN (XNR2D1BWP16P90) 0.04    0.96 f
52 step3/mult_884/U158/C0 (FA1D1BWP16P90LVT) 0.03    0.99 f
53 step3/mult_884/U157/C0 (FA1D1BWP16P90LVT) 0.03    1.02 f
54 step3/mult_884/U156/C0 (FA1D1BWP16P90LVT) 0.03    1.05 f
55 step3/mult_884/U155/C0 (FA1D1BWP16P90LVT) 0.03    1.07 f
56 step3/mult_884/U154/C0 (FA1D1BWP16P90LVT) 0.03    1.10 f
57 step3/mult_884/U153/C0 (FA1D1BWP16P90LVT) 0.03    1.13 f
58 step3/mult_884/U152/C0 (FA1D1BWP16P90LVT) 0.03    1.16 f
59 step3/mult_884/U151/C0 (FA1D1BWP16P90LVT) 0.03    1.19 f
60 step3/mult_884/U150/C0 (FA1D1BWP16P90LVT) 0.03    1.21 f
61 step3/mult_884/U149/C0 (FA1D1BWP16P90LVT) 0.03    1.24 f
62 step3/mult_884/U148/C0 (FA1D1BWP16P90LVT) 0.03    1.27 f
63 step3/mult_884/U147/C0 (FA1D1BWP16P90LVT) 0.03    1.30 f
64 step3/mult_884/U146/C0 (FA1D1BWP16P90LVT) 0.03    1.32 f
65 step3/mult_884/U145/C0 (FA1D1BWP16P90LVT) 0.03    1.35 f
66 step3/mult_884/U144/C0 (FA1D1BWP16P90LVT) 0.03    1.38 f
67 step3/mult_884/U143/C0 (FA1D1BWP16P90LVT) 0.03    1.41 f
68 step3/mult_884/U142/C0 (FA1D1BWP16P90LVT) 0.03    1.43 f
69 step3/mult_884/U141/C0 (FA1D1BWP16P90LVT) 0.03    1.46 f
70 step3/mult_884/U1182/ZN (XNR3D1BWP16P90) 0.05    1.51 r
71 step3/mult_884/U1181/Z (XOR4D1BWP16P90) 0.07    1.58 f
72 step3/mult_884/product[31] (EX_DW_mult_uns_0) 0.00    1.58 f
73 step3/U5307/ZN (AOI22D1BWP16P90) 0.03    1.62 r
74 step3/U5308/ZN (ND4D1BWP16P90) 0.03    1.64 f
75 step3/U5317/ZN (AOI22D1BWP16P90) 0.02    1.66 r
76 step3/U5327/ZN (ND3D1BWP16P90) 0.02    1.69 f
77 step3/U3623/ZN (AOI2D1BWP16P90LVT) 0.02    1.71 r
78 step3/U3071/ZN (ND4D1BWP16P90LVT) 0.02    1.72 f
79 step3/U3073/ZN (NR4D1BWP16P90LVT) 0.01    1.74 r
80 step3/U3625/ZN (AOI22D1BWP16P90LVT) 0.01    1.75 f
81 step3/U3624/ZN (IOA22D1BWP16P90LVT) 0.01    1.76 r
82 step3/Z_flag_reg/D (DFCNQD2BWP16P90LVT) 0.00    1.76 r
83 data arrival time           1.76
84
85 clock clk (rise edge)          2.75    2.75
86 clock network delay (ideal)  0.20    2.95
87 clock uncertainty            -0.02    2.93
88 step3/Z_flag_reg/CP (DFCNQD2BWP16P90LVT) 0.00    2.93 r
89 library setup time           0.00    2.93
90 data required time           2.93
91 data arrival time             -1.76
92
93 slack (MET)                  1.17

```

圖 4 : Pipeline Stage Delay - EX (DC)

```

2 ****
3 Report : timing
4     -path full
5     -delay max
6     -max_paths 1
7     -sort_by group
8 Design : thumb
9 Version: T-2022.03
10 Date  : Thu Nov 13 17:53:18 2025
11 ****
12
13 Operating Conditions: ss0p72vm40c Library: NI6ADFP_StdCellss0p72vm40c_ccs
14 Wire Load Model Mode: top
15
16 Startpoint: step2/ID_Rm_Rs_reg_2_
17     (rising edge-triggered flip-flop clocked by clk)
18 Endpoint: step3/Z_Flag_reg
19     (rising edge-triggered flip-flop clocked by clk)
20 Path Group: clk
21 Path Type: max
22
23 Des/Clust/Port      Wire Load Model      Library
24 -----
25 thumb                ZeroWireload        NI6ADFP_StdCellss0p72vm40c_ccs
26
27 Point                      Incr      Path
28 -----
29 clock clk (rise edge)          0.00      0.00
30 clock network delay (ideal)   0.20      0.20
31 step2/ID_Rm_Rs_reg_2_/CP (DFCNQD2BWP16P90LVT) 0.00      0.20 r
32 step2/ID_Rm_Rs_reg_2_/Q (DFCNQD2BWP16P90LVT) 0.10      0.30 f
33 step2/ID_Rm_Rs[2] (ID)        0.00      0.30 f
34 step3/ID_Rm_Rs[2] (EX) <-
35 step3/U3633/Z (BUFFD1BWP16P90LVT) 0.19      0.49 f
36 step3/mult_884/U1059/co (FA1D1BWP16P90LVT) 0.00      0.49 f
37 step3/mult_884/U1059/co (FA1D1BWP16P90LVT) 0.06      0.55 f
38 step3/mult_884/U1058/co (FA1D1BWP16P90LVT) 0.03      0.58 f
39 step3/mult_884/U1057/co (FA1D1BWP16P90LVT) 0.03      0.61 f
40 step3/mult_884/U1056/co (FA1D1BWP16P90LVT) 0.03      0.64 f
41 step3/mult_884/U1055/co (FA1D1BWP16P90LVT) 0.03      0.67 f
42 step3/mult_884/U1054/co (FA1D1BWP16P90LVT) 0.03      0.69 f
43 step3/mult_884/U1053/co (FA1D1BWP16P90LVT) 0.03      0.72 f
44 step3/mult_884/U1052/co (FA1D1BWP16P90LVT) 0.03      0.75 f
45 step3/mult_884/U1051/co (FA1D1BWP16P90LVT) 0.03      0.78 f
46 step3/mult_884/U1050/co (FA1D1BWP16P90LVT) 0.03      0.81 f
47 step3/mult_884/U1049/co (FA1D1BWP16P90LVT) 0.03      0.84 f
48 step3/mult_884/U1048/s (FA1D1BWP16P90LVT) 0.05      0.88 r
49 step3/mult_884/U1255/zn (AOI22D1BWP16P90) 0.02      0.90 f
50 step3/mult_884/U1254/zn (AOI22D1BWP16P90) 0.02      0.92 r
51 step3/mult_884/U1253/zn (XNR2D1BWP16P90) 0.04      0.96 f
52 step3/mult_884/U158/co (FA1D1BWP16P90LVT) 0.03      0.99 f
53 step3/mult_884/U157/co (FA1D1BWP16P90LVT) 0.03      1.02 f
54 step3/mult_884/U156/co (FA1D1BWP16P90LVT) 0.03      1.05 f
55 step3/mult_884/U155/co (FA1D1BWP16P90LVT) 0.03      1.07 f
56 step3/mult_884/U154/co (FA1D1BWP16P90LVT) 0.03      1.10 f
57 step3/mult_884/U153/co (FA1D1BWP16P90LVT) 0.03      1.13 f
58 step3/mult_884/U152/co (FA1D1BWP16P90LVT) 0.03      1.16 f
59 step3/mult_884/U151/co (FA1D1BWP16P90LVT) 0.03      1.19 f
60 step3/mult_884/U150/co (FA1D1BWP16P90LVT) 0.03      1.21 f
61 step3/mult_884/U149/co (FA1D1BWP16P90LVT) 0.03      1.24 f
62 step3/mult_884/U148/co (FA1D1BWP16P90LVT) 0.03      1.27 f
63 step3/mult_884/U147/co (FA1D1BWP16P90LVT) 0.03      1.30 f
64 step3/mult_884/U146/co (FA1D1BWP16P90LVT) 0.03      1.32 f
65 step3/mult_884/U145/co (FA1D1BWP16P90LVT) 0.03      1.35 f
66 step3/mult_884/U144/co (FA1D1BWP16P90LVT) 0.03      1.38 f
67 step3/mult_884/U143/co (FA1D1BWP16P90LVT) 0.03      1.41 f
68 step3/mult_884/U142/co (FA1D1BWP16P90LVT) 0.03      1.43 f
69 step3/mult_884/U141/co (FA1D1BWP16P90LVT) 0.03      1.46 f
70 step3/mult_884/U1182/zn (XNR3D1BWP16P90) 0.05      1.51 r
71 step3/mult_884/U1181/z (XOR4D1BWP16P90) 0.07      1.58 f
72 step3/mult_884/product[31] (EX_DW_mult_0) 0.00      1.58 f
73 step3/U5307/zn (AOI22D1BWP16P90) 0.03      1.62 r
74 step3/U5308/zn (ND4D1BWP16P90) 0.03      1.64 f
75 step3/U5317/zn (AOI22D1BWP16P90) 0.02      1.66 r
76 step3/U5327/zn (ND3D1BWP16P90) 0.02      1.69 f
77 step3/U3623/zn (AOI22D1BWP16P90LVT) 0.02      1.71 r
78 step3/U3071/zn (ND4D1BWP16P90LVT) 0.02      1.72 f
79 step3/U3073/zn (NR4D1BWP16P90LVT) 0.01      1.74 r
80 step3/U3625/zn (AOI22D1BWP16P90LVT) 0.01      1.75 f
81 step3/U3624/zn (IOA22D1BWP16P90LVT) 0.01      1.76 r
82 step3/Z_Flag_reg/D (DFCNQD2BWP16P90LVT) 0.00      1.76 r
83 data arrival time                         1.76
84
85 clock clk (rise edge)                    2.75      2.75
86 clock network delay (ideal)            0.20      2.95
87 clock uncertainty                     -0.02      2.93
88 step3/Z_Flag_reg/CP (DFCNQD2BWP16P90LVT) 0.00      2.93 r
89 library setup time                   0.00      2.93
90 data required time                  2.93
91 data arrival time                   -1.76
92
93 slack (MET)                           1.17

```

圖 5 : Pipeline Stage Delay - WB (DC)

```

2 ****
3 Report : timing
4     -path full
5     -delay max
6     -max_paths 1
7     -sort_by group
8 Design : thumb
9 Version: T-2022.03
10 Date   : Thu Nov 13 17:53:18 2025
11 ****
12
13 Operating Conditions: ss0p72vm40c  Library: N16ADFP_StdCellss0p72vm40c_ccs
14 Wire Load Model Mode: top
15
16 Startpoint: step3/write_data_n_reg
17     (rising edge-triggered flip-flop clocked by clk)
18 Endpoint: step4/R_reg_3_31_
19     (rising edge-triggered flip-flop clocked by clk)
20 Path Group: clk
21 Path Type: max
22
23 Des/Clust/Port      Wire Load Model      Library
24 -----
25 thumb                ZeroWireload        N16ADFP_StdCellss0p72vm40c_ccs
26
27 Point                           Incr      Path
28 -----
29 clock clk (rise edge)          0.00      0.00
30 clock network delay (ideal)  0.20      0.20
31 step3/write_data_n_reg/CP (DFCNQND1BWP16P90LVT) 0.00      0.20 r
32 step3/write_data_n_reg/QN (DFCNQND1BWP16P90LVT) 0.06      0.26 r
33 step3/write_data_n (EX)       0.00      0.26 r
34 U145/Z (BUFFD1BWP16P90LVT)  0.01      0.27 r
35 U116/Z (BUFFD1BWP16P90LVT)  0.01      0.29 r
36 U107/Z (BUFFD1BWP16P90LVT)  0.01      0.30 r
37 U26/ZN (OAI22D1BWP16P90)    0.02      0.32 f
38 U70/Z (CKBD1BWP20P90)       0.09      0.41 f
39 step4/data[7] (WB) <-      0.00      0.41 f
40 step4/U424/ZN (INR2D1BWP16P90LVT) 0.03      0.43 f
41 step4/U408/ZN (AOI21D1BWP16P90LVT) 0.06      0.49 r
42 step4/U505/Z (AN2D1BWP16P90LVT)  0.03      0.53 r
43 step4/U343/ZN (MAOI22D1BWP16P90LVT) 0.02      0.55 r
44 step4/R_reg_3_31_/D (DFCNQND1BWP16P90LVT) 0.00      0.55 r
45 data arrival time           0.55
46
47 clock clk (rise edge)          2.75      2.75
48 clock network delay (ideal)  0.20      2.95
49 clock uncertainty            -0.02      2.93
50 step4/R_reg_3_31_/CP (DFCNQND1BWP16P90LVT) 0.00      2.93 r
51 library setup time           -0.01      2.92
52 data required time           2.92
53
54 data required time           2.92
55 data arrival time           -0.55
56
57 slack (MET)                  2.38

```

圖 6 : Power Report (DC)

```

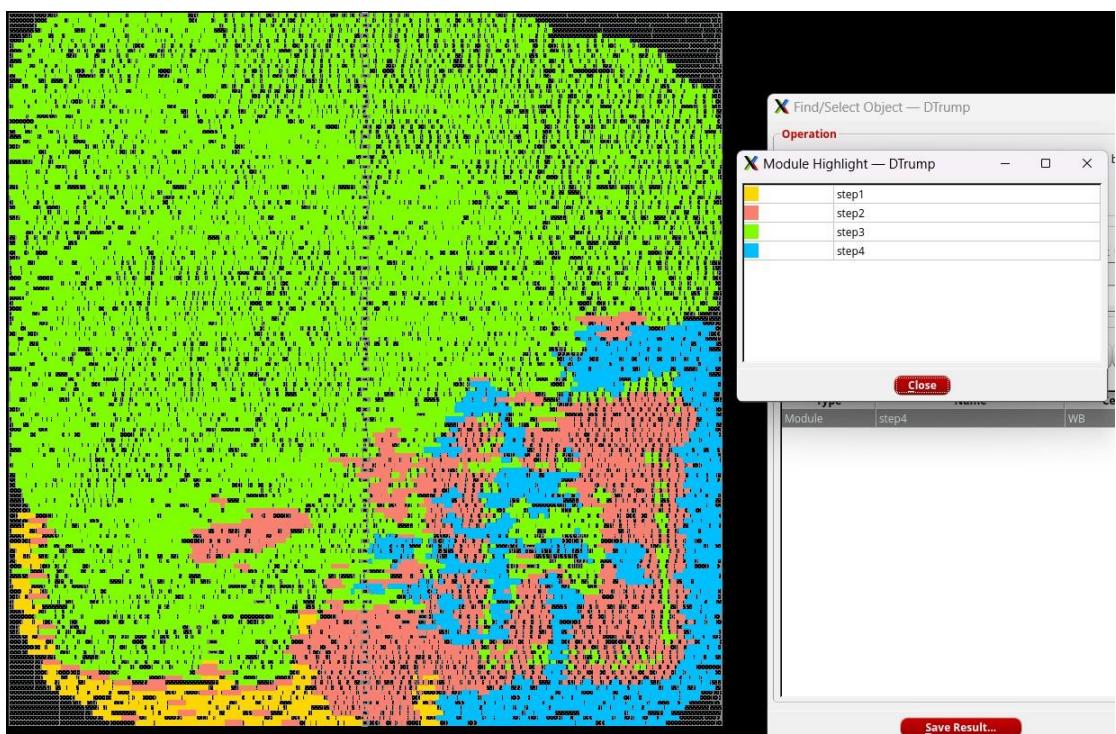
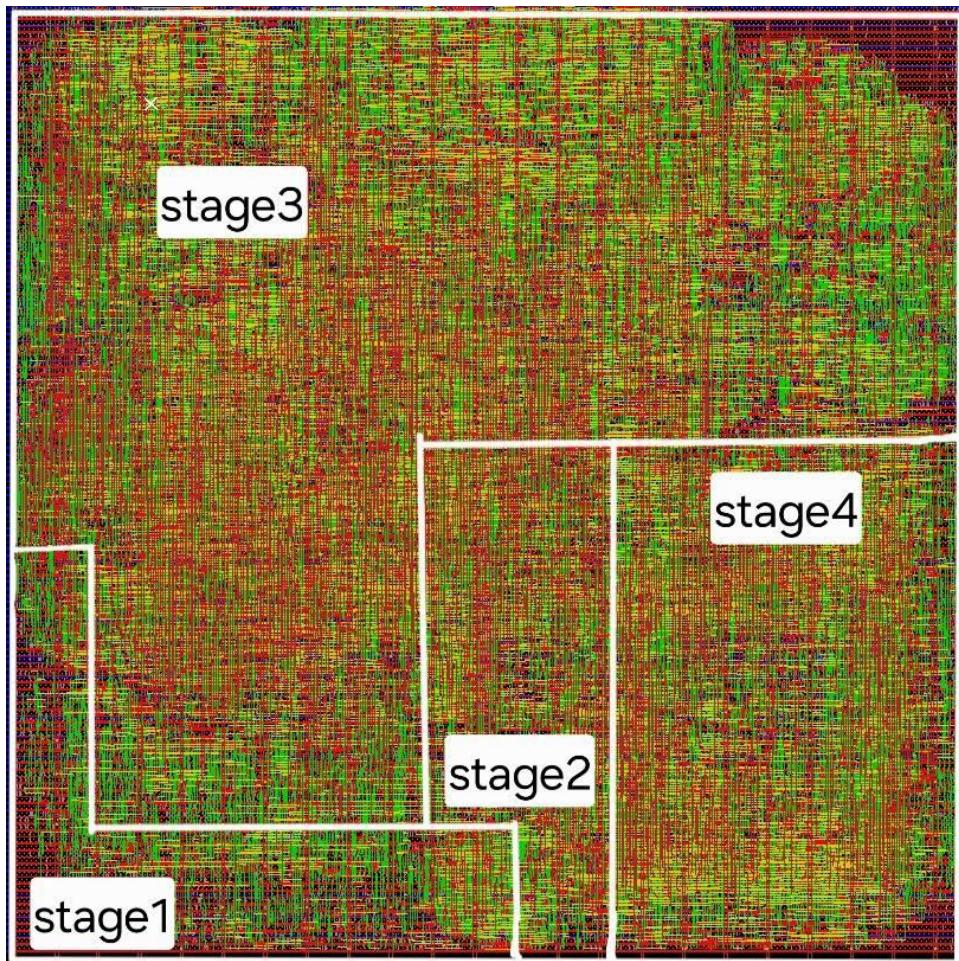
6 ****
7 Report : power
8     -analysis_effort low
9 Design : thumb
10 Version: T-2022.03
11 Date  : Thu Nov 13 17:53:17 2025
12 ****
13
14 Library(s) Used:
15
16     N16ADFP_StdCellss0p72vm40c_ccs (File: /cad/CBDK/ADFP/Executable_Package/Collaterals/IP/stdcell/N16A
17
18
19 Operating Conditions: ss0p72vm40c   Library: N16ADFP_StdCellss0p72vm40c_ccs
20 Wire Load Model Mode: top
21
22 Design      Wire Load Model      Library
23 -----
24 thumb        ZeroWireload      N16ADFP_StdCellss0p72vm40c_ccs
25
26
27 Global Operating Voltage = 0.72
28 Power-specific unit information :
29     Voltage Units = 1V
30     Capacitance Units = 1.000000pf
31     Time Units = 1ns
32     Dynamic Power Units = 1mW    (derived from V,C,T units)
33     Leakage Power Units = 1nW
34
35
36 Attributes
37 -----
38 i - Including register clock pin internal power
39
40
41 Cell Internal Power = 819.1270 uW (82%)
42 Net Switching Power = 185.4840 uW (18%)
43
44 -----
45 Total Dynamic Power = 1.0046 mW (100%)
46
47 Cell Leakage Power = 2.7284 uW
48
49
50 Power Group      Internal Power      Switching Power      Leakage Power      Total Power ( % ) Attrs
51 -----
52 io_pad          0.0000            0.0000            0.0000            0.0000 ( 0.00%)
53 memory          0.0000            0.0000            0.0000            0.0000 ( 0.00%)
54 black_box        0.0000            0.0000            0.0000            0.0000 ( 0.00%)
55 clock_network   0.6450            0.0000            0.0000            0.0000 ( 0.00%) i
56 register         2.5310e-02       1.9348e-02       468.7749          0.6901 ( 68.52%)
57 sequential        0.0000            0.0000            0.0000            0.0000 ( 0.00%)
58 combinational    0.1488            0.1661           2.2596e+03       0.3171 ( 31.48%)
59
60 -----
61 Total           0.8191 mW        0.1854 mW        2.7284e+03 nW       1.0073 mW

```

圖 7 : Power Report (PT)

	Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
1	*****					
2	Report : Averaged Power					
3	-hierarchy					
4	Design : thumb					
5	Version: V-2023.12					
6	Date : Thu Nov 13 19:37:36 2025					
7	*****					
8						
9						
10						
11						
12						
13	-----					
14	thumb	2.62e-05	9.77e-06	2.85e-06	3.89e-05	100.0
15	step1 (IF)	2.17e-06	2.35e-07	9.15e-08	2.49e-06	6.4
16	r363 (IF_DW01_add_0_DW01_add_15)	2.62e-08	1.28e-08	1.92e-08	5.82e-08	0.1
17	step2 (ID)	6.98e-06	4.30e-06	2.82e-07	1.16e-05	29.8
18	step3 (EX)	1.08e-05	4.80e-06	2.18e-06	1.78e-05	45.7
19	add_1_root_add_779_2 (EX_DW01_add_7)	1.83e-08	4.87e-09	1.79e-08	4.11e-08	0.1
20	add_780 (EX_DW01_add_6)	3.21e-08	1.05e-08	2.03e-08	6.29e-08	0.2
21	add_781 (EX_DW01_add_5)	5.45e-08	1.68e-08	2.14e-08	9.27e-08	0.2
22	add_840_2 (EX_DW01_add_3)	2.13e-07	7.58e-08	1.80e-08	3.07e-07	0.8
23	add_849 (EX_DW01_add_2)	3.89e-08	1.21e-08	1.55e-08	6.65e-08	0.2
24	add_852 (EX_DW01_add_1)	2.20e-08	1.57e-08	1.93e-08	5.70e-08	0.1
25	sub_1_root_sub_0_root_sub_910_2 (EX_DW01_sub_8)	1.72e-08	1.38e-08	2.27e-08	5.38e-08	0.1
26	sub_886 (EX_DW01_sub_4)	1.19e-08	5.30e-09	2.75e-08	4.47e-08	0.1
27	sub_896 (EX_DW01_sub_3)	0.000	0.000	2.22e-08	2.22e-08	0.1
28	add_891 (EX_DW01_add_0)	0.000	0.000	2.21e-08	2.21e-08	0.1
29	sub_0_root_sub_0_root_sub_910_2 (EX_DW01_sub_7)	2.12e-08	7.13e-09	1.76e-08	4.59e-08	0.1
30	r918 (EX_DW01_add_14)	2.20e-08	1.78e-08	1.90e-08	5.87e-08	0.2
31	r919 (EX_DW01_add_13)	7.27e-08	2.37e-08	1.85e-08	1.15e-07	0.3
32	r920 (EX_DW01_add_12)	9.79e-09	6.43e-09	2.03e-08	3.65e-08	0.1
33	r984 (EX_DW01_add_11)	2.12e-08	3.20e-08	1.92e-08	7.25e-08	0.2
34	r989 (EX_DW01_sub_6)	1.76e-07	7.97e-08	2.50e-08	2.81e-07	0.7
35	r990 (EX_DW01_sub_5)	3.10e-08	1.19e-08	1.75e-08	6.04e-08	0.2
36	r991 (EX_DW01_add_10)	5.99e-08	2.05e-08	1.93e-08	9.96e-08	0.3
37	r992 (EX_DW01_add_9)	5.04e-08	2.35e-08	2.01e-08	9.40e-08	0.2
38	r993 (EX_DW01_add_8)	5.11e-08	2.38e-08	1.96e-08	9.46e-08	0.2
39	sub_918 (EX_DW01_sub_2)	1.05e-07	4.41e-08	2.41e-08	1.73e-07	0.4
40	sub_921 (EX_DW01_sub_1)	1.84e-08	2.35e-08	2.09e-08	6.28e-08	0.2
41	sub_924 (EX_DW01_sub_0)	2.42e-08	9.77e-09	2.23e-08	5.62e-08	0.1
42	mult_884 (EX_DW_mult_uns_0)	1.99e-07	1.65e-07	1.55e-07	5.19e-07	1.3
43	add_0_root_add_831_2 (EX_DW01_add_4)	2.59e-07	8.27e-08	1.79e-08	3.59e-07	0.9
44						
45	step4 (WB)	6.30e-06	3.73e-07	2.82e-07	6.96e-06	17.9

第三部分：APR 佈局結果 (Layout View)



第四部分：心得

在這次的作業中，花費最多時間的應該是在前面切分 module 的時候，會有各種各樣的 error，有時候也不是很確定發生什麼事，但牽一髮就動全身，在切分 module 的時候可以去 trace 部分的 pipeline，有點像是計算機組織學到的內容，還記得計算機組織那一張 MIPS 的 pipeline 圖，就跟這一次 thumb 的 instruction set 蠻相似的，看到 PC 或是各指令的傳送，透過觀察 verilog，對整體 pipeline 也更有概念，後面做 APR 的時候，雖然有很多部分不懂，需要去 google，但是看到最後的成品出來也很有成就感，在這份作業中碰到很多新東西也學到很多。

