



CIRCUIT THEORY AND ELECTRONICS FUNDAMENTALS

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LABORATORY T2

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Contents

| | | |
|----------|--|-----------|
| 1 | Introduction | 1 |
| 2 | Theoretical Analysis | 2 |
| 2.1 | Circuit analysis for $t < 0$ | 3 |
| 2.2 | Circuit analysis for a voltage source-equivalent capacitor | 4 |
| 2.3 | Circuit analysis for $t > 0$ | 6 |
| 2.3.1 | Transient analysis: Natural solution | 6 |
| 2.3.2 | Transient analysis: Forced solution | 7 |
| 2.3.3 | Transient analysis: Final solution | 9 |
| 2.3.4 | Frequency analysis | 9 |
| 3 | Simulation Analysis | 11 |
| 3.1 | Circuit analysis for $t < 0$ | 11 |
| 3.2 | Circuit analysis for a voltage source-equivalent capacitor | 12 |
| 3.3 | Circuit analysis for $t > 0$ | 13 |
| 3.3.1 | Transient analysis: Natural solution | 13 |
| 3.3.2 | Transient analysis: Final solution | 14 |
| 3.3.3 | Frequency analysis | 15 |

| | | |
|----------|--|-----------|
| 4 | Result Analysis | 19 |
| 4.1 | Circuit analysis for $t < 0$ | 19 |
| 4.2 | Circuit analysis for a voltage source-equivalent capacitor | 21 |
| 4.3 | Circuit analysis for $t > 0$ | 23 |
| 4.3.1 | Transient analysis: Natural solution | 23 |
| 4.3.2 | Transient analysis: Final solution | 24 |
| 4.3.3 | Frequency analysis | 25 |
| 5 | Conclusion | 26 |

1 Introduction

The objective of this laboratory assignment is to study a circuit supplied by two voltage sources and one current source. The two voltage sources (one dependent, V_d , and one independent, V_s), and the current source (I_b), which is a dependent one, are connect to 7 different resistors (R_{1-7}) and to one capacitor (C). The voltage source (V_s) varies in time according to the equations 1 and 2. The circuit can be seen in Figure 1.

In Section 2, a theoretical analysis of the circuit is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 5.

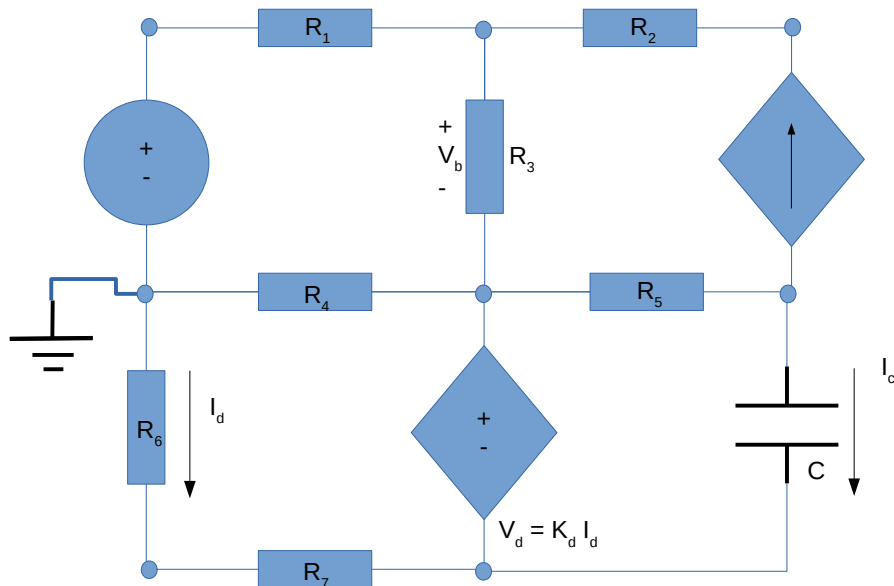


Figure 1: Voltage and Current driven circuit with 7 resistors and 1 capacitor.

$$u(t) = \begin{cases} 0, & t < 0 \\ 1, & t \geq 0 \end{cases} , \quad (1)$$

$$v_s(t) = V_s u(-t) + \sin(2\pi ft) u(t) . \quad (2)$$

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically.

This circuit has 4 meshes, in which we assume the current flows clockwise (Figure 2), and 8 nodes (Figure 3).

The voltage source v_s has a voltage of V_s for $t \leq 0$. For $t > 0$ its voltage varies with time according to equation 2.

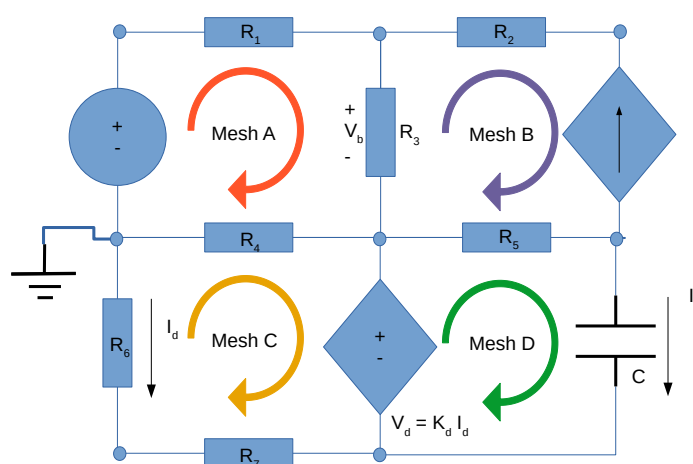


Figure 2: Current flow on each mesh.

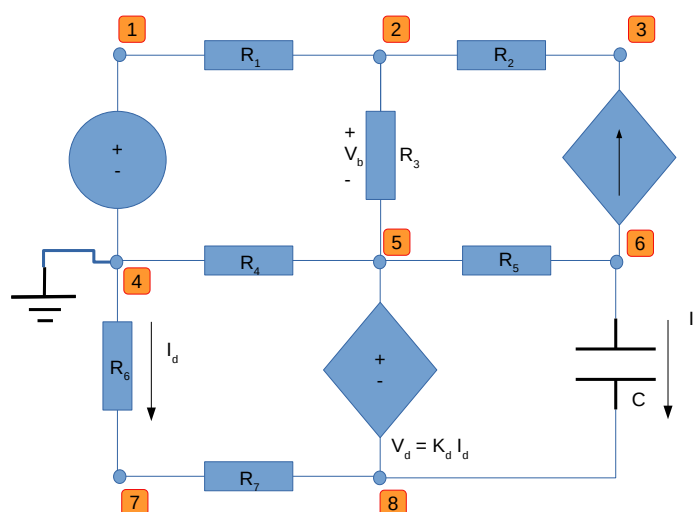


Figure 3: Nodes and their respective labels.

2.1 Circuit analysis for $t < 0$

For $t < 0$, $v_s = V_s$ and the capacitor acts like an open circuit ($I_c = 0$) since it is fully charged.

There are 8 nodes in total which means that we need 8 linearly independent equations to find out the voltages in each node and solve the circuit. Therefore, we use the Kirchhoff Current Law (KCL, shown in equation 3) in every node that is not connected to a voltage source (nodes 2, 3, 6 and 7, which are identified in Figure 1).

$$\sum_{k=1}^n I_k = 0. \quad (3)$$

Node 4 (the reference node) is connected to the ground, which means that its voltage (V_0) is 0.

It is also known that the value of a voltage source is equivalent to the difference of the voltages in each node to which the source is connected. That allows us to create two more equations, since there are two voltage sources in the circuit.

For the 8th equation we can create a *supernode* with nodes 5 and 8, since the dependent voltage source is not connected to the reference node. Through this method, nodes 5 and 8 are regarded as one single node (a *supernode*) by ignoring the voltage source between them.

To demonstrate the process, the node 2 equation resulting from the KCL application is the following:

$$(V_2 - V_3) \cdot G_2 = (V_5 - V_2) \cdot G_3 + (V_1 - V_2) \cdot G_1. \quad (4)$$

Doing this on all possible nodes/supernode and adding the extra equations, regarding the voltage sources, a system of linear equations can be obtained and solved with the aid of *Octave*. The results are presented on table 1.

| Name | Value [V] |
|------|---------------|
| V1 | 5.2482503879 |
| V2 | 4.9432441222 |
| V3 | 4.3036067811 |
| V4 | 0.0000000000 |
| V5 | 4.9860998009 |
| V6 | 5.9361135727 |
| V7 | -1.9166178707 |
| V8 | -2.8778549027 |

Table 1: Results from the node analysis, from *Octave*.

While analysing the current in each mesh we used the Kirchhoff Voltage Law (KVL, shown in equation 5) in every mesh. However, it would be equivalent to use Ohm's law (equation 6) since we already know the resistance of each resistor and the voltage at every node. The results of this analysis are shown in table 2.

$$\sum_{k=1}^n V_k = 0 , \quad (5)$$

$$R = \frac{V}{I} . \quad (6)$$

| Name | Value [A] |
|------|---------------|
| Ia | 0.0002949313 |
| Ib | 0.0003087683 |
| Ic | -0.0009468802 |
| Id | -0.0000000000 |

Table 2: Results from the mesh analysis, from *Octave*.

Since we know the current on each mesh we can compute the current on every branch with the aid of KCL (equation 3). The results can be seen in table 3.

| Name | Value [A] |
|------|---------------|
| C | -0.0000000000 |
| Ib | 0.0003087683 |
| R1 | 0.0002949313 |
| R2 | 0.0003087683 |
| R3 | -0.0000138371 |
| R4 | -0.0012418114 |
| R5 | 0.0003087683 |
| R6 | -0.0009468802 |
| R7 | -0.0009468802 |

Table 3: Results from mesh analysis, using *Octave*.

2.2 Circuit analysis for a voltage source-equivalent capacitor

Studying the circuit with the capacitor acting as a voltage source is equivalent to studying the circuit for $t = 0$. As stated, the independent voltage source has a voltage of 0 volts and therefore is

equivalent to a conductor wire on a closed circuit. Knowing this, it is possible to obtain the equivalent resistance of the circuit, and, therefore, obtain τ (the time constant of the capacitor).

A node analysis was performed similarly to what was done before. The capacitor voltage (V_x) was defined as $V_x = V_6 - V_8$, where V_6 and V_8 are the voltages in node 6 and 8, respectively, obtained on the first analysis (2.1). The results are expressed in table 4.

| Name | Value [V] |
|------|---------------|
| V1 | -0.0000000000 |
| V2 | -0.0000000000 |
| V3 | 0.0000000000 |
| V4 | 0.0000000000 |
| V5 | 0.0000000000 |
| V6 | 8.8139684754 |
| V7 | -0.0000000000 |
| V8 | 0.0000000000 |

Table 4: Results obtained from node analysis, using *Octave*.

Once again, the currents are calculated similarly to the previous section and are presented on the following table (table 5):

| Name | Value [A] |
|------|---------------|
| C | -0.0028646681 |
| Ib | 0.0000000000 |
| R1 | -0.0000000000 |
| R2 | 0.0000000000 |
| R3 | 0.0000000000 |
| R4 | 0.0000000000 |
| R5 | -0.0028646681 |
| R6 | 0.0000000000 |
| R7 | 0.0000000000 |

Table 5: Results obtained from mesh analysis, using *Octave*.

Here, we establish an equivalence between the capacitor and a voltage source, in order to compute the equivalent resistance (R_{eq}). R_{eq} is the scalar resistance value obtained by substituting the entire circuit by a single voltage source and a single resistor, connected in series, via *Thévenin's Equivalence*

Theorem. To calculate this scalar, we divide the voltage differential on the capacitor and its current to obtain the resistance, using Ohm's Law (6).

With the aid of this new information, it is possible to calculate the time constant (τ). For a RC circuit, the time constant can be obtained from the following equation (7):

$$\tau = R_{eq} \cdot C \quad (7)$$

The results for R_{eq} and τ are present on the table 6:

| Name | Value |
|----------|-----------------|
| R_{eq} | 3076.7852319200 |
| τ | 0.0031175171 |

Table 6: R_{eq} (in Ω) and τ (in s), from *Octave*.

2.3 Circuit analysis for $t > 0$

2.3.1 Transient analysis: Natural solution

As a result from the previous analysis (table 5) we know that $V_8 = 0$ and therefore $V_x = V_6$.

Knowing that this circuit only contains one capacitor and all the other components are resistors and voltage/current sources, the voltage of the capacitor (v_x) can be given by equation 8:

$$v_x(t) = v_x(+\infty) + [v_x(0) - v_x(+\infty)]e^{-\frac{t}{\tau}}, \quad (8)$$

where $v_x(0) = V_x = V_6 - V_8$ and $v_x(+\infty) = 0$, since the capacitor will tend to discharge completely over time.

With this, we can plot V_6 , as seen in image 4:

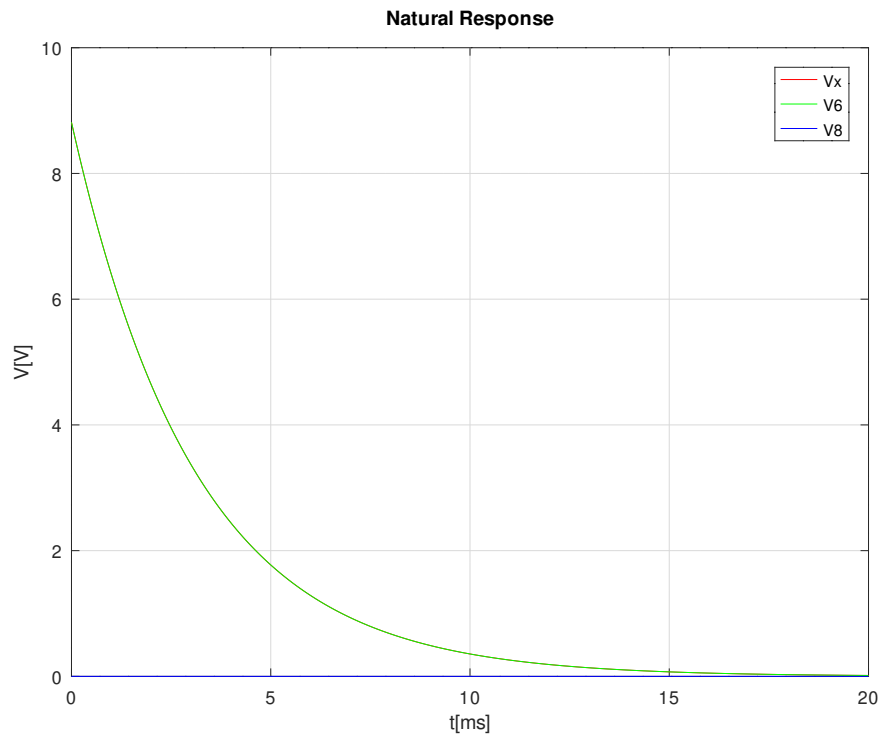


Figure 4: Natural response.

2.3.2 Transient analysis: Forced solution

To find the forced solution, we used complex numbers in order to simplify the calculations. Every component of the circuit but the sources was substituted by a "black box" with the same impedance (Z), which can be calculated using equation 9 (Phasor Ohm's Law) for resistors and equation 10 for capacitors.

$$Z_R = \frac{\tilde{V}}{\tilde{I}} = R , \quad (9)$$

$$Z_C = \frac{1}{j\omega C} . \quad (10)$$

The voltage source V_s is now imposing a sinusoidal excitation on the circuit with a frequency (f) of $1KHz$, and therefore its voltage varies in time according to the wave equation 11.

$$v(t) = V \cos(\omega t - \phi) . \quad (11)$$

Knowing that $v_s(0) = 0$, $V_s = 1V$ and that $\omega = 2\pi f$, we find v_s 's phase (ϕ) value which is 90° .

At last, we use the KCL (equation 3) in every node possible as described in subsection 2.1, computing the voltage in each node.

The voltage in this case is a complex number. By taking its absolute value we obtain the magnitude, while the phase is obtained by taking its argument. With both values computed, the plot for the voltages can be made according to the equation 11.

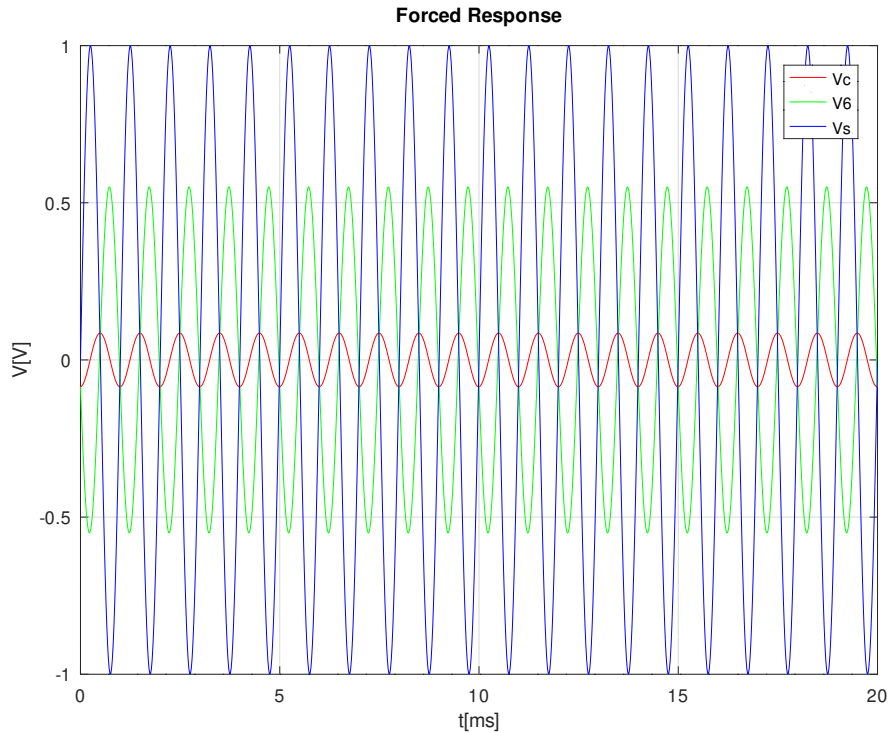


Figure 5: Forced response.

Table 7: Phase and magnitude of the voltage on each node

| (a) Magnitude | | (b) Phase | |
|---------------|--------------|-----------|-----------------|
| Name | Value [V] | Name | Value [Degrees] |
| V1 | 1.0000000000 | V1 | 0.0000000000 |
| V2 | 0.9418842008 | V2 | 0.0000000000 |
| V3 | 0.8200079004 | V3 | 0.0000000000 |
| V4 | 0.0000000000 | V4 | 0.0000000000 |
| V5 | 0.9500499085 | V5 | 0.0000000000 |
| V6 | 0.5506603547 | V6 | -171.0661663314 |
| V7 | 0.3651917742 | V7 | 180.0000000000 |
| V8 | 0.5483455799 | V8 | 180.0000000000 |

2.3.3 Transient analysis: Final solution

Since the natural and forced responses are already known, the final solution can be calculated simply by adding the natural and forced responses together. By doing this we obtain the following graph (Figure 6):

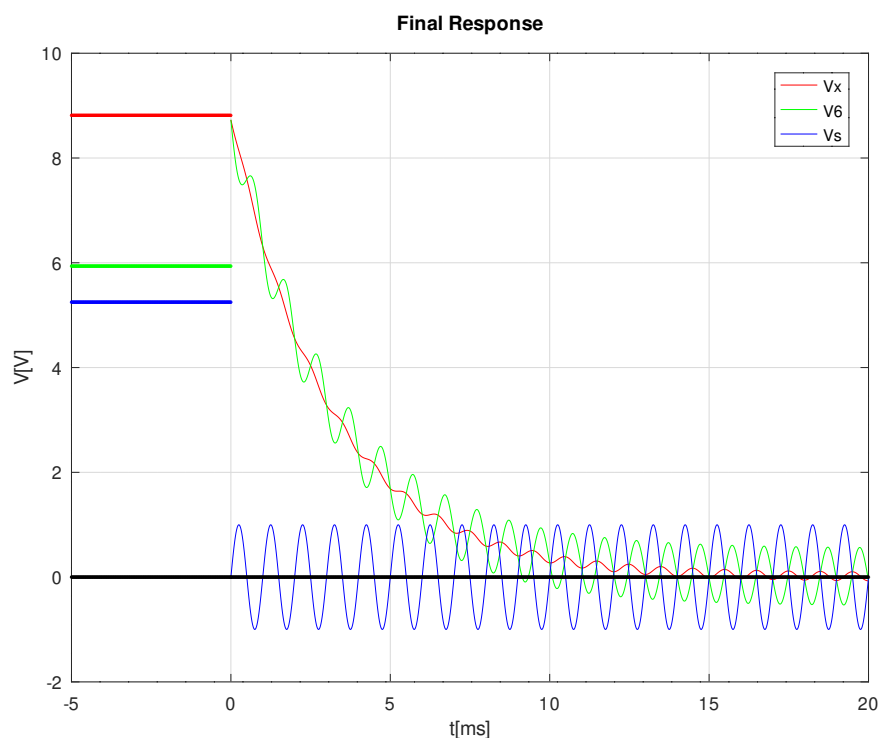


Figure 6: Final response.

The voltages before the oscillating regime were also added to this graph, with the purpose of showing the boundary conditions.

2.3.4 Frequency analysis

By iterating what was made in previous subsections while changing the frequency, it was possible to analyse the frequency variation's impact on the magnitude and phase on each node. The outcome may be seen in figures 7 and 8.

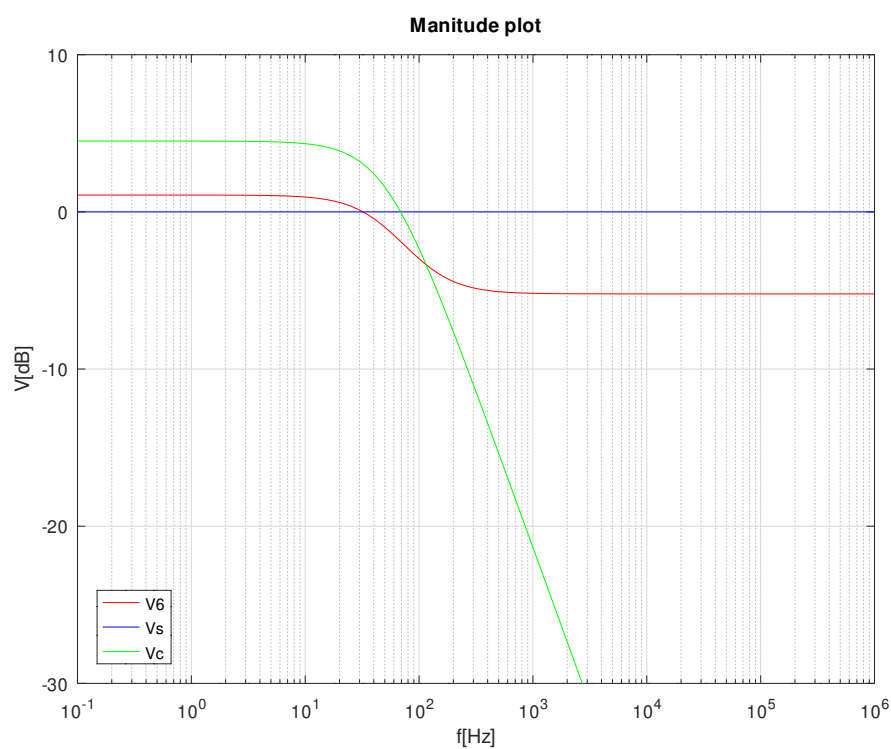


Figure 7: Magnitude graph.

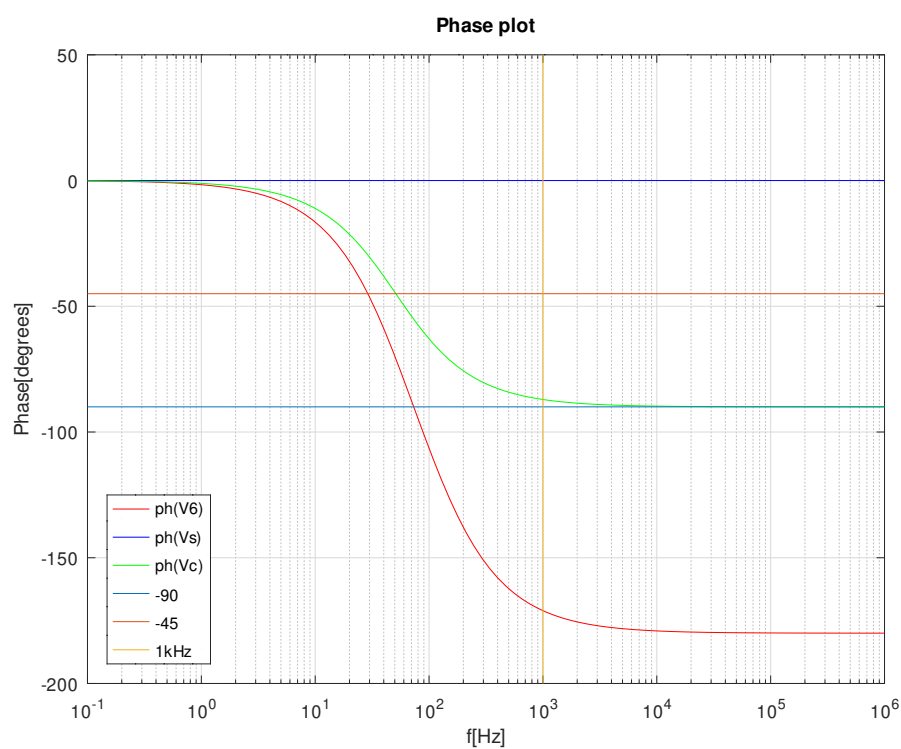


Figure 8: Phase graph.

3 Simulation Analysis

This section discusses the circuit simulation, performed using *Ngspice*.

This circuit was entered into the *Ngspice* simulation environment. This tool is used to simulate analog electronic circuits and predict circuit behaviour. This *Ngspice* simulation begins by defining the reference node, which is the node with potential 0 (by convention). In *Ngspice*, this node is represented by V_0 . In our theoretical analysis, the reference node was node 4. However node 4 is still needed because we must introduce a voltage source with 0V potential, in order to measure the current I_c for the dependent voltage source, since *Ngspice* considers the voltage sources as Ammeters. The new diagram, which represents more accurately what was introduced in *Ngspice*, is shown on Figure 9.

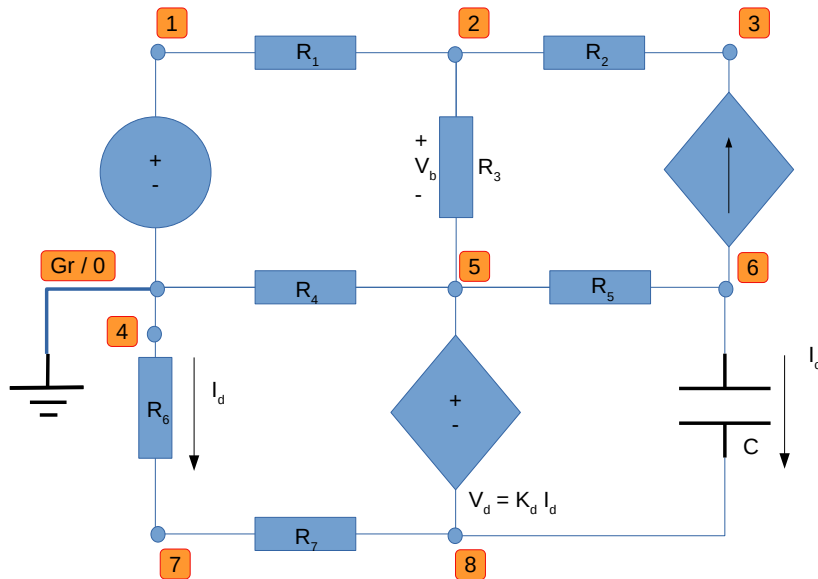


Figure 9: Voltage and Current driven circuit with 7 resistors.

3.1 Circuit analysis for $t < 0$

Table 8 shows the simulated operating point results for the circuit under analysis when $t < 0$, which means that the capacitor acts as an open circuit and therefore $I_c = 0$.

| Name | Value [A or V] |
|---------|----------------|
| @c[i] | 0.000000e+00 |
| @gcs[i] | 3.087679e-04 |
| @r1[i] | 2.949312e-04 |
| @r2[i] | 3.087679e-04 |
| @r3[i] | -1.38367e-05 |
| @r4[i] | -1.24181e-03 |
| @r5[i] | 3.087679e-04 |
| @r6[i] | -9.46880e-04 |
| @r7[i] | -9.46880e-04 |
| v(1) | 5.248250e+00 |
| v(2) | 4.943244e+00 |
| v(3) | 4.303607e+00 |
| v(4) | 0.000000e+00 |
| v(5) | 4.986098e+00 |
| v(6) | 5.936111e+00 |
| v(7) | -1.91662e+00 |
| v(8) | -2.87785e+00 |

Table 8: Operating point analysis. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

3.2 Circuit analysis for a voltage source-equivalent capacitor

Table 9 shows the simulated operating point results for the circuit under analysis when the capacitor acts as a voltage source outputting: $V_X = V_6 - V_8$ and the voltage source is turned off ($V_s = 0$).

| Name | Value [A or V] |
|---------|----------------|
| @gcs[i] | 0.000000e+00 |
| @r1[i] | 0.000000e+00 |
| @r2[i] | 0.000000e+00 |
| @r3[i] | 0.000000e+00 |
| @r4[i] | 0.000000e+00 |
| @r5[i] | -2.86467e-03 |
| @r6[i] | 0.000000e+00 |
| @r7[i] | 0.000000e+00 |
| v(1) | 0.000000e+00 |
| v(2) | 0.000000e+00 |
| v(3) | 0.000000e+00 |
| v(4) | 0.000000e+00 |
| v(5) | 0.000000e+00 |
| v(6) | 8.813968e+00 |
| v(7) | 0.000000e+00 |
| v(8) | 0.000000e+00 |

Table 9: Operating point analysis. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

3.3 Circuit analysis for $t > 0$

3.3.1 Transient analysis: Natural solution

In this graphic present on the Figure 10, we see the natural solution of the voltage in node 6 ($v_6(t)$) when $V_S = 0$, during the first 20 ms.

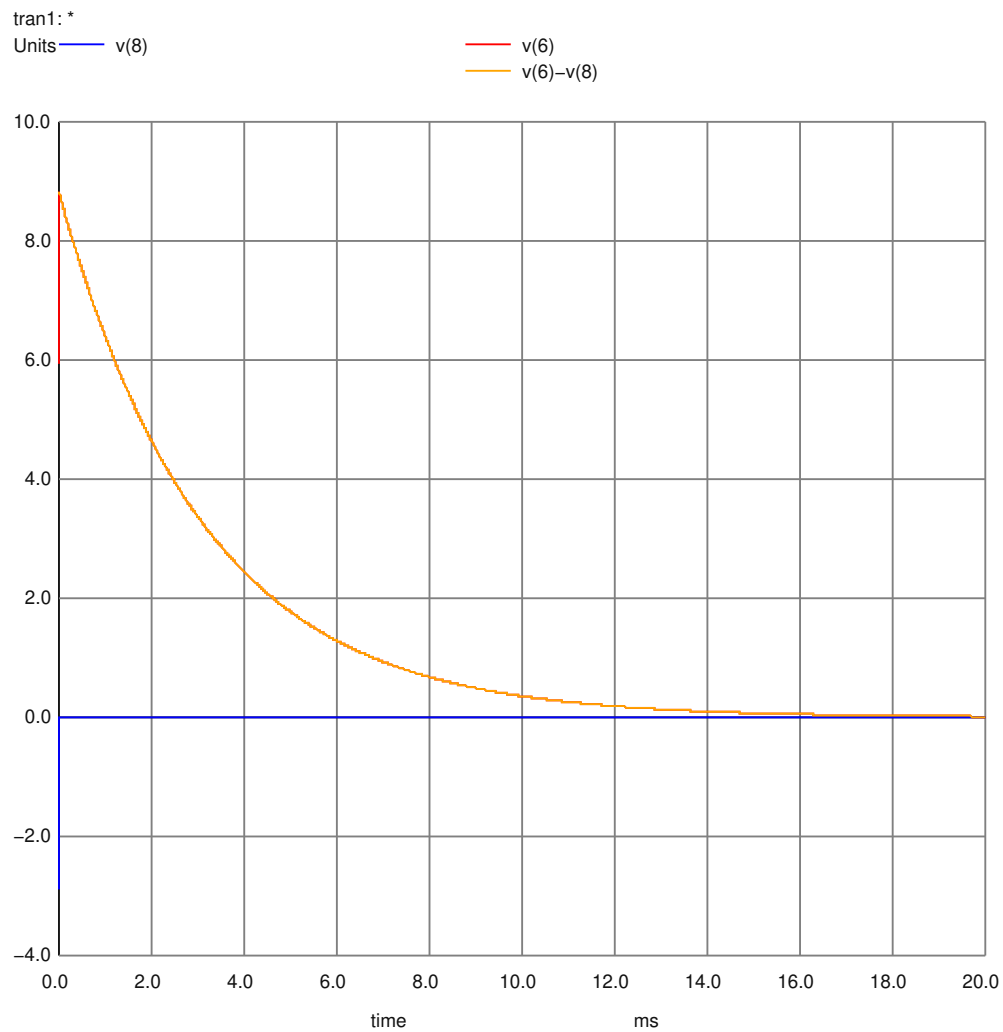


Figure 10: Natural response.

3.3.2 Transient analysis: Final solution

After adding the normal and the complex solutions, the final solution is obtained, which can be seen in this graphic (Figure 11).

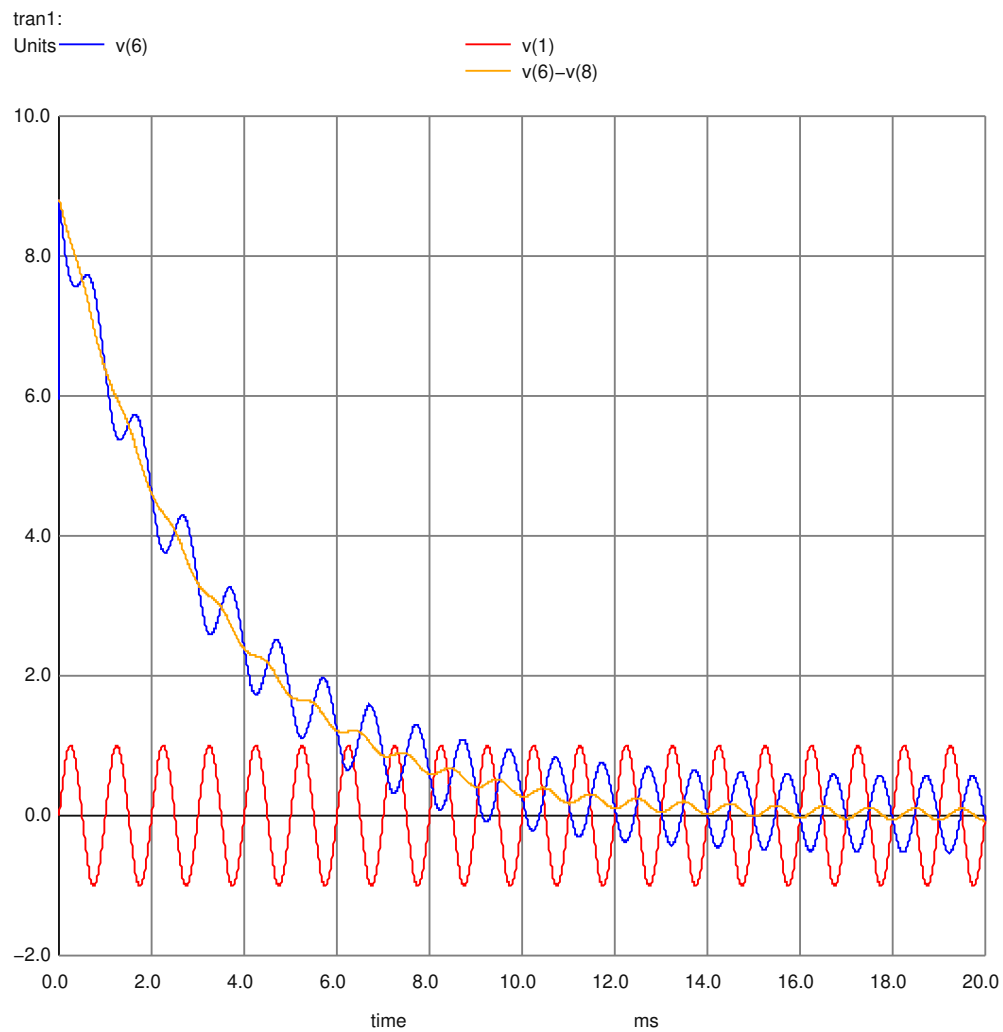


Figure 11: Forced response.

3.3.3 Frequency analysis

When varying the frequency from 0,1 Hz to 1 MHz we get these graphics, which show how the magnitude (Figure 12 and 13) and the phase (Figure 14) vary with this change.

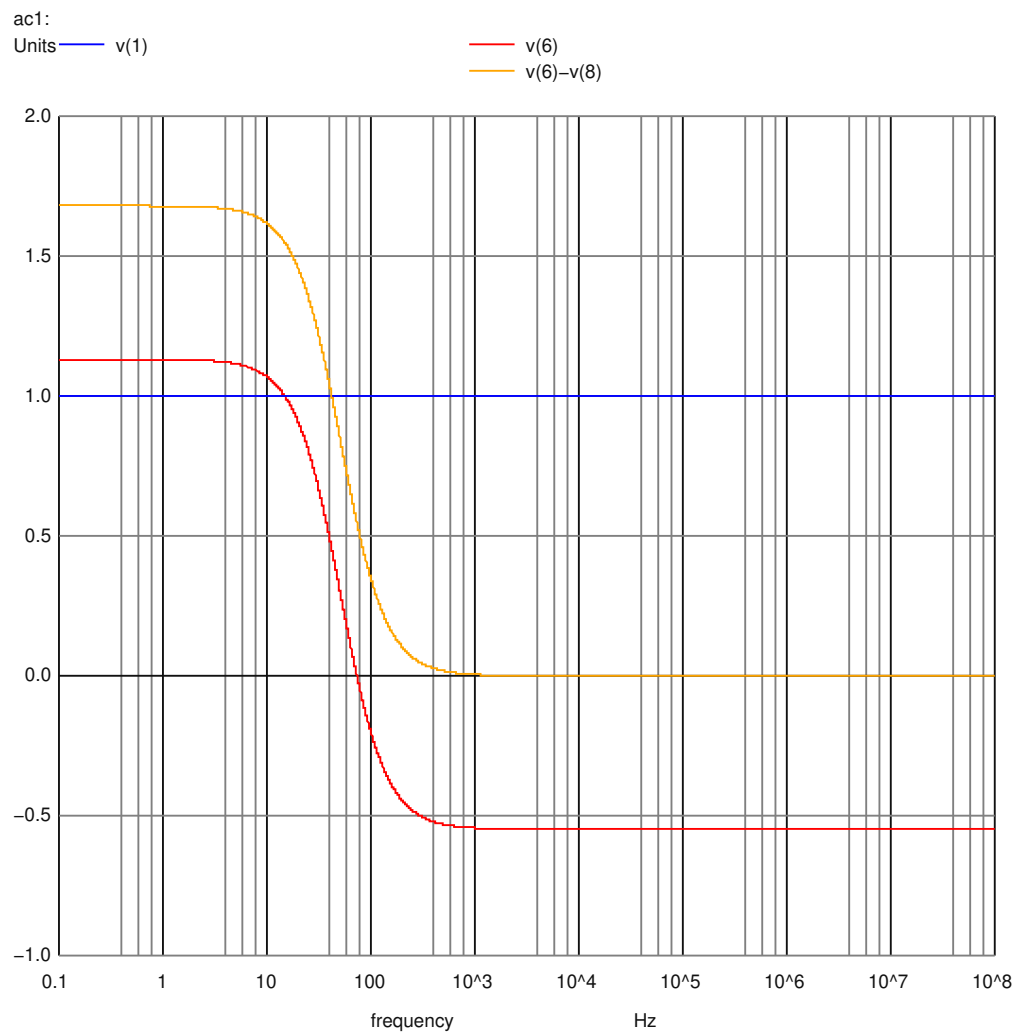


Figure 12: Magnitude graph in volts.

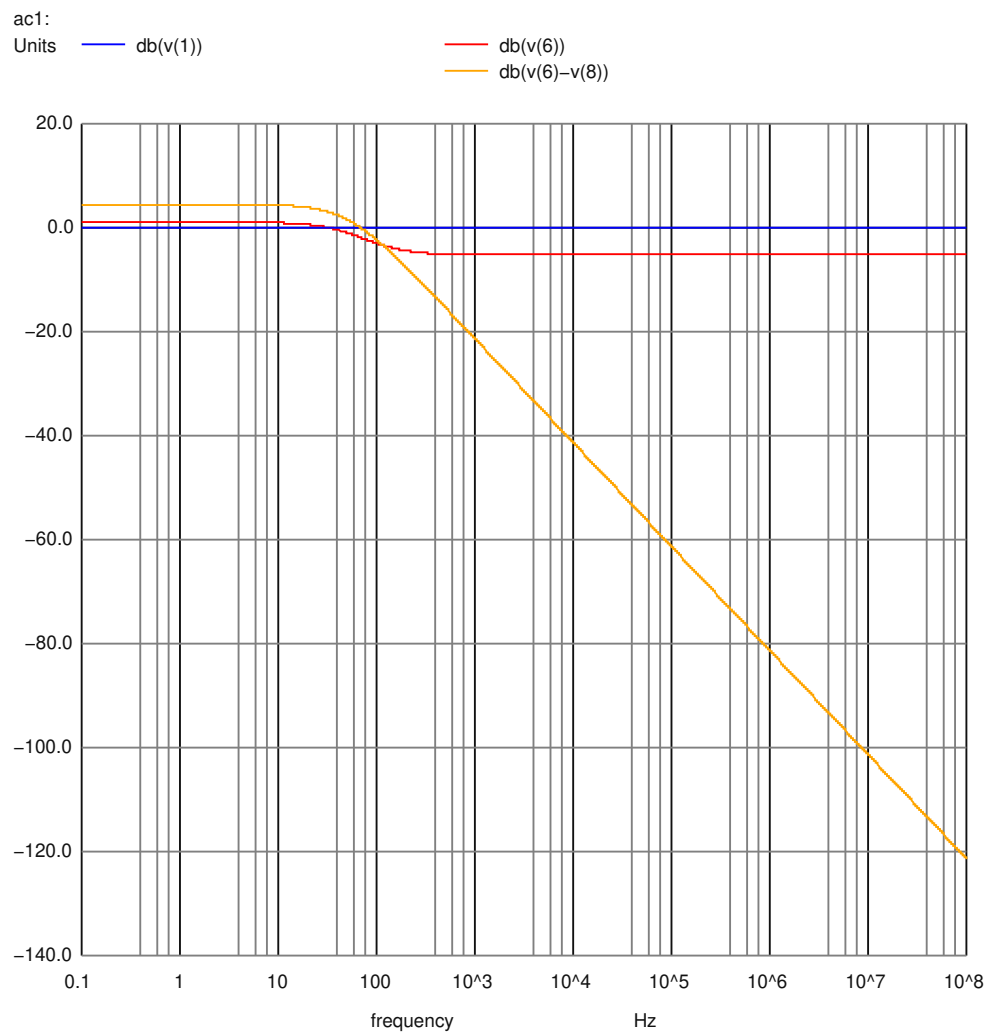


Figure 13: Magnitude graph in dB.

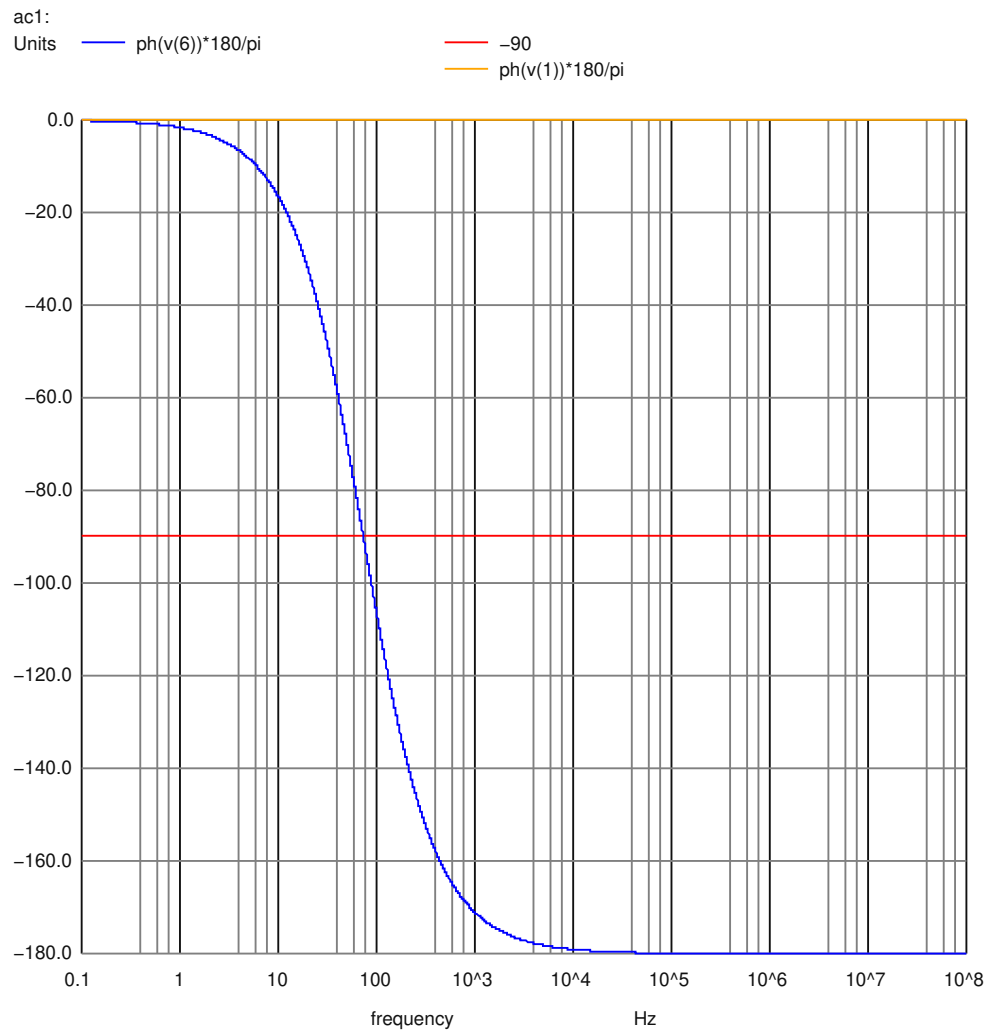


Figure 14: Phase graph in degrees.

4 Result Analysis

In this section the results will firstly be analysed and then compared, identifying the differences between the calculated results and the simulation results. The relative differences are calculated according to equation 12:

$$e_r = \frac{V_{Octave} - V_{ngspice}}{V_{Octave}} \quad (12)$$

4.1 Circuit analysis for $t < 0$

Table 10: Results from the first analysis

| (a) Octave | | (b) Ngspice | |
|------------|---------------|-------------|----------------|
| Name | Value [V] | Name | Value [A or V] |
| V1 | 5.2482503879 | @c[i] | 0.000000e+00 |
| V2 | 4.9432441222 | @gcs[i] | 3.087679e-04 |
| V3 | 4.3036067811 | @r1[i] | 2.949312e-04 |
| V4 | 0.0000000000 | @r2[i] | 3.087679e-04 |
| V5 | 4.9860998009 | @r3[i] | -1.38367e-05 |
| V6 | 5.9361135727 | @r4[i] | -1.24181e-03 |
| V7 | -1.9166178707 | @r5[i] | 3.087679e-04 |
| V8 | -2.8778549027 | @r6[i] | -9.46880e-04 |
| | | @r7[i] | -9.46880e-04 |
| Name | Value [A] | v(1) | 5.248250e+00 |
| C | -0.0000000000 | v(2) | 4.943244e+00 |
| Ib | 0.0003087683 | v(3) | 4.303607e+00 |
| R1 | 0.0002949313 | v(4) | 0.000000e+00 |
| R2 | 0.0003087683 | v(5) | 4.986098e+00 |
| R3 | -0.0000138371 | v(6) | 5.936111e+00 |
| R4 | -0.0012418114 | v(7) | -1.91662e+00 |
| R5 | 0.0003087683 | v(8) | -2.87785e+00 |
| R6 | -0.0009468802 | | |
| R7 | -0.0009468802 | | |

The values match almost perfectly. On the table below, the differences are studied with more detail.

Table 11: Differences on the first analysis

| (a) Voltages | | (b) Currents | |
|--------------|------------------|--------------|------------------|
| Name | Value [V] | Name | Value [A] |
| V1 | 0.0000000739 | C | NaN |
| V2 | 0.0000000247 | Ib | 0.0000012955 |
| V3 | -0.0000000509 | R1 | 0.0000003391 |
| V4 | NaN | R2 | 0.0000012955 |
| V5 | 0.0000003612 | R3 | 0.0000289078 |
| V6 | 0.0000004334 | R4 | 0.0000011274 |
| V7 | -0.0000011110 | R5 | 0.0000012955 |
| V8 | 0.0000017036 | R6 | 0.0000002112 |
| | | R7 | 0.0000002112 |

This results are commented and explained on the next subsection (subsection 4.2) since they require the same explanation.

4.2 Circuit analysis for a voltage source-equivalent capacitor

Table 12: Results from the second analysis

| (a) Octave | | (b) Ngspice | |
|------------|---------------|-------------|----------------|
| Name | Value [V] | Name | Value [A or V] |
| V1 | -0.0000000000 | @gcs[i] | 0.000000e+00 |
| V2 | -0.0000000000 | @r1[i] | 0.000000e+00 |
| V3 | 0.0000000000 | @r2[i] | 0.000000e+00 |
| V4 | 0.0000000000 | @r3[i] | 0.000000e+00 |
| V5 | 0.0000000000 | @r4[i] | 0.000000e+00 |
| V6 | 8.8139684754 | @r5[i] | -2.86467e-03 |
| V7 | -0.0000000000 | @r6[i] | 0.000000e+00 |
| V8 | 0.0000000000 | @r7[i] | 0.000000e+00 |
| Name | Value [A] | v(1) | 0.000000e+00 |
| C | -0.0028646681 | v(2) | 0.000000e+00 |
| Ib | 0.0000000000 | v(3) | 0.000000e+00 |
| R1 | -0.0000000000 | v(4) | 0.000000e+00 |
| R2 | 0.0000000000 | v(5) | 0.000000e+00 |
| R3 | 0.0000000000 | v(6) | 8.813968e+00 |
| R4 | 0.0000000000 | v(7) | 0.000000e+00 |
| R5 | -0.0028646681 | v(8) | 0.000000e+00 |
| R6 | 0.0000000000 | | |
| R7 | 0.0000000000 | | |

An interesting result appears from this procedure: we notice that the current flows exclusively on the capacitor's mesh (mesh D), on resistor R5. This is explained by the fact that "*current always flows through the path of least resistance*": since the linearly dependent voltage source has voltage 0 in this instant, it is equivalent to a conductor wire with 0 resistance, configuring a closed circuit with only one resistor (R5). This result appears on table 12.

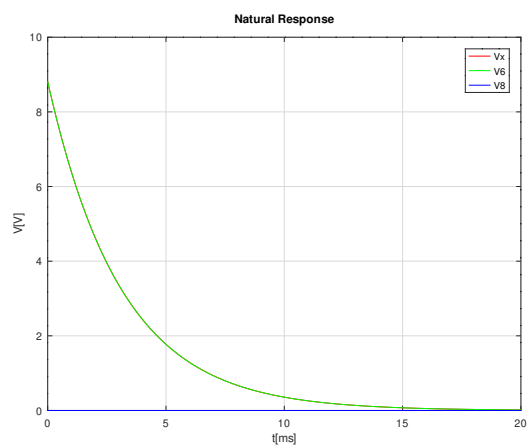
Table 13: Differences on the second analysis

| (a) Voltages | | (b) Currents | |
|--------------|--------------|--------------|---------------|
| Name | Value [V] | Name | Value [A] |
| V1 | NaN | C | NaN |
| V2 | NaN | Ib | NaN |
| V3 | NaN | R1 | NaN |
| V4 | NaN | R2 | NaN |
| V5 | NaN | R3 | NaN |
| V6 | 0.0000000539 | R4 | -0.0000006633 |
| V7 | NaN | R5 | NaN |
| V8 | NaN | R6 | NaN |

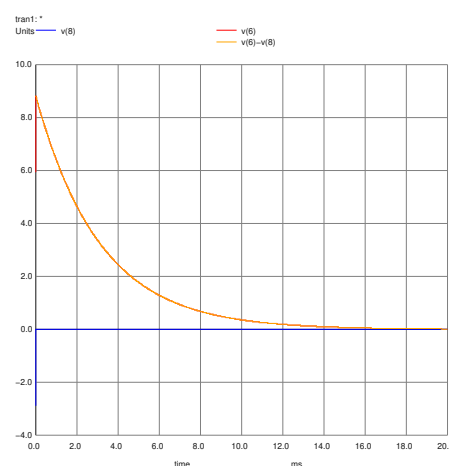
The simulation results from both these procedures (table 11 and 13) match the predicted ones from the theoretical analysis with great precision (errors are mostly in the range of $10^{-4}\%$). This was expected due to the fact that this circuit only contains linear (dependent and independent) components. The capacitor was not included since it was replaced by a simplified version (an open circuit or a voltage source, respectively). One detail which is present on both tables is that "NaN" appears on some of the entries. This results from dividing 0 by 0 which happens when the predicted result by *Octave* is 0 and the difference between *Octave* and *Ngspice* is also 0. Nevertheless, there are very small differences. This could probably originate from numerical approximation on either *Octave* or *Ngspice* or simulation errors.

4.3 Circuit analysis for $t > 0$

4.3.1 Transient analysis: Natural solution



(a) Octave

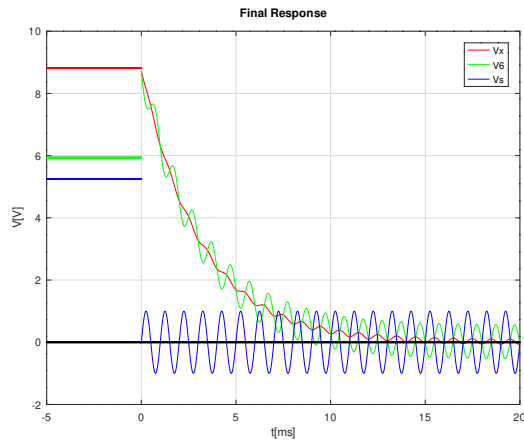


(b) Ngspice

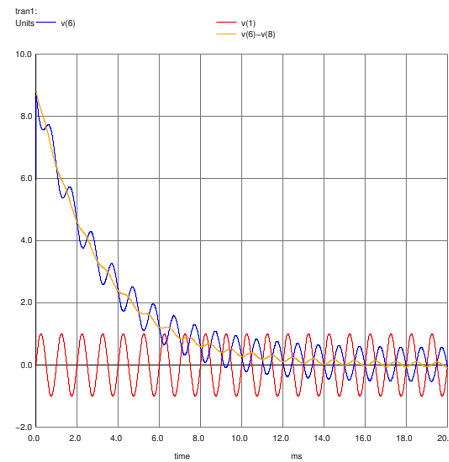
Figure 15: Natural response

As expected the voltages decrease exponentially with time, this represents the capacitor being discharged. Furthermore, it can be seen that the voltage on V_8 is zero and that the lines of V_6 and V_x are overlapping, meaning the relation $V_x = V_6$ is proved.

4.3.2 Transient analysis: Final solution



(a) Octave

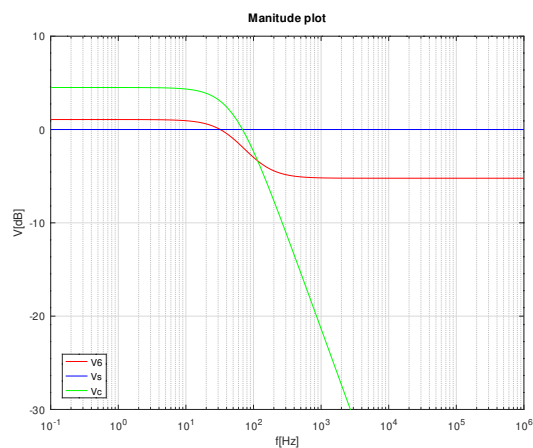


(b) Ngspice

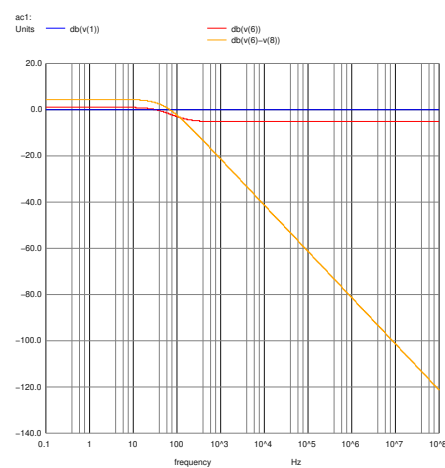
Figure 16: Natural response

One aspect that should be mentioned about this data is that the phase of the capacitor is offset to the voltage source by approximately 180° , and V_c is offset by approximately 90° . Therefore, it is possible to deduce that the current's frequency is greater than the cut-off frequency of this low pass filter (this topic will be further analysed below, on section 4.3.3). Moreover, V_x decreases with time, approaching zero, but maintains the oscillating regime. This means the capacitor is being discharged until its average is zero. Once this happens the capacitor is lightly charged and discharged in the same frequency as the source.

4.3.3 Frequency analysis

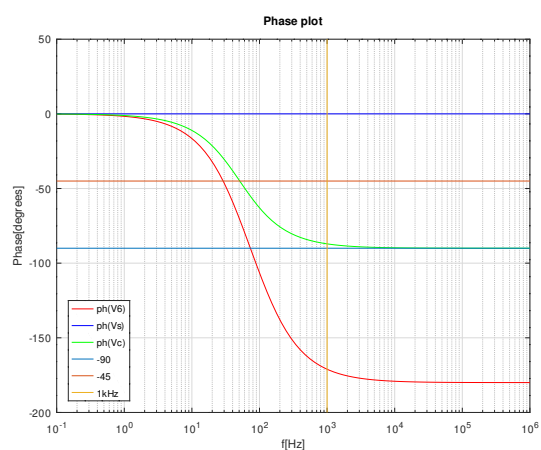


(a) Octave

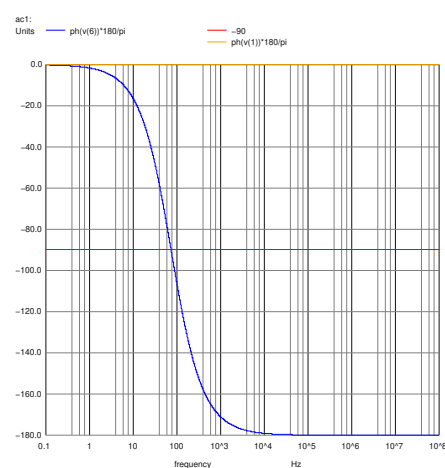


(b) Ngspice

Figure 17: Natural response



(a) Octave



(b) Ngspice

Figure 18: Natural response

V_s remains constant since it is the voltage that was taken as the reference (it is an independent voltage source). V_6 and V_c , on the other hand, have an asymptotic behaviour, tending to offset -180° and -90° , respectively.

These graphs confirm that the circuit can be classified as a low-pass filter, since, for low frequencies, the magnitude of voltage on the capacitor ($V_6 - V_8$) is close to the one from the voltage source. However this changes on high frequencies, the voltage drops drastically if the frequency increases.

As seen on figure 8, the cutoff frequency is around 50Hz . This value can be confirmed by calculating it according to the equation 13: 51.05 Hz . By definition, this frequency is the one with a phase of 45° .

$$f_{cutoff} = \frac{1}{2\pi \cdot R_{eq} \cdot C} \quad (13)$$

5 Conclusion

In this laboratory assignment, the objective of analysing a circuit with a capacitor has been achieved. This circuit has been analysed using *Operating point*, *transient* and *frequency* analysis. The *Operating point* analysis was conducted like in the previous laboratory assignment, using node and mesh analysis. The *transient* and *frequency* analysis were based on phasors and on the nodal method using imaginary numbers.

The theoretical section has been solved using the *Octave* Maths tool to compute all the previous values. Those results were then confronted with the simulation results, which were obtained by using the *Ngspice* tool, resulting in an almost perfect match (with a level of precision of 10^{-5}).